

# National Nanofabrication Users Network

## Research Experience for Undergraduates Program



**Stanford University**  
**August 12-14, 1999**

**NNUN** *National  
Nanofabrication  
Users Network*



## **Welcome to Stanford !!!**

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*The National Nanofabrication Users Network Research Experience for Undergraduates Program is generously supported by the National Science Foundation, the NNUN Sites, and Industry Sponsors.*

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**On Thursday August 12th, participants will be arriving at Stanford. Accommodations have been arranged for the NNUN REU interns at the Wilbur dormitories on campus. All talks will be held in the David Packard Electrical Engineering Building, Room 101.**

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|-----------------------------|-----------------------------------|-------------|--------------------------------------------------------------------------------------------------------------------|
| <b>4:00 - 4:30</b>          | <b>Greetings and Introduction</b> |             |                                                                                                                    |
| <b>4:30 - 5:00</b>          | <b>Guest Speaker: Cal Quate</b>   |             | <b>Cantilever Arrays as Mechanical Systems:<br/>A Project for MEMS</b>                                             |
| <b>Moderator: Mike Deal</b> |                                   |             |                                                                                                                    |
| <b>5:00 - 5:13</b>          | <b>Martino Poggio</b>             | <b>UCSB</b> | <b>Coherent Control and Measurement of Single Quantum Dots</b>                                                     |
| <b>5:13 - 5:39</b>          | <b>Kohli/Ma</b>                   | <b>HU</b>   | <b>Effects of Metallization on Ideality Factors of GaAs &amp; 3C-SiC Schottky-Barrier Diodes</b>                   |
| <b>5:40 - 6:40</b>          | <b>Dinner</b>                     |             |                                                                                                                    |
| <b>6:41 - 6:54</b>          | <b>Emma Wong</b>                  | <b>SU</b>   | <b>Electrical Characterization of Diffusion Barrier Properties For Copper Metallization in Integrated Circuits</b> |
| <b>6:54 - 7:07</b>          | <b>Nam Thai</b>                   | <b>SU</b>   | <b>Reverse Annealing of Boron in Isochronal Anneal</b>                                                             |
| <b>7:07 - 7:20</b>          | <b>Karen Rantamaki</b>            | <b>SU</b>   | <b>Pulsed Laser Formation of Cobalt Disilicide</b>                                                                 |
| <b>7:20 - 7:33</b>          | <b>Dmitriy Shneyder</b>           | <b>SU</b>   | <b>2-D Oxidation of SiGe</b>                                                                                       |
| <b>7:33 - 7:46</b>          | <b>Joseph Valentino</b>           | <b>SU</b>   | <b>Characterizing Lateral Solid Phase Epitaxy for 3D Device Integration</b>                                        |

**Friday August 13th - - David Packard EE Bldg, Room 101**

**7:45 - 8:00 Continental Breakfast**

**8:00 - 8:15 Introduction**

**Moderator: Bob Davis**

**8:15 - 8:28 Keith Green CU Determining the Multi-Phase Processing Window of Amorphous Silicon**

**8:28 - 8:41 S. Kumar Ravula CU Damascene Tungsten and Poly-Silicon Structures**

**8:41 - 8:54 Ethan Swint CU A Systematic Study of Metallization Techniques Using an Image Reversal Photolithography Lift-off Process**

**8:54 - 9:07 Vanessa Pagán CU Chemical Control of Surface Morphology Copper Deposition on Silicon 100**

**9:07 - 9:20 John Vrakas CU 100nm Polysilicon FET Gates**

**9:20 - 9:33 Ruth Stritsman CU Patterning of CVD Fluorocarbon Resist Using Electron Beam Lithography and Supercritical CO<sub>2</sub> Development**

**9:33 - 10:40 Lab Tour**

**Moderator: James Griffin**

**10:40 - 10:53 Jessica Montañez PSU Self-Assembled Monolayers as Alternative E-beam Lithography Photoresist**

**10:53 - 11:06 Ana Medina PSU Examination of Charging Effects in Electron Beam Lithography on a Leica EBPG-5HR at 50 keV**

**11:06 - 11:19 Joseph Bergevin SU Using Minority Carrier Lifetime to Monitor Process Contamination**

**11:19 - 11:32 Daron Westly CU Applications of Auger Electron Spectroscopy for IC Process Development, Failure Analysis, and Research**

**11:32 - 11:45 Stacie Hvisc SU Study of Oxidation Rates as a Function of Layer Thickness in high Al content AlGaAs**

**11:45 - 11:58 Megan Bader UCSB Thermal Conductivity of Semiconductor Superlattice**

**12:00 - 1:00 Lunch**

**Moderator: Al Flinck**

**1:01 - 1:14 Sandra Garcia UCSB Dry Etch Damage of Gallium Nitride**

**1:14 - 1:27 Adrian Lu SU Fabrication of Sub-Micron Pickup Loops for SQUID Microscopy**

**1:27 - 1:40 Keith O'Doherty UCSB Electron Paramagnetic Resonance and Photoluminescence spectroscopy of F centers in Sodalites**

**1:40 - 1:53 Yen Nguyen PSU Microfabricated Holder For Spatially Constrained Beads For Use In Combinatorial Libraries Analyzed By ToF SIMS**

**1:53 - 2:06 Sean Pham UCSB Microfabrication of Scanning Ion Conductance Microscope/Atomic Force Microscope Probes**

**2:15 - 9:00 Charter Bus to Tech Museum for Innovation, San Jose.**

**Followed by IMAX theater "Everest" and dinner at Il Fornaio, San Jose**

# Saturday August 14th - - David Packard EE Bldg, Room 101

7:45 - 8:00 Continental Breakfast

8:00 - 8:15 Introduction

Moderator: Mary Tang

8:15 - 8:28 Joseph Torralba SU Wafer Bonding for Forming Microscale Fluidic Channels

8:28 - 8:41 Thomas Kenny SU Polymer Hot Embossing With Silicon Templates

8:41 - 8:54 Jean Kim SU Characterization of Etches in Glass Substrates for Fabricating Microfluidic Devices

8:54 - 9:07 Mia DeBarros PSU The Proliferation of Streptomyces on Various Material Surfaces

9:07 - 9:20 Arrelaine Dameron UCSB Vesicles as a Model System Mimicking the Myelin Membrane

9:20 - 9:33 Mike Kimzey PSU Fabrication of Size-Variant Micropatterns for the Culture of Chondrocytes

9:33 - 10:35 Campus Tour

Moderator: Evelyn Hu

10:35 - 10:48 Adam Siegel CU Drug Delivery with Microfluidic Channels for Microelectrode Studies of Cells

10:48 - 11:01 Andrew Kearney UCSB Particle Trapping and Patterning by Optical Tweezers

11:01 - 11:14 Luis Esparza UCSB Thermionic Coolers

11:14 - 11:27 Renee Munoz-Verdejo CU Nano-Structures on Polymers and Measurement of Viscous Flow

11:27 - 11:40 Brianna Norton UCSB Fabrication and Characterization of Copper Chalcogenide Nanoclusters

11:40 - 11:53 Serene van Gent UCSB Search For Novel Open-framework Materials Using Various Copper-based Compounds

12:00 - 1:00 Lunch and Photo session

1:01 - 1:45 Guest Speaker: Greg Kovacs Miniaturization for Biological and Chemical Analysis Systems: Pros and Cons

1:45 - 1:58 Liang-Yu Chen CU Process Development for the Integration of MEMS and RF Devices

1:58 - 2:11 Paul Friedberg SU Multilayer Conducting Beams for MEMS

2:11 - 2:24 Johnathan Carlson CU Dynamic Behavior of Arrays of Coupled Oscillators

2:24 - 2:37 Amber Bullington CU A High Aspect Ratio Comb Drive for a Polysilicon Micromachined Mirror

2:37 - 2:50 Jami Meteer PSU Front-Side Processing for a Piezoelectric MEMS Accelerometer

3:00 - 4:00 Group Session and wrap-up

4:00 - BBQ, Gibbons Grove, Stanford



***THE  
1999  
NNUN  
REU  
ABSTRACTS***

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*In Alphabetical Order  
by Intern's Name*



*Thermal Conductivity of Semiconductor Superlattice*

**Megan Bader**

**Computer Engineering, University of Denver**

**David Clarke, Materials Department, University of California - Santa Barbara**

Heat buildup in lasers can affect performance so an understanding of the parameters which influence thermal conductivity of semiconductor superlattice is important. Thermal transport properties of Group III-V and Group II-VI semiconductor superlattice were studied using the electrical harmonic technique. The effects of interfacial scattering, alloy composition and ordering were systematically measured. Preliminary results show that these influences are crucial to the thermal transport process. In particular, Bragg mirrors for VCSEL and electronic coolers for laser structure were the devices focused on.

*Using Minority Carrier Lifetime to Monitor Process Contamination*

**Joseph E. Bergevin**

**Materials Engineering, San Jose State University**

**James McVittie, Electrical Engineering, Stanford University**

The presence of metal contaminants in cleaning and high temperature processes are detrimental to semiconductor devices. As minority carrier lifetime is reduced by the presence of metal contaminants it is an excellent indicator of process contamination. The carrier lifetime of several silicon wafers were measured using rf-PCD after being subjected to an iodine methanol solution to passivate the wafer surfaces. After establishing a basic methodology for the surface passivation and lifetime measurement we will evaluate the cleaning and high temperature processes at the Stanford Nanofabrication Facility for metal contamination.

*A High Aspect Ratio Comb Drive for a Polysilicon Micromachined Mirror*

**Amber Bullington**

**Electrical Engineering, Cornell University**

**Norman Tien, Electrical Engineering, Cornell University**

High aspect ratio comb drives are needed in microelectromechanical systems (MEMS) to generate the force needed to move structures at high resonant frequencies. Comb drives with aspect ratios greater than 10 to 1 can be achieved with deep reactive ion etching technology.

The focus of this project is to design a high aspect ratio comb drive for a raster-scanning polysilicon mirror. These comb drives can be coupled with polysilicon surface micromachining techniques to fabricate structures such as mirrors that can be used in a video display. This comb drive should increase the maximum achievable resolution compared to a comb drive fabricated directly from polysilicon.

*Dynamic Behavior of Arrays of Coupled Oscillators*

**Johnathan A. Carlson**

**Electrical Engineering, Tennessee Technological University**

**Dustin Carr, Applied Physics, Cornell University**

Arrays of micron-scale torsional paddle oscillators have been fabricated with electron beam lithography and measured using optical interferometry. The dynamic behavior of such systems is complex, and can serve as an analogy to the behavior of crystal lattice dynamics. Additionally, similar types of structures may have future applications in the areas optical switching or force detection.

A Leica VB6 electron beam system writes arrays of varying dimensions on SOI wafers with a negative-tone resist. After a chlorine reactive ion etch removes the non-exposed portion of single crystal silicon, an isotropic buffered oxide etch releases the paddles. The arrays undergo critical point drying to prevent breakage from stiction. 50 angstroms of chromium and 200 angstroms of gold are evaporated onto the structures for conductivity.

The arrays of coupled oscillators are driven by applying an AC voltage to the structures and measuring their resonant motion with an interferometer. Translational and torsional modes have been observed and characterized. Models have been developed which qualitatively predict the observed behavior.

*Process Development for the Integration of MEMS and RF Devices*

**Liang-Yu Chen**

**Electrical Engineering, University of Hawaii at Manoa**

**Hercules Neves, Electrical Engineering, Cornell University**

We fabricate RF MEMS devices with the SCREAM (Single Crystal Reactive Etching and Metallization) process, a low-temperature bulk micromachining technology. In order to minimize the attenuation for the transmission lines used in these devices, we would like to coat the lines with very thick metal (>1  $\mu\text{m}$ ). However, we do not want to coat our other MEMS structures with such thick metal so we would like to have a method for selectively depositing an extra layer of metal on the transmission lines. Due to the large depth of the microwave structures (50-150 $\mu\text{m}$ ) conventional lithography on fabricated devices is not feasible, and we need an alternative means of patterning the metal. We have therefore developed a backside etch process (that is compatible with the normal SCREAM process) to etch holes through the wafer. Holes etched underneath the transmission lines allow for metal to be selectively deposited through the holes from the backside of the wafer.

*Vesicles as a Model System Mimicking the Myelin Membrane*

**Arrelaine Dameron**

**Chemistry, University of California, Santa Barbara**

**Jacob Israelachvili, Chemical Engineering, University of California, Santa Barbara**

It is hypothesized that Multiple Sclerosis is linked to the demyelination and subsequent vesiculation of the myelin sheath covering the nerves. The causes of this vesiculation are unknown.

Vesicles, ranging in size from hundreds of nanometers to tens of microns, were constructed from either a mixture of extracted lipids or total brain lipid extract and were prepared using hydration, and freeze-thaw/extrusion methods. These vesicles were observed for size, shape, and population density changes using microscopy, dynamic light scattering, and in some cases freeze fracture. The morphological changes were monitored while exposing the vesicles to changes in pH, temperature and ion concentration.

*The Proliferation of Streptomyces on Various Material Surfaces*

**Mia DeBarros**

**Molecular Biology, Hampton University**

**Carlo Pantano, Material Science, Pennsylvania State University**

Streptomyces sp. is a bacteria of an unknown species that is known to proliferate in the presence of a mineral called hornblende. The purpose of this experiment is to determine the role of mineral composition on the growth and attachment of Streptomyces on solid surfaces.

In the process, bacteria were grown on uncoated 7059 glass, octadecyltrichlorosilane (OTS) coated glass, chrome-coated glass, and patterned tin-oxide coated glass. After five days of incubation, the bacteria were imaged using the tapping mode on an atomic force microscope (AFM). Then they were removed from the glass using an enzyme and imaged again on the AFM. The tin-oxide, chrome, and uncoated 7059 glass were analyzed using x-ray photoelectron spectroscopy (XPS) before and after bacterial incubation. The preliminary results suggest that the bacteria do adhere to some coatings more readily than others.

*Thermionic Coolers*

**Luis Esparza**

**Electrical & Computer Engineering, University of California, Santa Barbara**

**Christopher LaBounty, Electrical & Computer Eng, University of California, Santa Barbara**

Currently cooling in photoelectric devices has been of concern for transmitting mass quantities of data. Current cooling require bulky packaging and motorized parts. By utilizing thermionic emissions, over two degrees cooling has been observed over a one-micron barrier.

### *Multilayer Conducting Beams for MEMS*

**Paul Friedberg**

Physics/Math, Williams College

**Bruce Clemens, Materials Science and Engineering, Stanford University**

The fabrication and reliability of mechanical switches in MEMS applications depends on the mechanical properties and structural integrity of conductive free-standing beams. Frequently the stresses developed during growth of the films from which the beams are fabricated leads to warping and bending, rendering the device useless. One possible method of countering this stress is the use of multilayer metal beams. By alternating layers of molybdenum and tungsten--both of which are highly conductive--we hope to tune the total stress in the film by balancing opposite stresses in the constituent layers. These balancing effects will be monitored through both in-situ stress measurements and the patterning of actual free-standing beams in the multilayer film. Eventually, the project will involve an investigation of the mechanical properties of these Mo/W beams (stress, hardness, strength, fatigue rate, etc.) and development of a more general fabrication process to grow multilayer beams of other metals.

### *Dry Etch Damage of Gallium Nitride*

**Sandra Garcia**

Chemistry, California State University, Sacramento

**Evelyn Hu, Electrical and Computer Engineering, University of California-Santa Barbara**

Gallium Nitride (GaN) is a semiconductor material that offers great potential in the development of photonic devices. In the making of these devices, the material is exposed many times to dry etch conditions that may cause damage to the lattice. In this study we use transition line model (TLM) measurements to assess the damage caused by varying doses of 500 eV of Ar<sup>+</sup> ions in GaN. Samples were ion bombarded for 15 min. with current densities of 0.006 mA/cm<sup>2</sup>, 0.06 mA/cm<sup>2</sup> and 0.6 mA/cm<sup>2</sup>. Others samples were bombarded with 0.06 mA/cm<sup>2</sup> for 7.5 min., 15 min., and 30 min. It was observed that both contact and sheet resistance increase after ion bombardment. Preliminary results show that at a current density of 0.6 mA/cm<sup>2</sup> and an exposure time of 15 min., the sheet resistance increased from 86 ohms to 184 ohms, and the contact resistance increased from 3.9 ohms to 13.6 ohms, as compared to undamaged samples. By varying the current density, bombardment time, and dose of Ar<sup>+</sup> ions, we hope to learn more about ion damage mechanisms in GaN.

*Determining the Multi-Phase Processing Window of Amorphous Silicon*

**Keith Green**

Chemical Engineering, University of Arizona

**Michael Thompson, Materials Science and Engineering, Cornell University**

The kinetics of amorphous silicon is different during a laser melt than during a thermal melt. The melting point of amorphous silicon is a function of the doping level. The melt can be shown using transient conductance measurements.

*Study of Oxidation Rates as a Function of Layer Thickness  
in high Al content AlGaAs*

**Stacie Hvise**

Engineering Physics, Cornell University

**James Harris, Electrical Engineering, Stanford University**

The oxidation of high Al content AlGaAs layers has improved the performance of many GaAs devices including heterojunction bipolar transistors (used in cell phones), stripe lasers (used in long distance fiber optics), and vertical cavity surface emitting lasers. In typical applications, the oxidized layer is used to form a current aperture that improves device performance by reducing surface recombination and increasing current density in the device active region. This is the current tunneling effect. We are measuring the oxidation rate of AlGaAs for different aluminum concentrations as a function of layer thickness (from 125Å-1000Å) and temperature (from 380C - 460C). We will then fit the data to a model for the activation energy of the oxidation reaction so we can predict the oxidation rate for new devices.

*Particle Trapping and Patterning by Optical Tweezers*

**Andrew Kearney**

Physics and Material Science, University of Pennsylvania

**Deborah Fygenon, Physics Department, University of California - Santa Barbara**

Optical trapping by a focused laser beam offers an effective way to hold and position various objects of a micron size and smaller. In our study, we used these optical "tweezers" to trap and control the motion of both neutral and biological particles suspended in solution. The trapping of neutral particles (polystyrene and silica microspheres) can be used to create ordered arrays of particles in colloid systems. The trapping of biological particles (bacteria) can be used in studies of their growth.

*Polymer Hot Embossing With Silicon Templates*

**Thomas Kenny**

Bioelectrical Engineering, Brown University

**Mary Tang and Peter Griffin, Electrical Engineering, Stanford University**

The use of polymer embossing for fabricating microscale fluidic channels presents a cost-effective way of mass-producing such devices. Such fluidic channels may be used for electrophoresis, separating biological samples such as DNA and proteins in an electric field, providing rapid medical diagnostic tests. The mechanical properties of silicon allow for numerous embossings with minimal wear. In addition, the transparent optical properties of most polymers make them ideal candidates for optical sample detection. A mask for patterning the silicon has been designed. Its features include an arrayed structure of 1" x 1" chips, allowing for several tests from a single wafer, as well as a variety of different geometries, from 150 microns down to 2 microns, in order to determine the limits of the embossing process. The silicon wafers were processed using standard photolithography techniques followed by a vertical plasma etch of the wafer, creating 90 degree sidewalls within the geometries. The effects of this type of etch on the de-embossing process will be examined. It is hoped that this research will lead to the fabrication of straight-walled microelectrophoresis channels within a polymer substrate.

*Characterization of Etches in Glass Substrates  
for Fabricating Microfluidic Devices*

**Jean Kim**

**Biochemistry, Pacific Union College**

**Mary Tang and Peter Griffin, Electrical Engineering, Stanford University**

Electrophoresis using an electric field to separate DNA fragments can be feasibly achieved on a calculator-sized chip. Using such a microfluidic device, clinical diagnoses can be reached in a more time and cost-efficient manner than through the setups currently used. In such a microdevice, DNA fragments move through channels etched into a chip. The advantages to using a glass chip include 1) transparency for visual observation of the sample's resolution and 2) insulating properties of the glass substrate allowing large separation voltages to be applied.

In glass wafer processing, the photoresist used to mask wet etches does not adhere well to glass and subsequent photoresist lifting prevents a high-quality etch. Sacrificial layers that adhere well to both glass and photoresist (e.g. Cr/Au or amorphous Si) can be used as intermediate layers. However, excessive undercut of the various layers can result in a large undercut in the final etched profile in the glass. Ideally, the etches should be anisotropic (straight-walled) and close to the original geometries designed on the mask. Using a mask consisting of varying-size channels, test structures, and angles, etch qualities and etch rates of different types of glass will be examined. SEM (scanning electron microscope) will be used to analyze the different etch profiles.

*Fabrication of Size-Variant Micropatterns for the Culture of Chondrocytes*

**Mike Kimzey**

**Pharmacology, University of California - Santa Barbara**

**Edward J. Basgall, EMPRL, Pennsylvania State University**

Chondrocytes (cartilage-producing cells) which are allowed to maintain a spherical shape during their development excrete an extracellular matrix which has uses in cartilage replacement therapies. Recent advances in nanotechnology, such as the development of microcontact printing, has created methods to fabricate Self-Assembled Monolayers (SAMs) which can confine these cells into desired shapes. Two variables will be tested, a) size of the pattern that allows optimal extracellular matrix growth, and b) spacing between the patterns which also yields optimal extracellular matrix growth. Fabrication of the micropatterns will be as follows: Electron beam writing onto a "mask plate" which has positive features of the desired pattern, a negative copy of this pattern using photolithography, pouring of a PDMS stamp onto this negative resist, peeling of the stamp and coating it with a SAM, stamping the SAM onto a gold surface, and finally "backfilling" the gold surface with a different SAM.

*Effects of Metallization on Ideality Factors of  
GaAs & 3C-SiC Schottky-Barrier Diodes*

**Nita Kohli**, Electrical Engineering and Chemistry, University of New Orleans

**John Ma**, Mechanical Engineering, University of Idaho

**Gary L. Harris**, Materials Science Research Center of Excellence, Howard University

GaAs and 3C-SiC Schottky-barrier diodes were fabricated using a variety of metals to determine their effect on the ideality factor. An insulating layer was developed which enabled us to make small-area Schottky-barrier diodes (100  $\mu\text{m}^2$ ) with large-area bonding pads without having to etch the GaAs or SiC. Ideality factors obtained on GaAs ranged from 2.13 to 3.42, and on SiC they ranged from 9.42 to 39.53.

*Fabrication of Sub-Micron Pickup Loops for SQUID Microscopy*

**Adrian Lu**

Electrical Engineering, University of Texas at Austin

**Kathryn Moler**, Applied Physics, Stanford University

Due to its sensitivity to magnetic fields, scanning Superconducting QUantum Interference Device (SQUID) microscopy has found applications ranging from medical diagnostics to imaging vortices in superconductors. SQUIDs are currently the most sensitive magnetic field detectors, but a SQUID's spatial resolution is limited by the diameter of its pickup loop. A SQUID's circuitry detects the total magnetic flux through its pickup loop. We plan to fabricate submicron pickup loops on SQUIDs manufactured by HYPRES using a design our group provided. The diameter of the final pickup loops will be between half a micron and a micron, which is almost an order of magnitude smaller than existing state of the art loops.

Electron beam lithography and reactive ion etching will be used to define the loop in a layer of niobium. Before the niobium can be etched, we must remove a layer of silicon dioxide that covers the entire chip. Currently we are investigating the etch rates of silicon dioxide in buffered oxide etch as well as etch rates of niobium in various plasma chemistries. The next step is figuring out the intricacies of electron beam lithography, including alignment to small features and linewidth optimization.

***Examination of Charging Effects in Electron Beam Lithography  
on a Leica EBPG-5HR at 50 keV***

**Ana M. Medina**

**Electrical Engineering, University of Puerto Rico, Mayagüez Campus  
Robert Davis, EMPRL, Pennsylvania State University**

Resist proximity effects, stage placement errors, and beam deflection errors can cause pattern placement errors in electron beam lithography. Of these errors, charging effects (which affect beam deflection), are very important and relatively unknown and will affect the choice of e-beam versus optical lithography for next generation (NGL) applications. Due to charging, a pattern exposed at one time by electrons can deflect the electron beam used to expose an adjacent feature.

The objective of this project is to measure and characterize charging effects in e-beam lithography using the Leica EBPG-5HR tool at Penn State. The experiments here used a Sumitomo NEB-22A negative resist (200 nm thick) coated on top of 800 nm of silicon oxide on silicon. The actual experiments consisted of a) writing a fine (400 nm lines) grating; b) writing a large solid square shape (200 mm x 200 mm) which served as a charging feature; c) waiting a certain amount of time; and finally d) writing a final grating adjacent to the initial grating. The charging effects manifested themselves as a deflection of the sets of lines written before and after the square. Deflections of the second grating lines were always away from the charging (square) feature, indicating a negative charge buildup in the square. Surprisingly, even with a 10 min wait after the writing of the square feature, the charging effect is relatively unaffected, and only after a 30 min wait is the effect reduced by approximately one half. Since the effect drops with wait time, stage drift if the EBPG tool appears to be not a prime factor in the deflections.

***Front-Side Processing for a Piezoelectric MEMS Accelerometer***

**Jami Meteer**

**Electrical Engineering, University of Notre Dame**

**Robert Davis, EMPRL, Pennsylvania State University**

Thin film piezoelectrics such as lead zirconate titanate (PZT) are promising materials for MEMS applications due to their high piezoelectric properties. This project is the development and demonstration of the front side (two mask levels) process of a new MEMS accelerometer based on cantilever beams and PZT. The starting material for the front-side process (FSP) is a silicon wafer that has silicon dioxide, lower metal electrode (Ti/Pt), and PZT films deposited. First, the top metal (Ni) electrode on the PZT is evaporated. Next, photolithography is used to define the pattern of the top metal electrode and the PZT, using three wet chemical etches. A second (aligned) photolithography step and wet etch are used to pattern the lower metal electrode.

C-V measurements of PZT pads were made to identify the quality and hysteresis characteristics of the pixels, and compared to theoretical predictions for the capacitances (the relative dielectric constant of PZT is approximately 1000). Some of the pixels were shorted, perhaps due to low quality of the films (the PZT is not deposited in cleanroom environments). Some pixels, poled at room temperature at 60 V, showed high electrical leakage. We are currently attempting to excite acoustic resonances of the underlying silicon wafer using the PZT, and also attempting to sense these resonances using the same pixels.

*Self-Assembled Monolayers as Alternative E-beam Lithography Photoresist*

**Jessica Montañez**

**Chemical Engineering, University of Puerto Rico, Mayagüez Campus**

**Carole Mars and Matt Garrett, Department of Chemistry, Pennsylvania State University**

**David Allara, Dept of Chemistry & Dept of Materials Science, Pennsylvania State University**

E-beam resists provide a way to transfer and record patterns for e-beam lithography. This project explores the use of Self-Assembled Monolayers (SAM's) as an alternative to the traditional polymer resists. SAM's are expected to counteract the tendency of etchants to undercut the polymer resist and widen the desired patterns or features.

The focus of this project is to study the effect of different etching solutions on various types of SAM/substrate combinations. Aluminum, silicon and titanium substrates with octadecanetrichlorosilane (OTS) monolayers were studied. Octadecanethiolate (ODT) monolayers on indium phosphide, gallium arsenide and gold substrates was also studied. Standard etchants known to react with the substrate were used. The influence of the etching solutions was studied by contact angle measurements. Monitoring the change in contact angle provides a way to determine how long the monolayer can prevent the etchant from reacting with the substrate. The exposure was studied over different time intervals and concentrations of etchants to maximize etching conditions.

*Nano-Structures on Polymers and Measurement of Viscous Flow*

**Renee Munoz-Verdejo**

**Mechanical Engineering, University of Puerto Rico, Mayagüez Campus**

**Jack Blakely , Materials Science and Engineering, Cornell University**

The purpose of this project is to determine the principal mode of transport of polymer molecules in producing mass flow near surfaces. The principle of the method used is the following.

The patterns are formed using e-beam lithographic and ion etching techniques. A periodic modulation of the polymer surface is produced by imprinting the grating, formed on Si, into the polymer (Polystyrene). The polymer is then subjected to several annealing treatments involving a time and temperature variation. These structures are expected to decay with time. The feature dimensions that are being used range from 0.2 micron to 1.0 micron to allow an investigation of how the decay process scales with feature dimension.

Atomic force microscopy is used to characterize and measure the rate at which the amplitude of the structures decay for each grating period. These measurements will enable us to establish which is the dominant mode of mass transport at the surface.

***Fabrication and Characterization of Copper Chalcogenide Nanoclusters***

**Brianna Norton**

**Chemistry, Bard College**

**Scott Cumberland & Geoff Strauss, Chemistry Dept, University of California-Santa Barbara**

Current research in semi-conductor materials has focused on the production of monodisperse nanocluster compounds. These compounds exhibit interesting size-dependent optical and electronic properties that could potentially be used in nanoelectronics, such as sensors and LEDs. One of the key objectives of our research is to extend the methodology to allow growth of nano-scale I-VI semiconductors, permitting the exploration of their optical and electronic properties over a distribution of sizes.

Specifically, our research involves the fabrication and characterization of copper chalcogenide nanoclusters consisting from 4 to 32 core Cu atoms. These materials are characterized by electrospray mass spectrometry and optical spectroscopy.

***Microfabricated Holder For Spatially Constrained Beads For Use In Combinatorial Libraries Analyzed By ToF SIMS***

**Yen Phuong Nguyen**

**Biochemistry & Pre-Pharmacy, University of Nebraska - Lincoln**

**Nicholas Winograd, Department of Chemistry, Pennsylvania State University**

Time of Flight Secondary Ion Mass Spectrometry (TOF-SIMS) with imaging capability has been used to directly identify compounds on polystyrene beads. The focus of the project is to look for ways to spatially constrain beads and to microfabricate structures in Si <100> that can constrain a diverse set of compounds. A fine pattern photomask was made by electron beam lithography (EBL) as a first step of this project. Subsequent photolithography was used to transfer copies of the pattern onto the surfaces of silicon wafers. Processing steps involved the following steps; RIE (Reactive Ion Etching) to remove the nitride layer, acetone to remove photoresist, and KOH etching to create pattern channels through the Si forming a sieve like bead-retaining matrix, mild backside vacuum draw the beads into the channels for subsequent analysis.

*Electron Paramagnetic Resonance and Photo Luminescence  
spectroscopy of F centers in Sodalites*

**Keith O'Doherty**

Chemistry, University of Arkansas

Vojislav I Srdanov, Chemistry Department, University of California-Santa Barbara

My project focuses on the spectroscopy of F centers in sodalites. An F center consists of unpaired electron that resides in the spherical cavity of a missing anion. Its presence can be detected by either Electron Paramagnetic Resonance (EPR) or simple optical spectroscopy. We are particularly interested in photo-luminescence (PL) of F centers in sodalites because of their potential application for laser media. If sodalite F centers show strong luminescence we may be able to create more powerful F-center lasers. This is because F centers in sodalites are more abundant than in any other ionic solid. F-centers luminescence is usually quenched at room temperature, so we will use an optical cryostat. An argon ion laser will be used for optical excitation. EPR spectra will be obtained before and after PL measurements in order to infer about F-center sensitivity to light and heat.

*Chemical Control of Surface Morphology Copper Deposition on Silicon 100*

**Vanessa Ortiz Pagan**

Mechanical Engineering, University of Puerto Rico

Melissa Hines, Physical Chemistry, Cornell University

Metal contamination has been shown to cause fatal effects on semiconductor devices, and as these are decreased in scale, ultra-large scale integrated fabrication technology (ULSI) advances and achieving and ultra-clean wafer surface is a requirement. It has been postulated that metals like copper, having higher electronegativity than silicon, can be adsorbed onto the silicon surface by the interaction of a red-ox reaction. To try to understand the mechanism of copper adhesion onto the Si(100) surface, we studied the effect of exposure time, the nature of the dopants, and illumination on the size and distribution.

***Microfabrication of Scanning Ion Conductance Microscope/Atomic Force  
Microscope Probes***

**Sean D. Pham**

**Electrical Engineering, San Jose State University**

**Ami Chand and Paul Hansma, Dept. of Physics, University of California - Santa Barbara**

In order to improve the performance of atomic force microscopy, smaller cantilever probes are required. They produce less noise and have higher resonance frequencies, thus allowing faster imaging. They also have lower spring constants so that large deflections can be obtained with small forces of interaction.

The purpose of this project is to fabricate probes for scanning ion conductance and atomic force microscopy using silicon micromachining technology. The project involves all facets of the silicon micromachining technology from mask making to the device characterization. The fabrication steps would require RCA cleaning of the silicon wafer, growth of thermal oxidation, deposition of plasma enhanced and low pressure chemical vapor deposition of silicon nitride, both conventional and backside alignment photolithography, reactive ion etching of the oxide and nitride, isotropic and anisotropic etching of silicon, and metal deposition by sputtering and thermal evaporation techniques. The project also requires inspection of the samples at various stages using optical microscopes and scanning electron microscopes.

***Coherent Control and Measurement of Single Quantum Dots***

**Martino Poggio**

**Physics, Harvard University**

**David Awschalom, Dept of Physics, University of California - Santa Barbara**

Chemically synthesized InAs and CdSe quantum dots are studied with Photoluminescence (PL), time resolved absorption spectroscopy, and low temperature time resolved Faraday rotation (TRFR). As the region of excitation shrinks from covering ensembles of dots to single dots, measurements reveal the discretized single dot energy levels and the single dot spin coherence. Schemes for controlling and detecting the spin of single dots are described. The coherent control of the spin of individual dots allows for their use as qubits in a quantum computer. In the long range, a lattice of quantum dots with local interactions could be used as one block in a quantum error correction code (QEC).

*Pulsed Laser Formation of Cobalt Disilicide*

**Karen Rantamaki**

**Engineering and Applied Sciences, California Institute of Technology**

**Bruce Clemens, Material Science and Engineering, Stanford University**

Cobalt disilicide ( $\text{CoSi}_2$ ) is a useful material in self-aligned silicide processing because of its low resistance and its silicon compatible lattice structure. Problems arise, however, when Co and Si are reacted to form the disilicide phase. High temperatures are required to do this and a good portion of the silicon substrate gets consumed in the process, causing undesirable changes in the gate junction depth. In this work, the formation of cobalt disilicide is attempted by first reacting pure cobalt with a silicon substrate to produce cobalt silicide ( $\text{CoSi}$ ). This reaction occurs at a lower temperature and consumes less Si than the formation of  $\text{CoSi}_2$ . Finally, a layer of amorphous silicon is deposited and reacted with the  $\text{CoSi}$  using a pulsed laser to form the disilicide phase. This process allows for less damage to the underlying junction structure and less consumption of the silicon substrate. X-ray diffraction will be used to determine if the  $\text{CoSi}_2$  phase is present.

*Damascene Tungsten and Poly-Silicon Structures*

**Surendra K. Ravula**

**Electrical Engineering, Duke University**

**Sandip Tiwari, Electrical Engineering, Cornell University**

We wish to develop a process that allows tungsten and polysilicon to be embedded in a silicon dioxide dielectric layer while leaving the top surface as a planar surface. Lithography was used to pattern trenches of varying width (from 20 $\mu\text{m}$  to 0.5 $\mu\text{m}$ ) and about 200 nm depth in the oxide layer by reactive-ion etching. Following removal of the resist, about 500 nm of polysilicon (using LPCVD) and tungsten (using Sputtering) was deposited in the trenches. Finally, the poly and tungsten were chemical-mechanically polished to obtain a smooth top surface.

These structures are necessary for the fabrication of transistors with raised source and drain using reverse patterning and for three-dimensional integration allowing for bonding of other materials to it.

*2-D Oxidation of SiGe*  
**Dmitriy Shneyder**

**Electrical Engineering, Virginia Commonwealth University**

**Julie Ngau, Materials Science & Engineering, Stanford University**

Silicon germanium (SiGe) is a semiconductor that offers the opportunity to implement bandgap engineering and heterojunction characteristics for improved devices such as HBTs and MODFETs within a silicon-based system. Nonplanar oxidation of SiGe must be well understood in order for this material to be successfully implemented as device dimensions are continually reduced and novel structures are invented. In our experiment, submicron SiGe pillars were fabricated and oxidized for various times and temperatures in both wet and dry ambients. The oxidized pillar profiles were characterized using transmission electron microscopy (TEM). Rutherford backscattering (RBS) was done to obtain the exact concentrations of germanium in the samples. X-ray diffraction will be used to obtain lattice parameters, which should clarify the strain of the SiGe layers. If time permits, simulations in SUPREM will be performed to compare our results of SiGe oxidation to the results predicted by material models for similar oxidations of silicon.

*Drug Delivery with Microfluidic Channels for Microelectrode Studies of Cells*

**Adam C. Siegel**

**Electrical Engineering, University of Michigan - Ann Arbor**

**Harold G. Craighead and Conrad D. James, Applied Physics, Cornell University**

In recent years a great interest in integrating biological systems with nanofabrication technologies has emerged in science and industry. A present goal of this new field is the development of nanofabricated devices to study intracellular reactions and growth. In this project, a nanofabricated biosystem for the delivery of fluid pharmaceuticals to individual cells grown on a protein pattern is proposed; such a system would be used in conjunction with an extracellular planar microelectrode system to monitor neural-cell network response in the form of altered action potential production.

Three steps of experimentation are employed for the implementation of this project: (1) the design and characterization of subsurface channels for the transport of microliter fluid samples, (2) the fabrication of a working microchip and (3) the measurement and analysis of cells grown on the fabricated devices. For the microfluidic channels, two fabrication processes incorporating a number of techniques to etch out subsurface wires in silicon were explored. In the design of a working prototype, a full three-inch wafer was used for the substrate of thirty-six axially fabricated channels connecting outer macroscopic pores to inner microscopic pores arranged in a 6x6 square grid at the center of the chip. Microcontact printing has been shown to be a reliable method of producing micrometer scale protein patterns on surfaces for cell culture. Application of a protein pattern on the surface of the device is planned to promote cell adhesion and process outgrowth in near vicinity of the microchannel openings. In upcoming weeks, rat hippocampal neurons will be grown on the surface of a prototype chip and measurements from these cells will be taken for further analysis of the characteristics of the biosystem.

***Patterning of CVD Fluorocarbon Resist Using Electron Beam Lithography and Supercritical CO<sub>2</sub> Development***

**Ruth E. Stritsman**

**Chemical Engineering, Cornell University**

**Christopher K. Ober and Gina Weibel, Material Science & Engineering, Cornell University**

The goal of the project is to pattern a fluorocarbon resist with electron beam lithography, and develop the features in supercritical CO<sub>2</sub>, as well as to characterize this procedure. Fluorocarbon polymers are not soluble in standard basic developers, so supercritical CO<sub>2</sub> was used as an environmentally benign alternative. The fluorocarbon resist was deposited using chemical vapor deposition (deposition was done at MIT Lincoln Labs), using a variety of deposition conditions. These films were then exposed with an electron beam in varying doses, and developed in supercritical CO<sub>2</sub>. This is also a precursor to using the resist with 157nm photolithography, as the electron beam lithography can be used to emulate the feature size attainable with 157nm radiation.

***A Systematic Study of Metallization Techniques Using an Image Reversal Photolithography Lift-off Process***

**Ethan Swint**

**Electrical Engineering, Baylor University**

**Garry Bordonaro and Michael Skvarla, Photolithography Engineers, Cornell University**

The process of lifting off metals is a ubiquitous research technique with a broad range of applications. However, the process has disadvantages due to the physical contours of the surface. The image reversal process was developed to circumvent these shortcomings. Despite the common use of the image reversal process, little is known of the optimal conditions for image reversal. The goal of this project is to characterize the process in order to optimize the desirable qualities of the lift-off process. A scanning electron microscope will be used to examine the physical structures after three steps in the process: development of the wafer, metallization, and the lift-off procedure itself.

*Reverse Annealing of Boron in Isochronal Anneal*

**Nam Thai**

**Electrical Engineering, San Jose State University**

**Ali Mokhberi and Reza Kanasvi, Electrical Engineering, Stanford University**

Thermal annealing is the process that occurs after the implantation step in integrated circuit fabrication. Its function is to repair damages on silicon wafers and to activate implanted impurities. There is, however, a phenomenon called "reverse annealing", in which the concentration of electrical active boron decreases as the isochronal annealing temperature increases. Reverse annealing is studied in this experiment. Boron is implanted into the silicon wafer with the energy of 40KeV and a dose of  $2 \times 10^{14}$  cm<sup>-2</sup>. A time of thirty minutes is set for different temperatures ranging from 500 to 1100 degree C in a conventional furnace to anneal the sample wafers. The expected result is that the reverse annealing will occur at the temperature range between 500 and 650. The expected result is also used to verify the set up of Hall measurement for the further study in thermal annealing.

*Wafer Bonding for Forming Microscale Fluidic Channels*

**Joseph Torralba**

**Computer Engineering, University of California at Irvine**

**Mary Tang and Peter Griffin, Electrical Engineering, Stanford University**

Electrophoresis in capillary tubes is a technique that involves using an electric field to separate fragments of biological materials, such as DNA or proteins. It has the potential to play an important role in clinical diagnostics. Because it requires specialized laboratories to analyze and interpret the data, there is an increasing interest in miniaturizing an electrophoresis laboratory into a portable device. This project approaches that goal by fabricating micro-scale capillary channels on wafers and bonding wafers together. A wafer bonding technique using an applied voltage, known as anodic bonding, is used because it allows the bonding of insulating materials at low temperatures (300 to 450 degrees Celsius). Using an Electronic Visions 501 Bonder we successfully bonded silicon to glass, glass to glass and glass to a polysilicon coated wafer. The next step is to characterize the placement of electrodes in relation to the micro-channels. Two masks were designed with varying sizes of electrodes on one and micro-channels on the other. The masks will be used to characterize how the topography created by the electrodes will influence the bonding process.

*Characterizing Lateral Solid Phase Epitaxy for 3D Device Integration*

**Joseph Valentino**

Electrical Engineering, Villanova University

**Judy Hoyt and Brian Greene, Electrical Engineering, Stanford University**

Lateral solid phase epitaxy (L-SPE) of amorphous Si (a-Si) films on SiO<sub>2</sub> is a promising technique for possible applications in three-dimensional integrated circuits. Both increased growth length from the seed region and reduction of crystalline defects are desirable material characteristics for practical device integration. Using samples prepared in a Chemical Vapor Deposition chamber and then annealed in an Argon ambient, L-SPE growth and random nucleation are studied as functions of Si film deposition rate, annealing temperature, and Ge doping. An estimate of the activation energy for the L-SPE growth rate is obtained.

*Search For Novel Open-framework Materials Using Various Copper-based Compounds*

**Serene van Gent**

Mechanical Engineering, Northern Arizona University

**A.K.Cheetham, Materials Research Laboratory, University of California - Santa Barbara**

Zeolite structures are of current scientific interest because they are very efficient as molecular sieves and ionic exchangers and in gas separation and catalytic processes. Naturally formed zeolites are aluminosilicates, and provide beneficial applications in commercial, agricultural, and environmental areas. Usages range from detergents and water softeners to petroleum cracking. Large apertures in the open frameworks of the structures are ideal, thus contributing to their absorption properties. The incorporation of other elements into the basic aluminosilicate lattice of the zeolites should add novel attributes to their functionality.

This work entails the hydrothermal synthesis of zeolite-like materials based on copper oxalates and carboxylates. Our intention has been to find novel open-framework structures that contain porous channel systems. The resulting products are then characterized by X-ray diffraction techniques providing the identification of the synthesized phases. The isolation of a single crystal would then allow us to determine the three-dimensional atomic arrangement for these phases.

*100nm Polysilicon FET Gates*

**John Vrakas**

Physics, Illinois Wesleyan University

**Richard Tiberio and Sandip Tiwari, Cornell University**

The Semiconductor Industry of America Roadmap predicts that by 2003, 100nm CMOS transistor gates will be commercially produced, pushing further the limits of size and speed posed by 250nm and 180nm gates in production today. We will demonstrate the process of 100nm polysilicon FET gate fabrication using electron beam lithography and reactive ion etching. In this process, a polysilicon-oxide-silicon gate structure is patterned using a SiO<sub>2</sub> "hard mask" layer. The structure is exposed to a minimum feature size line with electron beam lithography, followed by a two-step RIE etch process. CF<sub>4</sub> is first used to etch through the SiO<sub>2</sub> hard mask layer. A Cl<sub>2</sub> etch is then evoked to complete the gate etch with high selectivity to the SiO<sub>2</sub> gate dielectric. Gate width vs electron beam dose analysis and SEM micrographs of resist and gate cross-sections will be presented.

*Applications of Auger Electron Spectroscopy for IC Process Development,  
Failure Analysis, and Research*

**Daron Westly**

Electrical Engineering, University of South Florida

**David Spencer and Lynn Rathbun, Cornell University**

Auger electron spectroscopy (AES) is a method of surface analysis used for determining elemental composition. The purpose of my project was to explore the capabilities of AES and help in failure analysis. I will briefly discuss techniques and physics of Auger analysis and then I will give examples of analysis done during the summer.

*Electrical characterization of diffusion barrier properties for copper metallization  
in Integrated Circuits*

**Emma Wong**

**Electrical Engineering and Computer Science, Duke University  
Pawan Kapur, Electrical Engineering, Stanford University**

As feature sizes in integrated circuits continue to shrink, RC interconnect delay becomes increasingly critical. Copper, with its lower resistivity and superior resistance to electromigration, has been a major industry focus as the conductor material to replace aluminum. However, one major reliability issue with copper is its drift and diffusion in SiO<sub>2</sub> and Si. Thus, Cu plugs and interconnects must be isolated from Si or SiO<sub>2</sub> by diffusion/drift barriers to ensure that no leakage current occurs. Previous studies have been performed, characterizing different Cu barriers on one dimensional, flat MOS capacitors. The current work investigates several Cu barriers using three dimensional trench capacitors. These trench MOS capacitors facilitate the examination of possible side-wall and bottom barrier property differences. C-V curves and flat band shifts will be analyzed to determine the quality of the different barriers.

