

# Reactive Ion Etching Process Development and Characterization

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## Abstract:

Reactive Ion Etching (RIE) is a major process in the fabrication of semiconductor devices for transferring patterns from masks to semiconductor substrates. From neutral gases and glow discharge utilization, chemically reactive species are generated to react with materials being etched to form volatile by-products.

This research focuses on etching process developments for SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, GaAs, and InAs, and studies etch depth, etch rate, surface roughness, and wall angle. Approximately 1.5 μm photoresist is coated on the materials and patterned prior to etching. After etching, the samples are analyzed using a Dektak profilometer, Scanning Electron Microscope (SEM), Ellipsometer, and Atomic Force Microscope (AFM).

## Introduction:

There is increasing interest in nanotechnology and its general framework, nanofabrication; specifically in the semiconductor industry. A primary process for semiconductor nanofabrication is RIE, which uses chemical and physical processes to etch away desired materials. Compared to wet etching, RIE has higher anisotropy, better uniformity and control, and better etch selectivity [1].

This paper reports the preliminary results of RIE process developments of SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, GaAs, and InAs substrate materials. Etch depths and etch rates versus etch time have been measured. GaAs studies for surface roughness and wall angle have also been conducted.

## Experimental Procedure:

All materials are prepared using the same photolithographic process. Shipley S1813 photo resist is spin coated onto all samples, forming ~ 1.5 μm layer. Then the samples are soft baked at 110°C for 3.5 minutes. Karl Suss MJB-3 mask aligner is used to expose the samples. Shipley CD-30 developer is used to develop the photoresist. Finally, the samples are hard baked at 120°C for 10 minutes.

Table 1 shows the RIE process conditions for each material. All etches are carried out in a Nexx Cirrus-150RIE at room temperature. After etching, the photoresist is removed using an O<sub>2</sub> plasma. A Dektak profilometer is used to measure the etch depth. AFM is used to measure the surface roughness and LEO982 SEM is used to measure the wall angle.

## Process Conditions

Film	Pressure	Etching Gases	Microwave Power	RF Power
SiO <sub>2</sub>	15 mTorr	15 sccm CF <sub>4</sub>	200 W	200 W
Si <sub>3</sub> N <sub>4</sub>	10 mTorr	10 sccm Ar 15 sccm CF <sub>4</sub>	600 W	100 W
GaAs	10 mTorr	10 sccm Ar 5 sccm CH <sub>4</sub> 15 sccm H <sub>2</sub>	250 W	70 W
InAs	10 mTorr	10 sccm Ar 5 sccm CH <sub>4</sub> 15 sccm H <sub>2</sub>	250 W	70 W

Table 1: RIE process conditions (at RT).

## Results and Discussion:

For semiconductor applications, minimizing surface roughness is essential; the less surface roughness, the better the device's performance. Surface roughness is correlated with etch time: the longer etch time, the more surface roughness. Therefore, it is essential to find high etch rates to optimize device performance.

**Etch Depth versus Etch Time:** Figure 1 shows etch depths versus etch times. All points were repeated several times to ensure accuracy and repeatability. The standard deviations are low, indicating the etch processes are repeatable and consistent. All lines have a linear trend, showing that the materials' etch rates are consistent and independent of time.

Etch rate is calculated by finding the best fit slope, setting the etch depth intercept to 0. The results for calculation show that the etch rates for SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>, GaAs, and InAs are: 17.14 Å/s, 31.20 Å/s, 4.16 Å/s, and 6.67 Å/s, respectively, with R<sup>2</sup>, or correlation values, 0.9999, 0.979, 0.841, and 0.9864 respectively.

**Etch Rate:** Figure 2 shows point division calculated etch rates versus etch time. Again, the standard deviation bars are low, showing repeatability and consistency. All materials exhibit a 1/Log trend, converging to a finite number. However, due to the graph's scale, it is not easily seen for SiO<sub>2</sub>, GaAs, and InAs. The curves have a 1/Log trend because of chamber conditioning. However, Si<sub>3</sub>N<sub>4</sub> causes concern because of the much higher initial etch rate compared to its converging etch rate. Further investigations need to be conducted on Si<sub>3</sub>N<sub>4</sub>.

Point division etch rate calculations show that  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , GaAs, and InAs etch rates converge to  $17.07 \text{ \AA/s}$ ,  $31.17 \text{ \AA/s}$ ,  $4.66 \text{ \AA/s}$ , and  $6.81 \text{ \AA/s}$ , respectively. These values are within  $0.5 \text{ \AA/s}$  of their best fit slope etch rate calculations, showing consistency.

**Surface Roughness:** A preliminary GaAs surface roughness study after etch has been conducted using AFM. The etching conditions are listed in Table 1, with an etch time of 200s. The average surface roughness measured was  $1.73 \text{ \AA}$ , which is promising. Further investigations must be done to try and reproduce this result.

**Wall Angle:** Wall angle for GaAs has been investigated, though only preliminarily. Figure 3 shows a GaAs wafer SEM picture etched for 200s at the same process conditions listed in Table 1. A vertical wall is desired, however, the wall angle measured is between  $75^\circ$  and  $80^\circ$ . Further experiments need to be conducted to improve the wall angle.

### Conclusions and Future Work:

Several properties were characterized for  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , GaAs, and InAs in this project. The first was etch depth versus etch time. This showed a linear trend for all materials, with low standard deviation bars. Best fit slope calculations showed that all materials had high etch rates. The second property characterized was etch rate versus etch time. Etch rate was calculated using point division. Results showed that the materials exhibited a  $1/\text{Log}$  trend, converging to a finite number, with low standard deviation bars. The  $1/\text{Log}$  trend is due to chamber conditioning.  $\text{Si}_3\text{N}_4$  etch rate needs to be further investigated due to the higher starting etch rate value in comparison to its converging value.

Preliminary surface roughness and wall angle studies for GaAs were reported. Surface roughness was low at the process conditions studied. Further experiments need to be done to reproduce this result. Wall angle was not as vertical as desired. Process conditions need to be changed to get a vertical wall etch.

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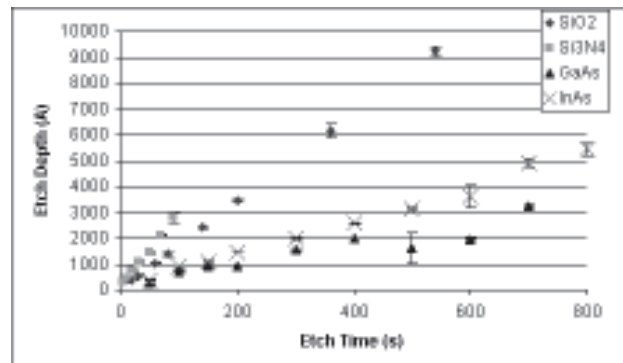


Figure 1: Etch depth versus etch time.

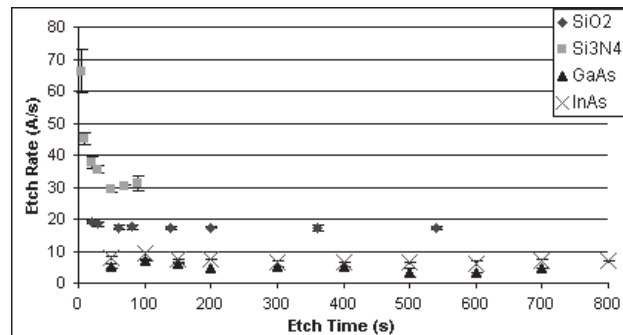


Figure 2: Etch rate versus etch time.

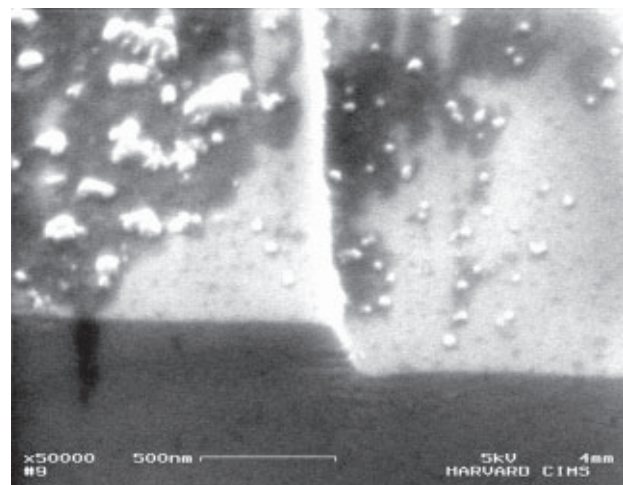


Figure 3: GaAs SEM picture.