

# Nanomechanical Structures for Digital Logic

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## Abstract:

As electromechanical systems decrease in size, researchers have become interested in scalability effects. We address these issues with regards to nanoscale electromechanical systems (NEMS) cantilevers and present potential new applications. The primary issues we explored were the following: pull-down voltage, switching speed, static power loss due to Brownian Motion, and fabrication constraints. We then explored potential applications for such NEMS such as static power reduction in transistors, ultra-low power logic gates, and zero stand-by power Static Random Access Memory (SRAM) devices.

## Introduction:

It is always useful to decrease the stand-by power of transistors. In Figure 1, as physical gate lengths continue to decrease, the dynamic power is predicted to remain relatively constant. However, the sub-threshold leakage power, (stand-by power) has become larger by comparison, and therefore more problematic. Therefore our main goal for NEMS is to decrease and eliminate this leakage stand-by power. Indeed, small cantilevers could be used to shunt the source and the drain, and when open, interrupt the flow of current.

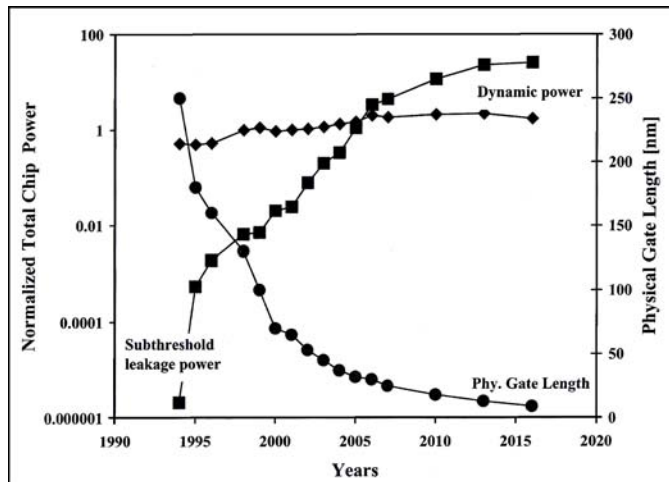


Figure 1: Stand-by and dynamic power comparison.

## Procedure

### Primary Considerations:

The primary issues with small cantilever designs are their physical size, pull-down voltage, switching speed, and Brownian motion noise. The physical size limit is dictated by our fabrication process, and modeling shows that the pull-down voltage can be held constant by appropriately scaling the relevant variables. The spring constant is the primary factor controlling both the switching speed and Brownian motion noise, and is inversely proportional to the pull-down voltage. The modeling leads us to design an acceptable compromise.

### Theoretical Findings:

Modeling the primary considerations, we are able to develop scaling constraints which can isolate and accentuate desired characteristics of the nano-scale cantilevers, or mask undesirable characteristics. Defined in terms of the minimum photolithographic feature size of any given device,  $\lambda$ , these equations can be tailored to suit its application.

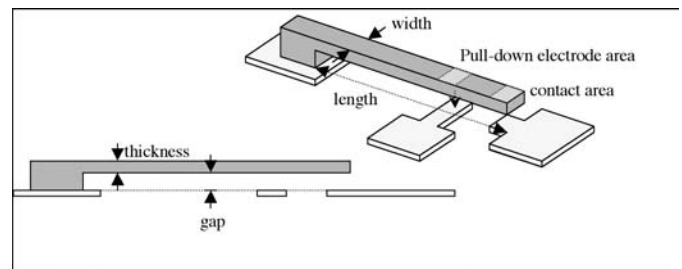


Figure 2: Physical parameters governing cantilever performance.

The physical parameters which govern the properties of the cantilever are: length, width, thickness, gap, Pull-down electrode area and Young's modulus of the material (see Figure 2 for more details).

Certain ideas to consider, however, are that electromechanical devices will always be slower than electronic devices of the same size, resulting in a lower switching speed for the given transistor. Also, the pull-down voltage must remain reasonably similar

<p><b>Pull-down Voltage:</b> <math>V_{pd} = \sqrt{\frac{8kg^3}{27A_{cap}\epsilon_0}}</math></p> <p><b>Switching Speed:</b> <math>\omega = \sqrt{\frac{k}{m}}</math></p> <p><b>Static Power Loss:</b> <math>P_{rms} = V_{dd}^2 \frac{A_{cap} \cdot \epsilon_0}{g^2} \cdot \dot{x}_{rms}</math></p>	<p><b>l:</b> length  <b>w:</b> width  <b>t:</b> thickness  <b>g:</b> gap  <b>k:</b> spring constant  <b>A<sub>cap</sub>:</b> pull-down electrode area  <b>ε<sub>0</sub>:</b> permittivity of free space  <b>V<sub>dd</sub>:</b> power supply voltage</p>
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Figure 3: Cantilever equations.

to the saturation threshold voltage of comparable conventional transistors, or else no benefit will result. The defining equations can be found in Figure 3.

### Fabrication Design:

Our proposed designs were two-fold. We first wanted to make a conventional complementary metal oxide transistor (CMOS), on top of which we would place two cantilevers. The intention was that when either the PMOS or NMOS transistor was turned on by the latching of the cantilever, the opposite transistor would be unlatched and thus eliminate power leakage. Our second proposed idea was simply to eliminate the CMOS transistor altogether and create a transistor out of simple cantilevers. This design would allow for a much simpler fabrication process, and would also create little stand-by power leakage.

## Results and Conclusions

### Theoretical Results:

For our fabrication test cases, we designed the pull-down voltages to be similar to the saturation threshold voltages according to the International Technology Roadmap for Semiconductors (ITRS). We then fitted the remaining parameters to optimize the switching speed as this was a detrimental factor we wanted to minimize. Afterwards we compared our stand-by power loss compared to the current ITRS predictions and found an almost complete order of magnitude improvement. Another advantage of these new designs is that as devices become smaller and smaller, the static power losses decrease instead of typically increase as it does in the current design.

### Experimental Results:

Our experimental results were far from successful. We were trying to make nano-scale cantilevers and ran into two major fabrication constraints: curl-up and stiction. We determined that the curl-up was caused by stressed placed on the cantilevers while releasing the cantilevers from the sacrificial layer underneath.

In Figure 4, clear examples of both curl-up (the 3 left most cantilevers) and stiction (the 2 right most cantilevers) are seen. We have ideas in how to correct such fabrication constraints but haven't had time to fabricate these improvements yet.

### Future Work:

Our future work consists of resolving fabrication complications (mainly curl-up and stiction) as well as characterizing several metals to determine optimal parameters for given applications. In order to resolve the issue of curl-up, we propose to design cantilevers with a higher spring constant. To resolve the problem of stiction, we propose to use a dimpled array of small indentations rather than a solid wall for the contact pad. This will reduce the surface area to edge ratio of the contact pad and eliminate stiction. Following the guidelines set forth in our experiments, this should not be terribly difficult to complete.

### Acknowledgements:

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### References:

- [1] Ultimate limits to inertial mass sensing based upon nanoelectromechanical systems, KL Ekinci, YT Yang, ML Roukes - Journal of Applied Physics, 2004.
- [2] Influence of automatic level control on micromechanical resonator oscillator phase noise, Seungbae Lee, Nguyen, C.T.- C. Proceedings of the 2003 IEEE International Frequency Control Symposium and PDA Exhibition., 2003, p 341-9.
- [3] MEMs relay based digital logic systems, Ezekiel J. J. Kruglick, Kristofer S. J. Pister - Transducers 1999, Sendai, Japan.
- [4] Noise: How important is it in the applications of MEMS and MOEMS? A Selvarajan - Proceedings of SPIE, 2003.

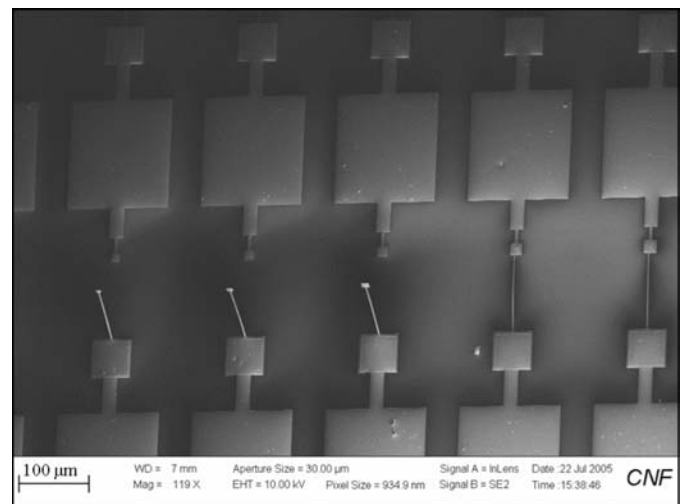


Figure 4: Curl-up and stiction.