Compositional Analysis of W and Ti Bilayer Electrodes at the Metal-Dielectric Interface and Its Effects on Work Function

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Abstract:

In this work, we characterized the metal-dielectric interface of a W/Ti bilayer electrode capacitor to determine how varying the thickness of the Ti layer between 0.5 Å and 12 Å affects the device work function. Characterization using x-ray reflectivity and x-ray photoelectron spectroscopy (XPS) indicates that thin layers of Ti form islands on the dielectric and thus are insufficient in altering the work function of the device to that of Ti. Ti layers of greater than 3 monolayers in thickness are required for continuous coverage and work function control.

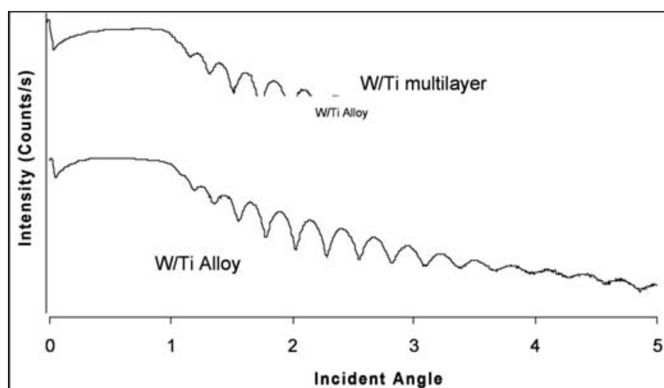

Figure 1: X-ray reflectivity scans of W/Ti multilayer and W/Ti alloy samples.

Introduction:

As nanoscale transistors decrease in size, a new material is needed to replace the polycrystalline silicon gates currently used in these metal oxide semiconductor (MOS) devices. Metals are being investigated as the proposed replacement gate material because they would eliminate the problems of dopant penetration and poly-depletion currently seen in poly-Si gates, due to their high carrier density [1]. According to theory, only a few nanometers of material in contact with the dielectric interface controls the work function of a device [2]. Previous work has demonstrated that the work function of a metal gate can thus be tuned by using a bilayer metal system and varying the thickness of the bottom metal layer [3]. Yet, the mechanism for how this works is not well understood. In order to better understand the mechanism for work function tuning, we studied a W/Ti bilayer metal gate system, with the bottom Ti layer being monolayers in thickness. This paper focuses on the materials characterization part of the project.

Device Fabrication:

MOS capacitors were fabricated using <100> p-type Si substrates, with a SiO_2 dielectric that was thermally grown at 900°C. The metal bilayers were deposited using sputter deposition for one set of samples, and e-beam evaporation for a second set. The thickness of the Ti layer ranged from 0.5 Å to 12 Å, while the W cap layer was consistently 500 Å. After patterning, all samples were subsequently annealed using forming gas ($H_2 + N_2$) at 400°C for 30 minutes.

Characterization Results and Discussions:

Figure 1 shows the low angle x-ray reflectivity scans of a W/Ti multilayer sample, and a W/Ti alloy with the same overall composition and thickness. The multilayer sample was made by sputter depositing two monolayers of Ti (4.68 Å) followed by 15 Å of W, and repeating this bilayer period 15 times. It shows a peak at the higher incident angle that is not characteristic of an alloy system. Complete intermixing between the W and Ti metals would have yielded a result that was more similar to the alloy data. Instead, we see an interruption in the W layers with a material that has a very different electron density. We are thus confident that there is minimal W/Ti intermixing in our capacitors during sputter deposition.

Type of Deposition	Expected Thickness (Å)	Calculated Thickness (Å)	Surface Percent Coverage
Sputtering	4.68	4	40%
Evaporation	4.00	10	48%
Sputtering	8.00	9	56%
Evaporation	8.00	16	60%

Figure 2: Layer thickness and Ti surface coverage of dielectric as calculated from XPS data.

Figure 2 gives the Ti percent coverage of dielectric surface as well as the measured average thickness of the thin Ti layer as calculated from XPS angle resolved measurements at 30° and 90°. The partial coverage of the surface indicates that instead of a continuous layer, there are islands of Ti metal on the dielectric. This is significant because the island morphology and surface coverage of the dielectric affects the work function of the device [4]. With the 4.68 Å sputtered Ti sample, approximately 40% of the interface is covered by Ti, resulting in the remaining 60% of the dielectric being covered by W. Such a sample should have a work function close to W, which we do indeed see with our MOS capacitors. Island growth was also studied using atomic force microscopy (AFM), and preliminary results are shown in Figure 3.

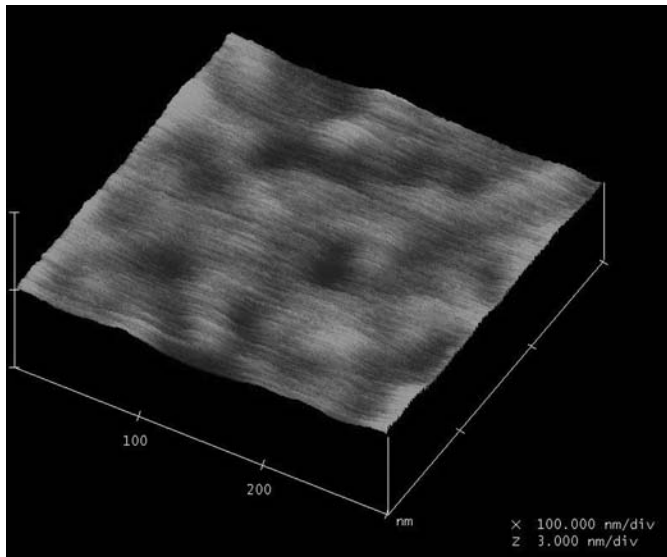

Figure 3: AFM showing metal islands on SiO_2, with 30 Å z-scale.

The discrepancy between expected and calculated thickness values (Figure 2) for the evaporation samples also illuminated the poor monitoring and control of layer thickness at such a small range using e-beam evaporation. Sputtering, on the contrary, showed a good agreement between the expected and measured thickness.

Conclusions:

Although x-ray reflectivity data shows that we can achieve distinct W/Ti interfaces, we conclude that current sputtering and e-beam evaporation techniques do not allow for the deposition of a continuous layer of such a thin Ti film on SiO_2. Furthermore, it is unclear if any deposition technique could produce non-island growth of metal monolayers. Therefore, despite theory that only a monolayer worth of material is enough to control the work function of a device, due to islanding of Ti metal, a layer thickness greater than 3 monolayers is required to form a continuous film, and control the work function of a W/Ti MOS capacitor.

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References:

[1] Y.-C. Yeo. Thin Solid Films, vol 462-63, pp. 34-41, Sept. 2004.

[2] S. Park, L. Colombo, K. Cho, and Y. Nishi. Applied Physics Letters, vol 86, no. 7, pp. 073118, February 2005.

[3] C.-H. Lu, G.M.T. Wong, M.D. Deal, W. Tsai, P.Majhi, C.O. Chui, M.R. Visokay, J.J. Chambers, L. Colombo, B.M. Clemens, and Y. Nishi. IEEE Electron Device Letter, vol 26, pp. 445-448, July 2005.

[4] I.S. Jeon, J. Lee, P. Zhao, P. Sivasubramani, T. Oh, H.J. Kim, D. Cha, J. Huang, M.J. Kim, B.E. Gnade, J. Kim, R. M. Wallace. IEDM 04, pp. 303-306, 2004.