

# Fabrication and Electrical Analysis of Metal Bilayer Electrodes for Nanodevices

Heidi Wheelwright, Physics, Utah Valley State College  
NNIN REU Site: Stanford Nanofabrication Facility, Stanford University

NNIN REU Principal Investigator: Yoshio Nishi, Electrical Engineering, Stanford University  
NNIN REU Mentor: Ching-Huang Lu, Materials Science and Engineering, Stanford University  
Contact: hjw@cc.usu.edu, nishiy@stanford.edu

## Abstract:

In this study we investigated how the work function of a W/Ti bilayer metal gate depends on the Ti thickness. The work function for each metal gate was determined by measuring the capacitance-voltage (C-V) characteristics of our metal oxide semiconductor (MOS) capacitors. We compared the work function behavior of the as-deposited and annealed samples. For the as-deposited samples, with 4.7Å (2 monolayers) of Ti and thinner, the Ti is electrically transparent. After the 400°C FGA, up to 8Å of Ti is electrically transparent and doesn't affect the work function. Islanding and diffusion have been proposed to explain this behavior.

## Introduction:

In order to continue the scaling of integrated circuits (ICs), new materials need to be introduced. Metal gates are needed in complementary metal oxide semiconductor (CMOS) technology to reduce the resistivity, depletion effects, and dopant penetration of polysilicon gates. Metal bilayer gates have been proposed to provide adjustable work functions [1]. The ability to control the work function will help optimize device performance. Previous work demonstrated how changing the bottom metal thickness could modify the work function [1,2]. However, the mechanism for this is not clear. In this paper we report on the work function behavior of a W/Ti bilayer metal gate for 12Å of Ti and thinner.

## Experimental Procedure:

We prepared bilayer metal gates of W/Ti on a SiO<sub>2</sub> dielectric. The thickness of Ti was varied from 0.25-3.5 monolayers, and the Ti was capped with 500Å of W. On some of the samples, the metal was deposited using e-beam evaporation, and on other samples by the sputtering method. The MOS capacitors were then fabricated using standard processing techniques. Characterization and electrical analysis were performed on these MOS capacitors. This paper will focus on the electrical analysis.

To investigate the electrical properties of these

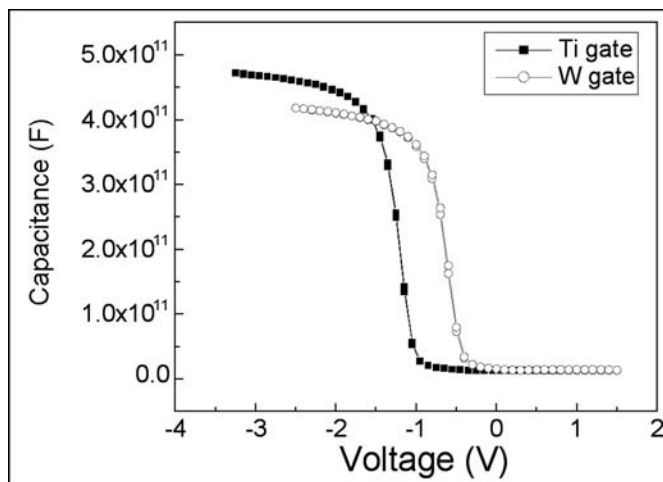


Figure 1: C-V curves of Ti and W showing a shift for different work functions.

capacitors, capacitance-voltage (C-V) measurements were performed. The C-V curves for Ti and W are shown in Figure 1. Because of the difference in the work functions, the two curves are shifted with respect to each other and thus have different flat band voltages ( $V_{fb}$ ). There is a linear relationship between the  $V_{fb}$  and the thickness of the oxide that allows for the work function of each metal gate to be calculated. For this

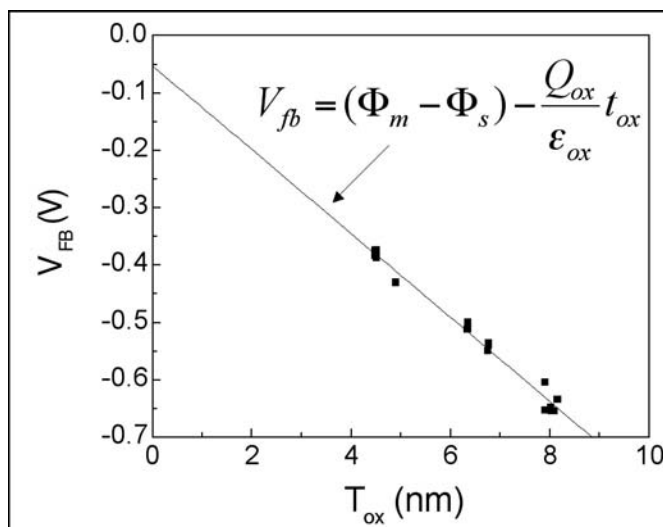


Figure 2:  $V_{fb}$  vs.  $T_{ox}$ , showing a linear relationship.

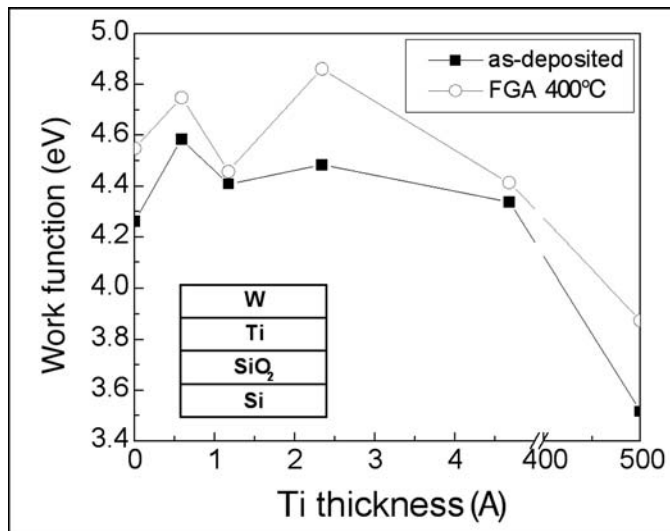


Figure 3: Work function vs. Ti thickness results from sputtered deposition samples.

reason we used four different thicknesses of oxide, 4-10 nm, for each thickness of Ti. The  $V_{fb}$  for each oxide thickness was determined using the NCSU C-V program [3]. Figure 2 shows this linear relationship and the equation that allows for the work function ( $\Phi_m$ ) to be extracted from these characteristics. Using this procedure, the work function of each metal gate was determined. A 400°C forming gas anneal (FGA) was further performed on these samples for 30 min.

### Results and Discussion:

Figure 3 presents the results for the sputtered method of metal deposition for the W/Ti/SiO<sub>2</sub> bilayer metal gate showing the relationship between the work function and the Ti thickness. The as-deposited results are compared with the results after the FGA. Before the FGA, the work functions of the thin layers of Ti are close to the work functions of W. Metal islanding has been proposed by Hung et. Al. [1] to explain this behavior. The Ti could be forming islands on the surface, in which case, some of the W is touching down onto the SiO<sub>2</sub> interface. For Ti thicknesses of 4.7Å or less, the Ti doesn't cover enough surface area to cause any change in the work function. The results after the FGA are similar.

The results for the evaporated method of metal deposition are shown in Figure 4. Ti thicknesses of 12Å and below show the dependence of the work function on the Ti thickness. Again, the as-deposited and FGA samples are compared. Notice the results from the Ti thickness of 8Å. For the as-deposited sample, the work function is in between Ti and W. After the FGA, the work function is close to W. One possible theory to explain this behavior is that the W could be diffusing

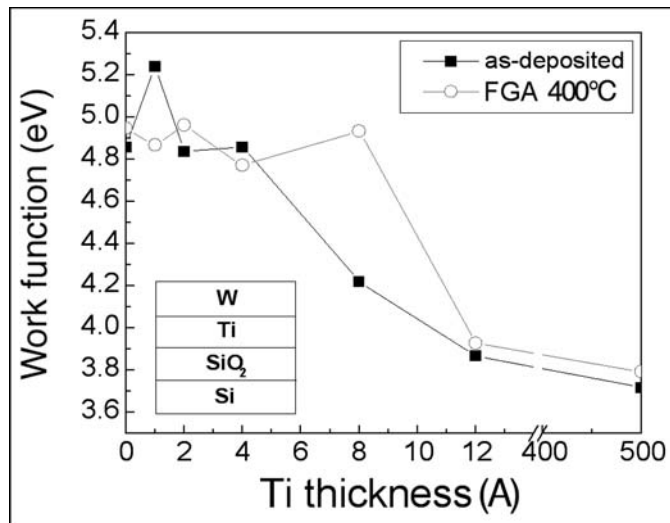


Figure 4: Work function vs. Ti thickness results from evaporated deposition samples.

down through the Ti toward the SiO<sub>2</sub> interface during the annealing process, changing the work function to W.

### Conclusions and Future Work:

Theoretically, 1 or 2 monolayers of bottom metal thickness is enough to completely determine the work function based on *ab initio* simulations [4]. In this experiment we found that 3 or 4 monolayers are needed to change the work function from one metal to the other. Metal islanding could be the cause of this observation for the as-deposited samples, and diffusion for the annealed evaporated samples. To continue researching the work function behavior of bilayer metal gates, different metal combinations will be investigated to provide more information to what determines the work function. From this, we expect to learn how to control and tune the work function of the gate.

### Acknowledgements:

I would like to thank Prof. Yoshio Nishi, Ching-Huang Lu, Dr. Michael Deal, Gloria Wong, Que-Anh Nguyen, Prof. Bruce Clemens, and Dr. Chih-Sheng Chang for their help and assistance with this research project. I would also like to thank the NNIN, CIS, and NSF for their support.

### References:

- [1] S. C.H. Hung, J. Hoyt, J. Gibbons, C.-H. Lu, M. Deal, and Y. Nishi, 2003 Semiconductor Interface Specialists Conference.
- [2] CH Lu, GMT Wong, MD Deal, W Tsai, P Majhi, CO Chui, MR Visokay, JJ Chambers, L Colombo, BM Clemens, and Y Nishi, IEEE Electron Device Lett., vol 26, pp. 445-448, July 2005.
- [3] J.R. Hauser and K. Ahmed, Proc. AIP Conf., pp. 235-239, 1998.
- [4] S. Park, L. Colombo, K. Cho, and Y. Nishi, Appl. Phys. Lett., vol. 86, no. 7, p. 073118, Feb. 2005.