Nanowire-Based Flexible Thin Film Devices

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Abstract

High-performance flexible thin film transistors (TFTs) were fabricated on plastic substrates using lightly tantalum (Ta)-doped tin dioxide (SnO_2) nanowires as the channel material. High densities of crystalline SnO_2 nanowires were dry-transferred directly onto plastic substrates, followed by lithographic patterning of resist, sputtering of chromium/gold (Cr/Au) contacts and a silicon dioxide (SiO_2) insulator layer, and a second lithography process to define a top Cr/Au gate. The top-gated TFT structures exhibit both mechanical flexibility and excellent electrical properties under cyclic tension experiments. Charge carrier mobility was estimated to be as high as 160 $cm^2/(V\bullet s)$—two orders of magnitude higher than that of conventional amorphous-silicon or organic TFTs. The low-cost nanowire growth and dry-transfer processes make this approach a cost-effective means to fabricate flexible TFT's. SnO_2 nanowire-based transparent TFT (TTFT) devices were also fabricated on glass substrates optimized for transparency using sputtered Sn doped indium tin oxide (ITO) electrodes (annealed at 200°C) and a photocured hard-baked epoxy as a gate dielectric (SU8-25 20%, MIBK; Microchem Corp.). Although highly transparent, higher contact resistance was observed for TTFT devices using ITO contacts, additional improvements to these devices need to be further explored.

Introduction

Metal oxide nanowires have attractive electrical and optical properties (i.e. high electron mobility and optical transparency) that make them ideally suited for use in high performance TFTs on low-temperature substrates. In this work, we report on the performance of lightly Ta-doped SnO_2 nanowires incorporated into flexible polyethylene terepthalate (PET) based top-gated TFTs. High density dry transfer of previously synthesized single-crystalline nanowires enables subsequent low-temperature device fabrication without sacrificing device performance [1,2]. The performance of these devices show field effect mobilities in excess of 100 $cm^2/(V\bullet s)$ and on/off ratios > 10^5 which are a marked improvement over existing conventional amorphous-silicon and organic semiconductors [3-5]. Additionally, high optical transmittance of SnO_2 nanowires suggests that TFT devices could be designed for high transparency as well as flexibility [1].

Device Fabrication

Ta-doped SnO_2 nanowires were synthesized with the method described by Dattoli et. al. [1]. After growth, nanowires were dry transferred onto the PET substrate (100 μm thick) in one direction to maximize the number of parallel nanowires (Figure 1, bottom inset). A photolithography process was used to define the Cr/Au source and drain contacts, followed by 360 nm sputter deposition of the SiO_2 gate insulator and definition of the Cr/Au gate contact. All electrical measurements were carried out in air at room temperature.

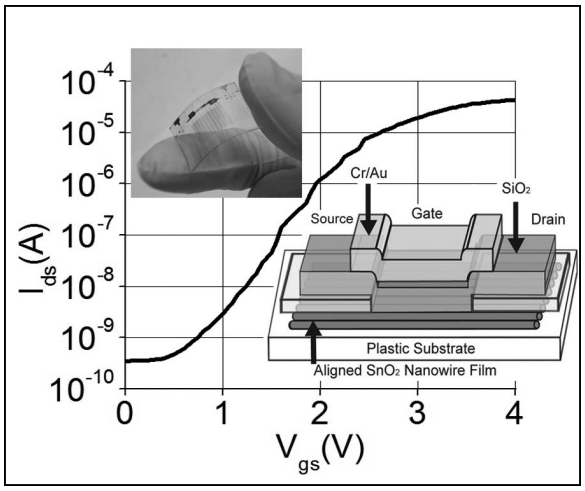

Figure 1: Logarithmic scale gate sweep characteristics of an unbent plastic TFT device shown in the upper inset. Bottom inset depicts the device architecture.

Results and Conclusions

As a result of Ta doping, the TFTs behaved like n-type enhancement-mode transistors [1]. Doping of the SnO_2 nanowires reduced the contact resistance in the TFT devices, evidenced by the ohmic behavior in the linear regime current-voltage (I_{ds}-V_{ds}) characteristics (Figure 2). Devices showed negligible gate leakage at both source and drain. The field-effect mobility, μ_{fe} ranged from 55 $cm^2/(V\bullet s)$ to 160 $cm^2/(V\bullet s)$ and coincided with mobilities measured on similar SnO_2 nanowire-based TTFTs [1]. The mobility was estimated from low-bias (1V) transconductance

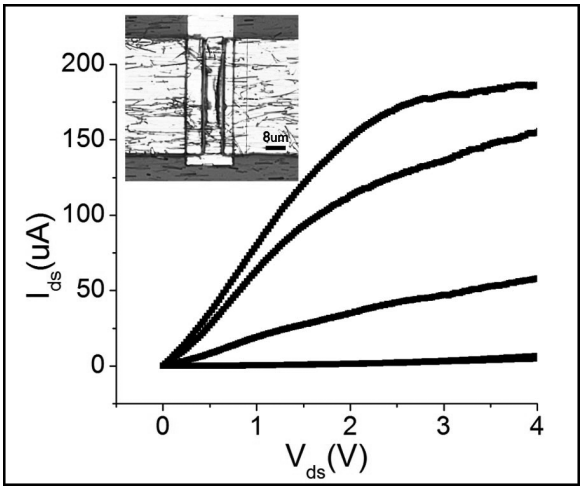

Figure 2: Voltage sweep characteristics of an unbent plastic TFT device shown in the inset.

measurements, and the capacitance of the nanowire "film" was approximated using the formula for an infinite plane ($\varepsilon_0 \bullet 3.9/t_{ox}$) [1]. An on/off ratio of > 10^5 was achieved within a 5V gate bias range with a 1V bias at the source (Figure 1). The channel length and width of this device is 8 μm and 47 μm respectively (Figure 2, inset).

The TFT radius of curvature was used to quantify the degree of compression during bending measurements. The radius of curvature was measured with ImageJ by analyzing photographs of the TFTs during compression (Figure 3). TFTs were tested before and during compression at 8 mm. The gate sweeps in Figure 3 are at a 1V source bias and show high gate mobilities above 100 $cm^2/(V \bullet s)$ for both bent and unbent conditions. This device (Figure 3, lower inset) has a channel length of 3.3 μm and width of 66 μm. At the 8 mm radius of curvature, there is a decrease in the maximum current and ~ 66% reduction in field effect mobility, μ_{fe}.

TFT devices were also tested after ten repeated compressions at curvatures from 20 mm to 4 mm. Gate sweeps at decreasing radii of curvature (Figure 4) show μ_{fe} above 100 $cm^2/(V \bullet s)$ and on/off ratios > 10^4. Like devices tested during compression, lower radii of curvatures show an 80% reduction in field effect mobility, and an order of magnitude reduction of the on/off ratio. Even after these reductions, the TFT performance characteristics in compression are still above comparable devices [3-5].

Future Work

The highest fabrication temperature was 150°C which shrank the PET substrate on the order of microns. This shrinkage encumbered alignment of subsequent mask layers. Future processing should maintain temperatures lower than 90°C to minimize plastic substrate shrinkage. Finally, highly transparent TTFT devices using ITO contacts were obtained but showed high contact resistances. Future TTFTs could have thinner SU-8 insulating layers or separate annealing of ITO to minimize sheet resistance prior to spin coating SU-8.

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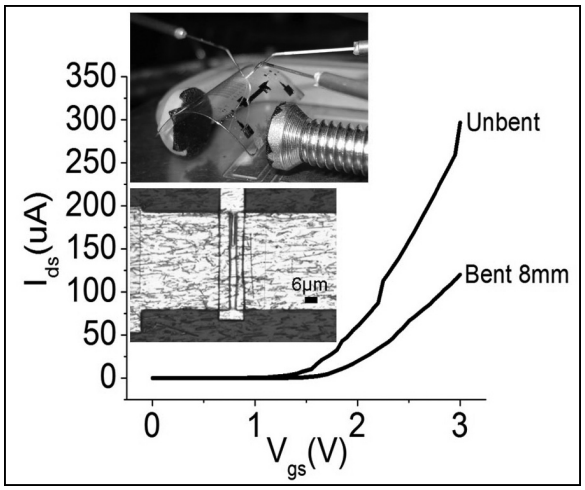

Figure 3: Gate sweep characteristics of an unbent and bent plastic TFT device (insets) taken during compression.

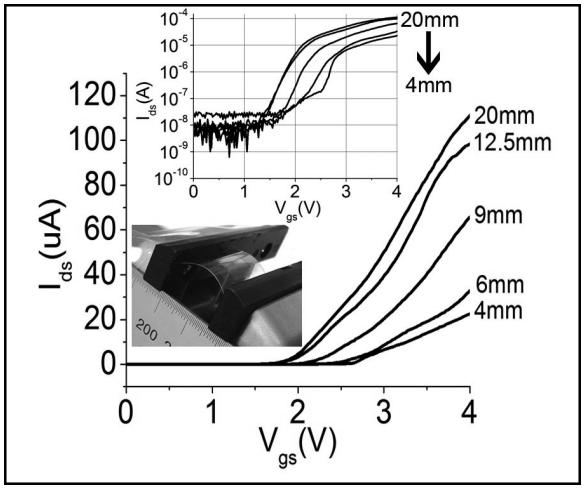

Figure 4: Gate sweep characteristics of the same plastic TFT device tested after 10 compressions of decreasing radius (20-4 mm) shown in the bottom inset. Upper inset shows log scale representation of the same data.