

# Demonstration of a Novel Fabrication Methodology to Produce Complex, Three Dimensional Structures

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## Abstract

Fabrication of high aspect-ratio three-dimensional (3D) microstructures has many important applications in modern microchip technology. A micro-electro-mechanical system (MEMS) fabrication procedure is presented that can produce high aspect-ratio 3D metal structures, which may be used for (but is in no way limited to) electronic, optical, chemical, and/or fluidic interconnection. This represents the interdisciplinary marriage of a number of highly disparate device technologies. The aforementioned MEMS structures were produced through micro-fabrication procedures, including spinning photoresist, post and pre-baking, developing, curing, electroplating, polymer decomposition, and seed layer etching. Some of the applications of the structures which were fabricated using this method include coplanar waveguides, inductors, and microfluidic filters. The primary focus of this research was to develop an enabling process technology to meet the fabrication and integration needs of generic 3D complex device structures.

## Introduction

This study was performed in an attempt to demonstrate a novel fabrication methodology for producing complex three-dimensional microstructures. Although this method extends far beyond the creation of high aspect ratio copper pillars, the most comparable previous fabrication methodology was for that purpose.

In the past, there have been many different proposed fabrication methodologies for creating high aspect ratio copper pillars. These included the copper pillar bump process [5,6] and a method involving through silicon vias [2,3,4,6] wherein the silicon is etched following copper filling of the holes (known as “vias”).

The pillar bump process involved patterning a layer of photoresist and then electroplating into the resist openings [5,6]. This method was severely limited in several ways, including the fact that it was extremely difficult to electroplate copper into high aspect ratio resist openings and it was very difficult to fabricate high aspect ratio vias in resist [6]. This process, therefore, was typically only able to achieve comparably low aspect ratios (usually, < 5.)

The other process essentially involved creating vias in a silicon wafer and then electroplating into the resultant vias [2,3,4,6]. Via creation was usually done either by etching or laser-ablation [6]. Next, an oxide layer would be deposited onto the wafer, followed by the deposition of a seed layer. The via would be filled with copper through an electroplating process. Finally, the silicon wafer would be etched away (using potassium hydroxide (KOH)) to leave behind the high aspect ratio copper pillars. There were also several problems with this process, to which several solutions were proposed. One such problem was the creation of voids during electro-deposition inside the vias due to the non-uniform current densities resulting from the local geometry of the sample. One proposed solution to this problem was the use

of an aspect ratio dependent electro-deposition process, whereby the current density was continuously varied as a function of time [3]. Moreover, it is difficult to bond the resulting pillars to the wafer containing the circuitry.

It has been well established that it is possible to create high aspect ratio polymer pillars [1,7]. These have been mainly been used in attempts to create electrical-optical I/O devices (such as micro-electro-optical-mechanical systems or MEOMS) [1,7].

During a previous REU project, sidewall metallization of polymer pillars for use as chip I/Os was investigated [7], and it was shown to be possible to create copper pillars with aspect ratios exceeding 20:1. Under that method, polymer pillars were created, and then a seed layer was deposited onto them. Once the seed layer had been created, copper was electroplated onto the side wall of the pillar. Finally, the polymer was removed through thermal decomposition. What remained was a high aspect ratio structure [7].

The method proposed here extends that previous work and uses a similar process to create structures with a more complex geometry. Some of the structures created were square spiral inductors, coplanar waveguides, an electromechanical chuck, and a microfluidic filter.

## Experimental Procedure

Two different fabrication methodologies were created, capable of creating  $\sim 50 \mu\text{m}$  and  $\sim 140 \mu\text{m}$  tall polymer pillars respectively (which would directly affect the height of the resulting structures). They differed in that the taller pillars were created by spinning two layers of polymer (Avatrel®) on the substrate surface. Herein, the sample with two layers of Avatrel shall be denoted as being produce through the “2-spin process.”

A single layer of Avatrel 2090P polymer photoresist was spun on a silicon dioxide coated silicon wafer at 600 RPM for 40 seconds (twice for the 2-spin process.) The wafer was then pre-baked for 45 minutes on a hot plate at 108°C. Then the wafer was exposed for 25 seconds in an EVG620 mask aligner (50 seconds for the 2-spin). Following the exposure, the wafer was post baked for 20 minutes at 108°C in an oven. The wafer was then developed using an Avatrel development solution. Following this development, the wafer was inserted into a PlasmaTherm reactive ion etcher (RIE) for a minimum of 3 minutes for descumming. After the descum, the wafer was cured in the Lindberg furnace at a temperature of 160°C for 2 hours. After having been cured, the wafer was metallized using the Unifilm sputterer (with 300Å of titanium, 3000Å of copper, and 300Å of titanium). This thin layer of metal acted as a seed layer for the copper electroplating which would occur later in the procedure.

A second layer of Avatrel was then spun on top of the wafer, again at 600 RPM for 40 seconds (this is done twice for the 2-spin process.) The wafer was then pre-baked once more, and then exposed using the mask aligner (for 30 seconds for the single spin process and 37 seconds for the 2-spin process). Once again, the wafer was post baked at 108°C for 20 minutes, following which the wafer was again developed. The wafer was placed into the RIE for a minimum of an additional 3 minutes. The wafer was then placed into a buffered oxide etchant (BOE) to remove the 300Å layer of titanium on its surface. The top surface of the wafer was then electroplated using a copper sulfate solution, a copper anode and the wafer as the cathode. The wafer was then thermally decomposed in the Lindberg Furnace for 2 hours at 450°C to remove the Avatrel. To remove the remaining seed layer, the wafer was placed into a copper etching solution produced from a 1:1 ratio of hydrogen peroxide and ammonium peroxide.

## Results and Conclusions

A novel fabrication methodology for producing complex, 3D structures was demonstrated to be feasible. Several different structures with various different interdisciplinary applications were constructed. In addition, process optimization has been performed. An aspect ratio of ~ 17.1:1 was achieved, as measured via images from the Hitachi scanning electron microscopy (SEM).

## Future Work

In the future, additional work can be done on building taller structures, or structures with more complex geometries. Work can also be done on providing a computational model of the various stresses, strains, and forces induced on the structures to determine the origins (and theoretical magnitudes) of the several different kinds of deformations that were observed to occur on the structures during the fabrication process.

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