

# Fabrication of Locally-Gated Bilayer Graphene Field Effect Transistors

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## Abstract:

We fabricated local backgate stacks for bilayer graphene field effect transistors. Local gates were patterned onto 290 nm silicon oxide/silicon ( $\text{SiO}_2/\text{Si}$ ) wafers using optical lithography. We etched the  $\text{SiO}_2$  layer partially by reactive ion etching (RIE), and deposited metal gate electrodes, followed by a hafnium dioxide ( $\text{HfO}_2$ ) dielectric layer. Since graphene conforms to the morphology of the substrate, a smooth  $\text{HfO}_2$  surface was critical to obtaining smooth graphene flakes.  $\text{HfO}_2$  follows the morphology of the metal and the  $\text{SiO}_2$  underneath. We explored different etching recipes to achieve a smooth  $\text{SiO}_2$  surface. Chlorine gas ( $\text{Cl}_2$ ) etched  $\text{SiO}_2$  exhibits a root mean square (rms) surface roughness of 5.1 Å. Bilayer graphene exfoliated onto  $\text{HfO}_2$  in the completed gate stacks displays a rms roughness of 5.8 Å.

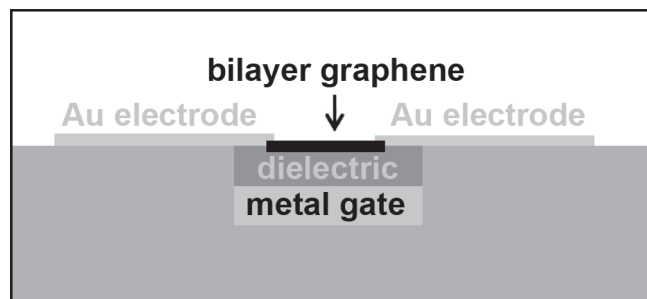


Figure 1: Gate stack diagram.

## Introduction:

Bilayer graphene, composed of two carbon monolayers in Bernal stacking, displays the unique property of having a bandgap that is tunable by electric fields. The development of local gating would enable local control of the charge carrier density and band gap in bilayer graphene as shown in Figure 1.

## Experimental Procedures:

We patterned the design for the backgate stacks with optical lithography onto 290 nm  $\text{SiO}_2/\text{Si}$  wafers. 60 nm deep wells were then etched using RIE. Early trials were run with carbon tetrafluoride ( $\text{CF}_4$ ) and later trials with chlorine gas ( $\text{Cl}_2$ ). We varied the parameters in the etching recipe to achieve a smooth  $\text{SiO}_2$  surface. The resulting  $\text{SiO}_2$  surfaces and etch depths were characterized with atomic force microscopy (AFM). We then constructed the gate stacks by depositing 5 nm titanium (Ti) / 25 nm gold (Au) using electron-beam evaporation, and subsequently 30 nm of  $\text{HfO}_2$

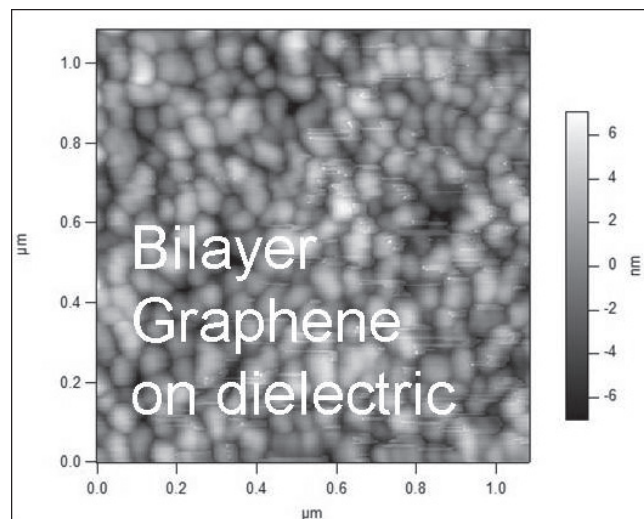


Figure 2: AFM image of bilayer graphene exfoliated on  $\text{HfO}_2$  deposited on  $\text{Au}/\text{SiO}_2$  stack. The  $\text{SiO}_2$  was etched by  $\text{CF}_4$  RIE. The rms surface roughness = 2.26 nm.

using atomic layer deposition. A lift-off procedure using acetone and sonication left only the completed gate stacks. Bilayer graphene was exfoliated onto the  $\text{HfO}_2$  surface by tape, identified by optical microscope, and characterized by AFM.

## Results and Discussions:

The bilayer graphene sheet exfoliated onto gate stacks fabricated with  $\text{CF}_4$  RIE showed a surface rms roughness of 2.26 nm as shown in Figure 2. This roughness matched the

surface roughness of the  $\text{HfO}_2$  dielectric (rms of 2.20 nm), indicating that the bilayer graphene followed the morphology of the dielectric. The roughness of the dielectric was also similar to the roughness of the Au (rms of 2.31 nm) and the  $\text{SiO}_2$  (rms of 2.08 nm) beneath it. This showed that it is crucial to produce smoothly etched  $\text{SiO}_2$  to obtain smooth bilayer graphene. The roughness of the  $\text{SiO}_2$  was insensitive to the parameters used in the recipes including temperature, gas flow and pressure.

In contrast, we were able to produce a much smoother  $\text{SiO}_2$  surface with a rms roughness of  $5.1\text{\AA}$  using a  $\text{Cl}_2$  etch. This resulted in a bilayer graphene roughness of  $5.8\text{\AA}$  as shown in Figure 3.

The  $\text{Cl}_2$  etch showed time-dependent etch rates which were much slower than the  $\text{CF}_4$  etch. In several different trials, the etch rate dropped considerably within the first five minutes before leveling off to a constant  $1.7\text{ nm/min}$  (see Figure 4).

Care should be taken when using  $\text{Cl}_2$  etch since long etches may cause heating issues with the photoresist.

### Conclusions:

To conclude, we studied the etching of  $\text{SiO}_2$  by  $\text{CF}_4$  and  $\text{Cl}_2$ . A smooth surface of  $\text{SiO}_2$  (rms  $\sim 5\text{\AA}$ ) is achieved by  $\text{Cl}_2$  etch. We successfully deposited metal gates and  $\text{HfO}_2$  dielectric layers, and performed lift-off to create local back gates. Bilayer graphene exfoliated onto these local gates showed a rms roughness of  $6\text{\AA}$ , similar to that of the etched  $\text{SiO}_2$ .

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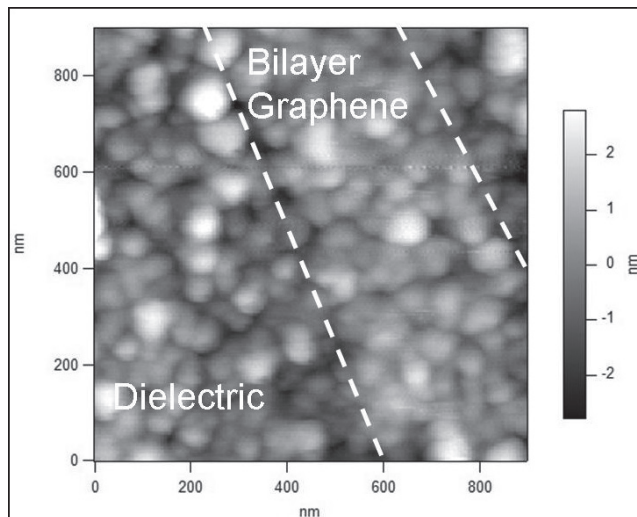


Figure 3: AFM image of bilayer graphene exfoliated on  $\text{HfO}_2$  deposited on  $\text{Au/SiO}_2$  stack. The  $\text{SiO}_2$  is etched by  $\text{Cl}_2$  RIE. The rms surface roughness =  $5.8\text{\AA}$ .

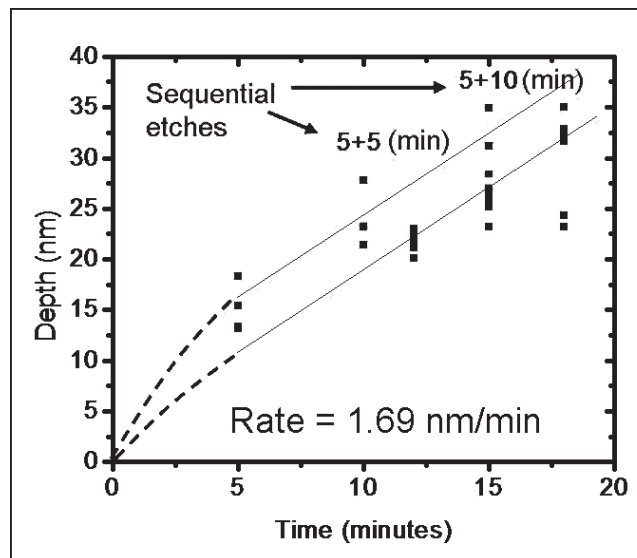


Figure 4:  $\text{Cl}_2$  etch rates.