

# Graphene Contacts to Pentacene Thin-Film Transistors

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## Introduction:

Organic thin-film transistors (OTFTs) have attracted significant interest in recent years as their performance approaches that of traditional amorphous and polycrystalline silicon electronics. OTFTs are especially promising for large-area, flexible, and low-cost circuits, such as organic light-emitting diode displays and RFID tags. Despite recent improvements, however, traditional gold (Au)-contact OTFTs still suffer from somewhat poor performance, in part because of their large contact resistance.

We propose single-layer graphene as a novel contact material for pentacene-based OTFTs. Graphene's 2D hexagonal lattice and pentacene's linked benzene ring structure are remarkably similar, motivating a belief in improved electrical contact. Additionally, atomically thin and flat graphene allows uninterrupted contact to the pentacene active region, facilitating improved performance. Despite this potential, graphene remains almost entirely unexplored in this application.

## Methods I:

We began with a 285 nm thermal oxide on a highly doped silicon wafer, on which we deposited a 495 nm copper (Cu) film with a 5 nm nickel adhesion layer. We then grew

graphene on the Cu film via CVD in a low-pressure methane and hydrogen atmosphere at 1000°C, as has been described elsewhere [1]. This created a uniform, low-defect single layer of graphene, as confirmed by Raman spectroscopy (Figure 1) [2]. Graphene was patterned with standard contact lithography and an oxygen plasma reactive ion etch. A dilute ferric chloride / hydrochloric acid solution removed exposed Cu and under-etched graphene, leaving a  $\sim 10 \mu\text{m}$  lip of graphene resting directly on the gate oxide. After drying in a vacuum oven to adhere the graphene to the oxide surface, remaining photoresist was vigorously stripped in acetone.

As a standard of comparison for the graphene devices, we also fabricated identical gold electrodes (45 nm gold with a 5 nm chromium adhesion layer) via evaporation and lift off on a wafer with the same thermal oxide.

Because pentacene is incompatible with standard lithographic processes, we first patterned windows in a second layer of photoresist and then thermally evaporated 50 nm of pentacene in a dry nitrogen glovebox, leaving the photoresist as a permanent part of the device (Figure 2). An HMDS vapor treatment was applied just prior to pentacene deposition to improve growth behavior and the quality of the final film. The highly doped silicon wafer serves as a back-gate electrode. Finished devices were stored in a glove box and analyzed under vacuum to avoid atmospheric degradation of the pentacene layer.

## Results and Discussion I:

Electrical measurements for these devices were less than ideal. Graphene devices showed mobility several orders

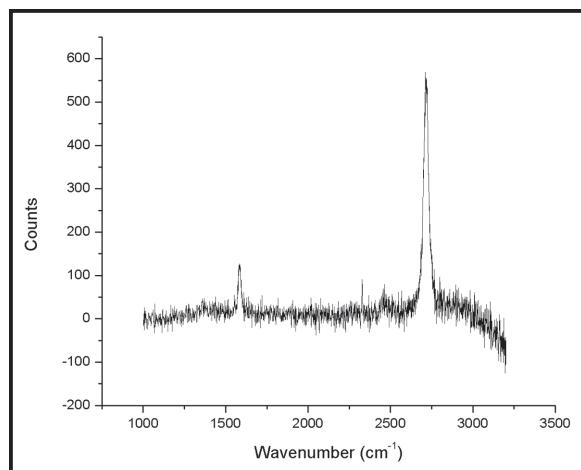


Figure 1: Graphene Raman spectrum.

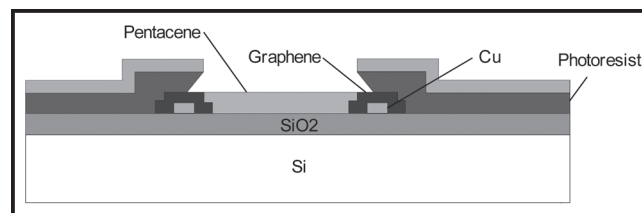


Figure 2: Device cross-section.

of magnitude lower than published gold devices, and had a negative contact resistance when analyzed by standard methods [3]. Scanning electron and atomic force microscopy (SEM and AFM) revealed an uneven and ridged graphene edge, and we hypothesized that iron compounds from the copper etch built up at the edge and affected behavior of the pentacene layer. Additionally, iron is a known dopant for pentacene; contamination at the contacts and dopant-induced channel-length shortening perhaps explain deviation in behavior from the standard contact resistance model.

## Methods II:

To circumvent this problem, we fabricated identical devices using a graphene transfer process. Here, we grew graphene on a copper foil, spun on a thin layer of PMMA (2% in anisole), and etched away the copper foil entirely, leaving the PMMA-coated graphene floating in the etch solution. We then transferred well-rinsed graphene onto an oxide-coated wafer, removed the PMMA in acetone, and continued fabrication as before.

## Results and Discussion II:

The electrical performance of these transferred graphene devices was approximately one hundred times better than under-etched transistors, with mobility and contact resistance comparable to published gold-contact transistors. Significantly, mobility did not substantially decrease with shorter channel length, unlike most published OTFT designs.

To examine the physical causes of this performance, we deposited only 5 nm of pentacene, equivalent to approximately 2.5 monolayers, on both graphene and gold devices. We then examined the deposition with an SEM (Figure 3). While overall nucleation was similar on both devices, pentacene grains grew across the edge of the graphene / silicon dioxide interface, while nucleation predominantly stopped at the edge of the gold electrodes. We believe this was primarily caused by the difference in thickness between the two materials (approximately 1 nm for graphene versus 50 nm for gold). Pentacene films only conduct in an approximately 3 nm thick active layer [4]; the thin graphene not only contacted this layer more directly, but also did not disrupt it with a large height step at the electrode edge (Figure 4).

The full depositions of pentacene on Au electrodes, however, were not as successful. The Au-based devices did not conduct significant current regardless of applied gate voltage. Electrically probing various parts of the device pointed to a problem at the gold/pentacene interface.

This bad contact could have perhaps been caused by trace organic contamination of the gold from photoresist residue or other factors. It is possible that the graphene contacts were less sensitive to similar contamination because of the purely organic interface. Simply cleaning the gold surface was difficult because of gold's tendency to sputter off in a reactive ion etch and the need to preserve the permanent layer of photoresist.

Going forward, we hope to further investigate the Au surface chemistry and various cleaning methods to fabricate working gold electrodes and complete the device comparison.

## Acknowledgements:

We gratefully acknowledge support from the National Science Foundation, the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, and the Cornell NanoScale Science and Technology Facility. I especially thank Dr. Jiwoong Park, Adam Wei Tsen, and other members of the Park group; Rob Ilic and Melanie-Claire Mallison, CNF REU Program Coordinators; and CNF Staff.

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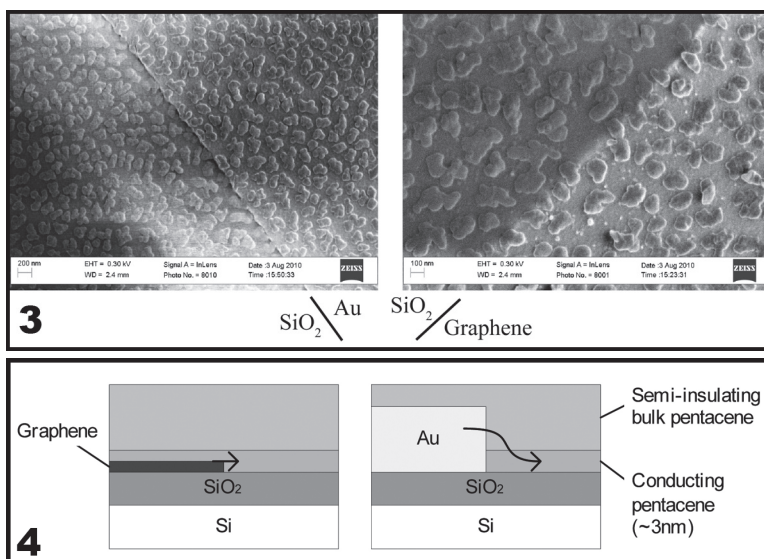


Figure 3: Partial deposition SEM.

Figure 4: Pentacene active layer cross-section.