Characterization of High Aspect Ratio Silver Micromachining for Radio Frequency Inductors

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Abstract:

This paper fully characterizes silver (Ag) electroplating and polishing processes for the implementation of low-loss integrated inductors. Silver was the chosen conductor material as it exhibits the highest electrical conductivity of all metals. Electroplating deposits a thick metal layer from a metal anode on a substrate by passing an electrical current between them. Depending on the type of electric current, the electroplating process can be classified into three categories: direct current (DC), pulse, and pulse-reverse (PR). PR electroplating offers the best surface profile and uniformity by decreasing the porosity of the electroplated regions. Therefore, in this study, we characterized silver PR electroplating and compared the results with DC electroplating. To reduce the surface roughness and further increase the uniformity, we utilized a silver polishing process and achieved a surface uniformity of better than 0.13 μm. The same electroplating and polishing methods can be used with higher aspect ratio silicon molds enabling fast, smooth, and uniform deposition of silver.

Introduction:

Silicon technologies are becoming more desirable for wireless communication applications as they offer low-cost and high performance systems. In lumped radio frequency (RF) filters, high quality factor (Q) inductors and capacitors are needed for reduced insertion loss. Two loss mechanisms affect the inductor Q: the metal loss and the substrate loss [1]. The metal loss dominates at low frequencies while the substrate loss determines the Q at higher frequencies. To reduce the metal loss, several approaches have been taken including depositing thick layers of high conductivity metals and shaping the inductor geometry.

In this project, we electroplated thick Ag layers to decrease the metal loss. Furthermore, we used coplanar structures with a distant ground to alleviate any uneven distribution of the current flow [1]. Since the current flows on the outer most surface of the conductor, the surface roughness plays an important role in determining the metal loss.

We optimized the deposition and polishing processes of inductors to obtain smooth surfaces and high Q values. We optimized the electroplating conditions using PR electroplating, which offered good uniformity and reduced surface roughness. We polished the silver layer to further smooth out the surface. When comparing DC with PR plus polishing samples, the inductor Q improved by 20% at low frequencies where the metal loss is dominant.

Feature Size	DC Height (µm)	PR Height (µm)
200 µm	7.52 ± 0.22	9.34 ± 0.31
20 µm	8.24 ± 0.19	9.58 ± 0.21
Overall Uniformity	8.00 ± 0.40	9.49 ± 0.27

Figure (Table) 1: Comparing DC and PR electroplating overall surface uniformity and deposition rate.

Experimental Methods:

The fabrication process started with sputtering the seed layer (100Å Ti/ 500Å Ag/100Å Ti) onto the passivated silicon wafer. Then negative resist NR-4 was spin-coated and patterned to form the electroplating mold.

Once a plasma process removed the top titanium (Ti) layer, the photoresist mold was ready for Ag electroplating. With an Ag anode positioned parallel to the silicon wafer cathode in a cyanide solution, an electrical current was induced into the system, and the Ag cations were redeposited onto the Ag seed layer.

The plating rate depended on the open areas on the photoresist. After over-electroplating 0.5-1 μm, we polished the

wafer to remove the excess Ag and obtain uniform thickness of Ag on the wafer. Finally, the Si substrate was selectively removed to reduce the substrate loss.

Results and Conclusions:

The forward and reverse current bias and duration were varied to find the optimum electroplating conditions. The optimal PR electroplating occurred with an effective current density of 5 mA/cm^2. The respective forward and reverse current amplitude was 60 mA for 17 ms and 180 mA for 1 ms, with a pulse off time of 1 ms.

Table 1 compares the electroplating rate and uniformity using the optimum PR conditions with those of DC plating. The measurements recorded in Table 1 were from two extreme mask widths, 20 μm and 200 μm. Comparing the data in Table 1 and the surface profiles in Figure 2, we observe two distinct differences: 1) across a 4″ wafer, the electroplated Ag thickness in the DC sample varied up to 1.24 μm, while the variance was only 0.35 μm on the PR sample; 2) PR plating deposited 16% faster than the DC electroplating wafer. Therefore, under the optimal conditions, the PR electroplating sample had an improved overall surface uniformity and a faster deposition rate than the DC plating sample.

To further improve the surface roughness and therefore the inductor Q, we polished both samples. The polishing process incorporated a 0.3 μm aluminum oxide slurry and a 8:1:1 volume ratio solution with distilled water, hydrogen peroxide (H_2O_2) and ammonium hydroxide, respectively. We achieved a 0.13 μm surface roughness for both samples (Figure 3). The surface roughness (0.13 μm) was lower than the size of aluminum oxide slurry (0.3 μm) as the additional solution aided the polishing process by wet removal of silver: the hydrogen peroxide oxidized the silver layer, and the ammonium hydroxide removed silver oxide.

When quantifying the Q, we tested four samples: DC electroplating, DC plus polishing, PR electroplating and PR plus polishing. At 200 MHz, there was a 20% Q improvement between the DC plating and PR electroplating plus polishing samples (Figure 4).

Scanning electron microscopy images of the inductors in Figure 4 illustrates the extreme porosity in DC plating and the varying surface grain size between the two samples: 1.24 μm in the DC sample and 0.13 μm in the PR plus polishing sample.

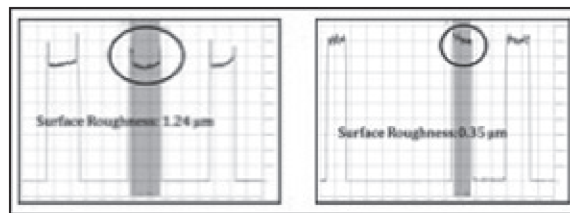

Figure 2: Showing the surface profiles of the PR and DC sample.

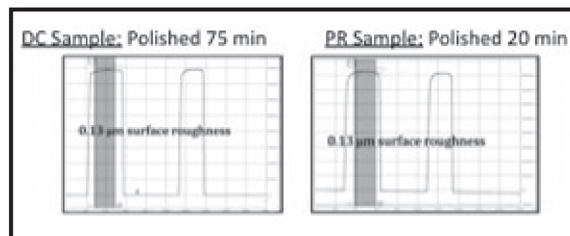

Figure 3: Achieving a 0.13 µm surface roughness using a 0.3 µm slurry, H_2O_2, and ammonium hydroxide.

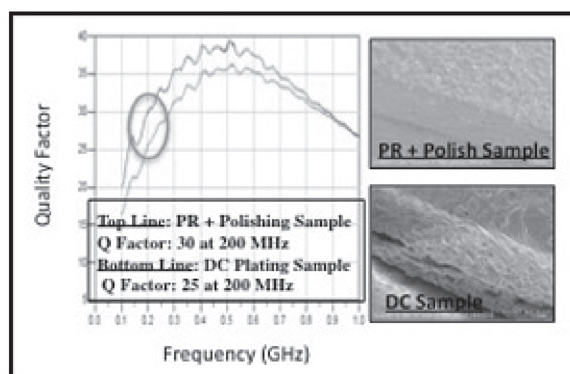

Figure 4: Q is improved by 20% in PR + Polish sample. This is due to improvement of surface roughness.

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References:

[1] Rais-Zadeh, Mina; “High-Q integrated inductors on trenched Si islands,” Master thesis, Department of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA, 2005.