Heterogeneous Integration of p- and n- type Nanowires for Complementary Nanowire Circuits

NNIN Grad Program

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Abstract:

Semiconductor nanowires are of considerable interest as an advanced building block for the next generation nanodevices because of their promising and fascinating properties. For successful implementation in wide variety of applications, however, the ability to tightly define the diameter of the semiconductor nanowires is becoming indispensable because their fundamental properties are strongly dependent on the radial dimension. Therefore, there have been increasing demands for the development of new efficient methods that precisely control the nanowire geometries for more practical applications. We report growth of diameter-controlled tin oxide (SnO_2) nanowires by vapor-liquid-solid (VLS) process via boiled aluminum oxide/silicon (Al_2O_3/Si) substrate for develop of a heterogeneous integration technique to build complementary circuits based positive and negative type nanowires.

Introduction:

SnO_2 nanowires were chosen in our studies due to the low growth cost, high optical transmittance. Particularly, single-crystalline SnO_2 nanowires may be grown using a simple vapor transport synthesis method that allows for the growth of large quantities of nanowires at a low cost. We have developed a reliable *in situ* doping process that has been shown to dramatically affect the nanowires' electrical properties in a controlled fashion. In previous work, we focused on lightly tantalum (Ta)-doped SnO_2 nanowires that serve as the channel material in nanowire field-effect transistor and transparent thin-film transistor devices [1]. The Ta-doped SnO_2 nanowires were synthesized on Si substrates by a catalyst-mediated VLS process in which the Ta and Sn source materials were provided by a vapor transport method. In this work, we grew diameter-controlled SnO_2 nanowires by VLS process via boiled Al_2O_3/Si substrate.

Experimental Procedure:

The first step was to create a substrate. First, a Al_2O_3 film was deposited on bare Si surfaces by evaporator (80 nm). The Al_2O_3/Si was boiled in deionization water at 95°C (by thermometer) in Pyrex® beaker on a hot plate around 300°C. The boiled Al_2O_3/Si was cleaned up by oxygen plasma cleaning for 30 seconds at 150 W. Poly-lysine solution was coated on the Al_2O_3/Si for five minutes and rinsed with deionization water. Poly-l lysine functionalization of the Al_2O_3/Si surface was utilized in order to promote gold (Au) nanoparticle adhesion. 20 nm Au nanoparticle colloid solution procured was coated on the surface for five minutes and rinsed with deionization water. The boiled Al_2O_3/Si with 20 nm Au nanoparticle was used as the growth substrate.

The second step was to grow SnO_2 nanowires via VLS process. First, Argon gas flowed, acting as the carrier gas of 0.55 SCFH, which was made to flow through a tube using metered flows and at atmospheric pressure. The growth process proceeded as follows. The source material, consisting of a mixture of Sn and Ta powder and the boiled Al_2O_3/Si growth substrate, was loaded into a separate quartz tube that had a diameter of 1.0 cm and a length of 10.1 cm. The ratio of mixture of Sn and Ta was 500/1 and the amount of mixture was 0.5 g. The distance between the source and the growth substrate was 3 cm. The temperature ramp rates were fixed at 20°C/min, the tube furnace was allowed to heat up to 900°C and was held there at 900°C. Once the furnace temperature reached 900°C, the furnace was opened and the quartz boat was pushed into the center of the furnace using a stainless steel rod while the furnace was still at the process temperature. After heating at 900°C for 15 min, the quartz boat was unloaded from the furnace.

Results and Conclusion:

Following growth, SEM imaging of the growth substrate showed diameter-controlled VLS SnO_2 nanowire growth (Figure 1). The images show ~ 30 nm diameter SnO_2 nanowires growing from 20 nm Au nanoparticles.

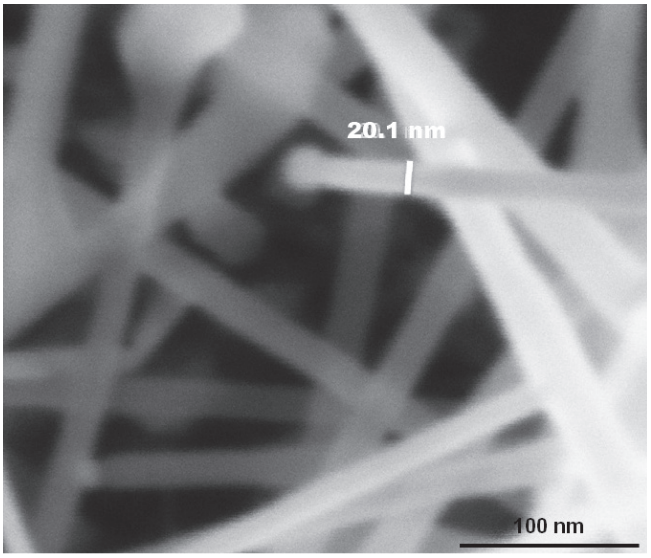

Figure 1: SEM image of SnO_2 nanowires.

It can be clearly seen that there is a catalyst at the tip of the nanowires. In addition, a spherical Au nanoparticle was observed at the end of each as grown nanowire, which is a common characteristic of the nanoparticle nucleated VLS nanowire growth process. This was due to pores of boiled Al_2O_3 that can fix nanoparticles.

We demonstrated the effect of pores of boiled Al_2O_3 by heating 20 nm Au nanoparticles on Si substrate, 20 nm Au nanoparticles on boiled Al_2O_3/Si substrate in the same condition, except for a source. SEM imaging after heating 20 nm Au nanoparticles on a Si substrate showed the agglomeration of 20 nm Au particles (Figure 2), whereas SEM imaging after heating 20 nm Au nanoparticles on a boiled Al_2O_3/Si substrate showed no agglomeration of 20 nm Au particles (Figure 3). This result indicates that pores of boiled Al_2O_3 can prevent agglomeration of Au particles.

In conclusion, we reported a simple and effective method for fabrication of semiconductor nanowires. The boiled Al_2O_3/Si substrate enables control of the agglomeration of nanoparticle catalysts, and thereby, the diameter of semiconductor nanowires can be manipulated depending on the catalyst size in the VLS growth process.

Future Works:

Diameter-dependent electrical properties of the controlled SnO_2 nanowires will be explicitly embodied by the application to nanowire field effect transistors. The ability to control a well-defined radial dimension of the semiconductor nanowires could facilitate implementation of integration of nanowires for complementary nanowire circuit.

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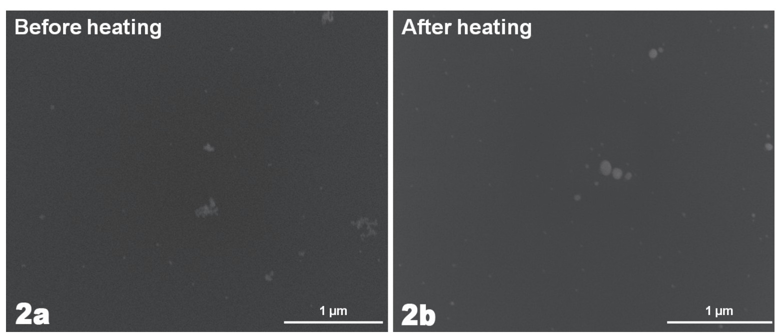
References:

[1] Wei Lu et al., Nano Lett., 2007, 7, 2463-2469.



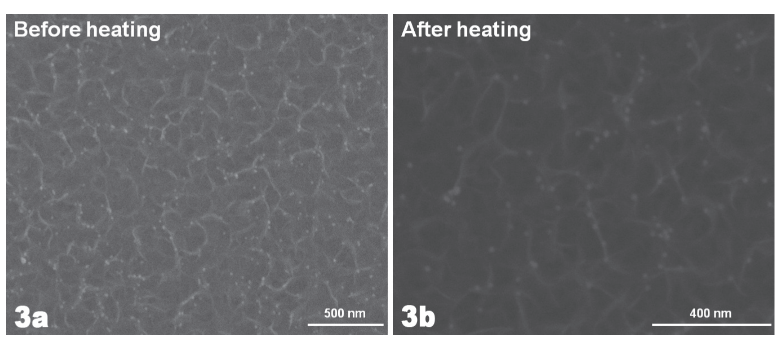


Figure 2, top: SEM images of Au particles on Si substrate.

Figure 3, bottom: SEM images of Au particles on boiled Al_2O_3/Si substrate.