

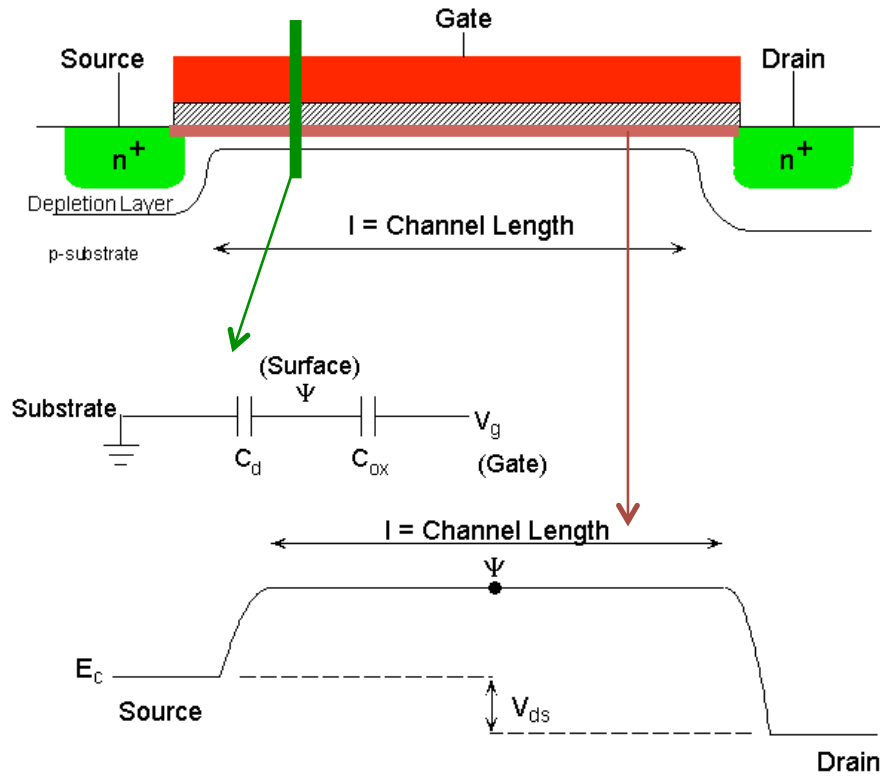
Non-volatile and Volatile Memories

Prof. Paul Hasler

Georgia Institute of Technology



MOS Transistor Derivation

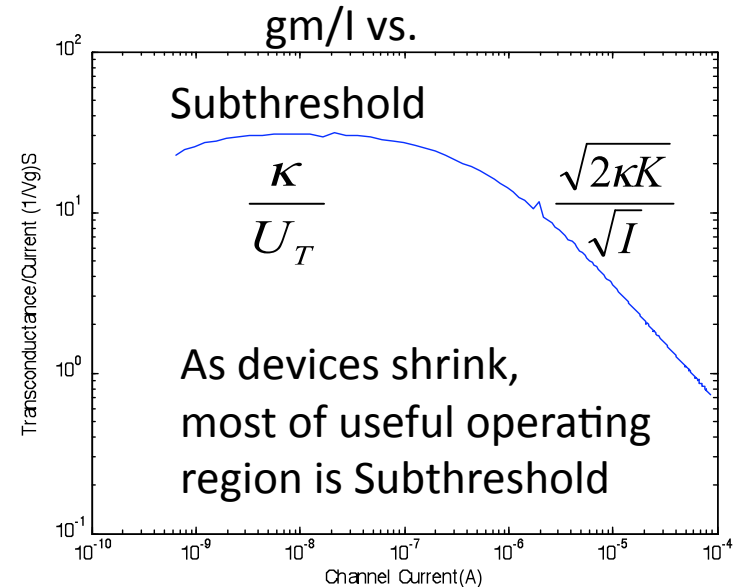
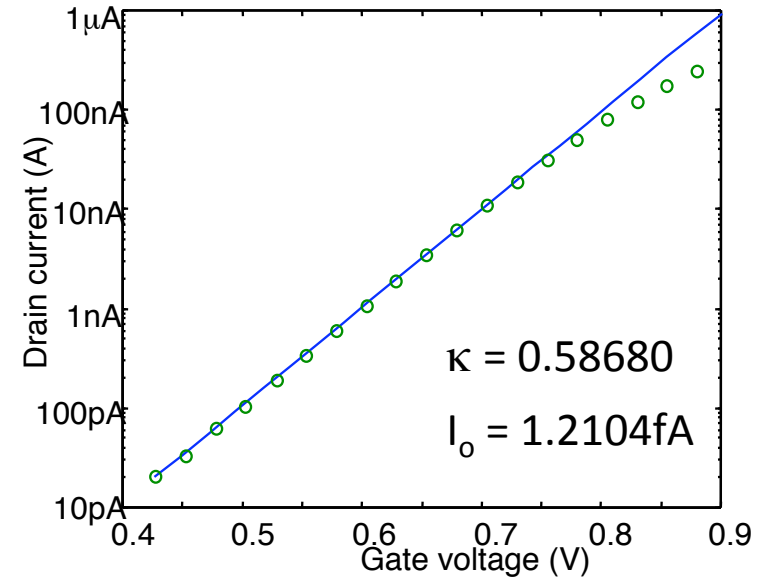


$$I_{ds} = I_0 e^{kV_g/U_T} (e^{-V_s/U_T} - e^{-V_d/U_T})$$

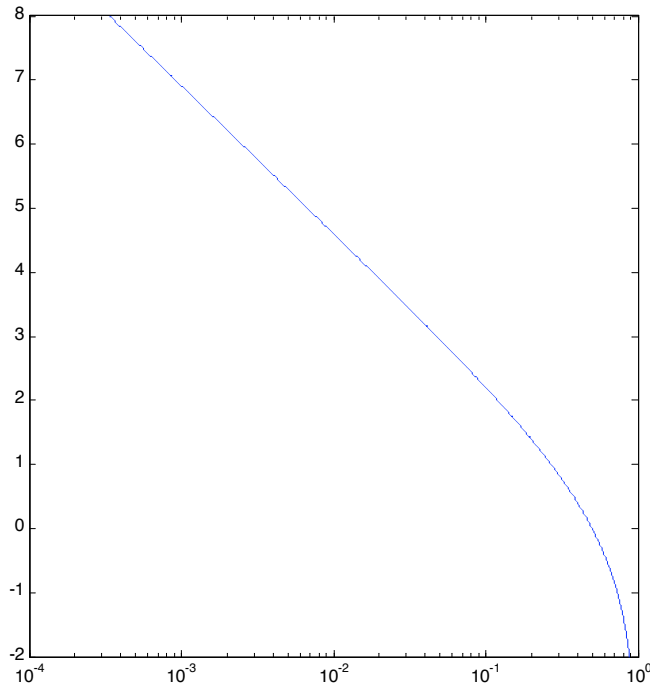
$$= I_0 e^{(kV_g - V_s)/U_T} \quad (V_{ds} > 4 U_T) \quad U_T = \frac{kT}{q}$$

"Saturation"

Mismatch is significant: 10mV V_T shift
 $\sim 50\%$ bias current variation

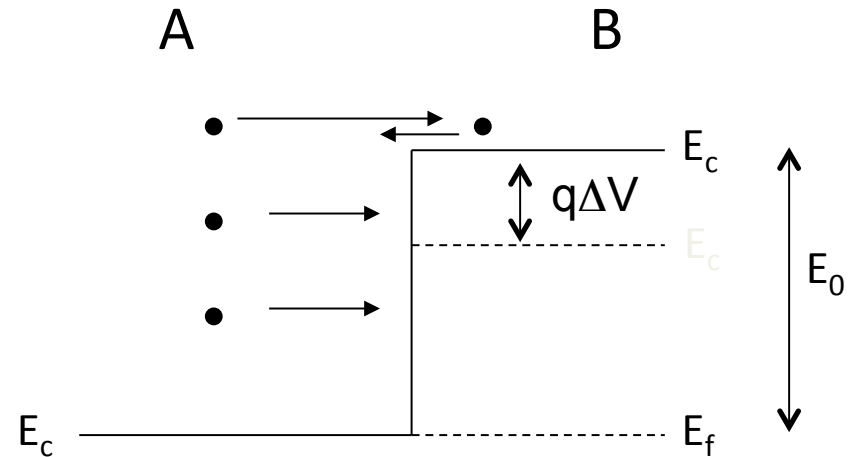


Diffusion of Charge over Barrier



$$P(E) = \frac{1}{1 + e^{-(E-E_f)/kT}}$$

$$\sim e^{-(E-E_f)/kT}$$



Case I: $P(E) \sim \exp(-E_0/kT)$

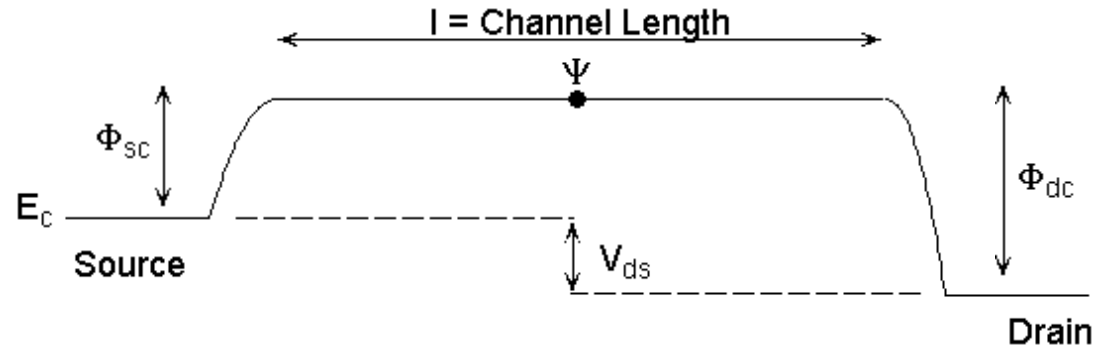
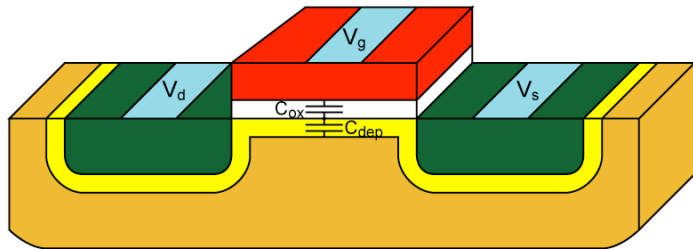
Case II: $P(E) \sim \exp(-(E_0 - q\Delta V)/kT)$

Ratio of Case II to Case I = $\exp(\Delta V / U_T)$

$$U_T = kT/q$$



Calculation of Drain Current



No recombination

$$\frac{dn}{dt} = D_n \frac{d^2 \Delta n}{dx^2} + G - R$$

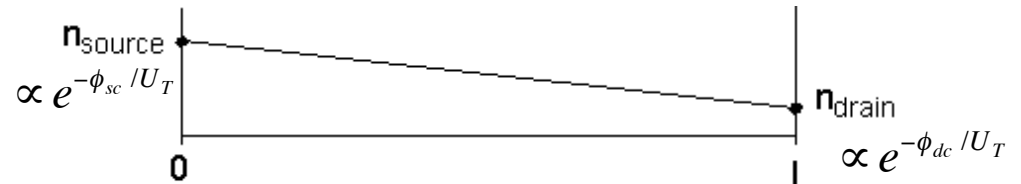
$$D_n \frac{d^2 n}{dx^2} = 0$$

$$\Delta n = Ax + B$$

$$\Phi_{sc} = V_s - \Psi$$

$$\Phi_{dc} = V_d - \Psi$$

ψ varies as κV_G $\kappa = \frac{C_{ox}}{C_{ox} + C_{dep}}$



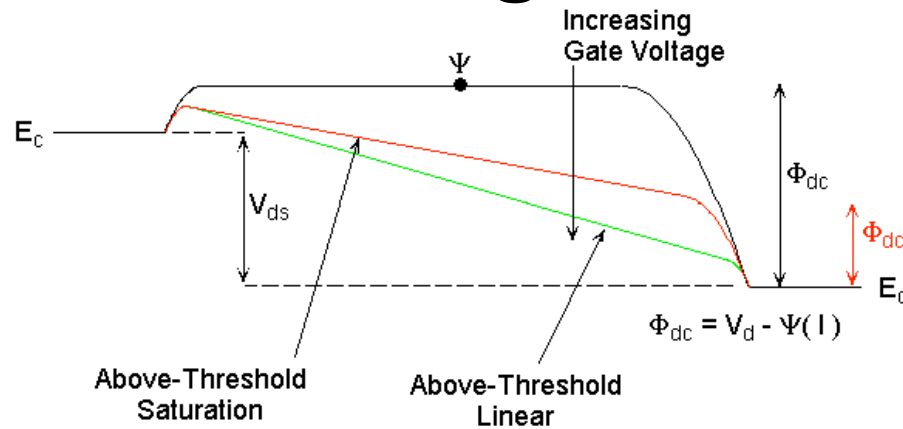
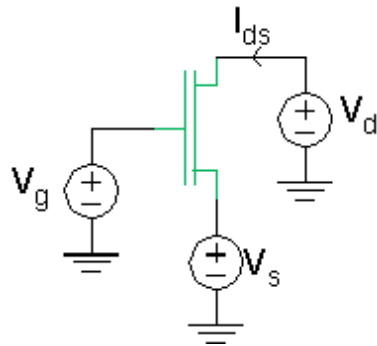
L = Drain Length

Diffusion: $J_n = q D_n \frac{dn}{dx} = q D_n \frac{n_{source} - n_{drain}}{l} = (q D_n / l) (e^{(\Psi - V_s)/U_T} - e^{(\Psi - V_d)/U_T})$

$$I = I_0 (e^{(\kappa V_g - V_s)/U_T} - e^{(\kappa V_g - V_d)/U_T})$$



MOSFET Current-Voltage Curves



$$I = I_f - I_r$$

EKV Model

$$I_{f,r} = 2 I_{th} \ln^2 \left(1 + e^{(\kappa(V_g - V_T) - V_{s,d} - \sigma V_{d,s}) / 2U_T} \right)$$

$$I_{th} = \mu C_{ox} U_T^2 (W/L) / \kappa \quad \leftarrow \text{DIBL} / V_A$$

Subthreshold

$$I = 2 I_{th} \left(e^{(\kappa(V_g - V_T) - V_s - \sigma V_d) / U_T} - e^{(\kappa(V_g - V_T) - V_d - \sigma V_s) / U_T} \right)$$

$$I_f = 2 I_{th} e^{(\kappa(V_g - V_T) - V_s - \sigma V_d) / U_T} \quad (\text{Saturation, } V_{ds} > 4U_T)$$

Above-threshold

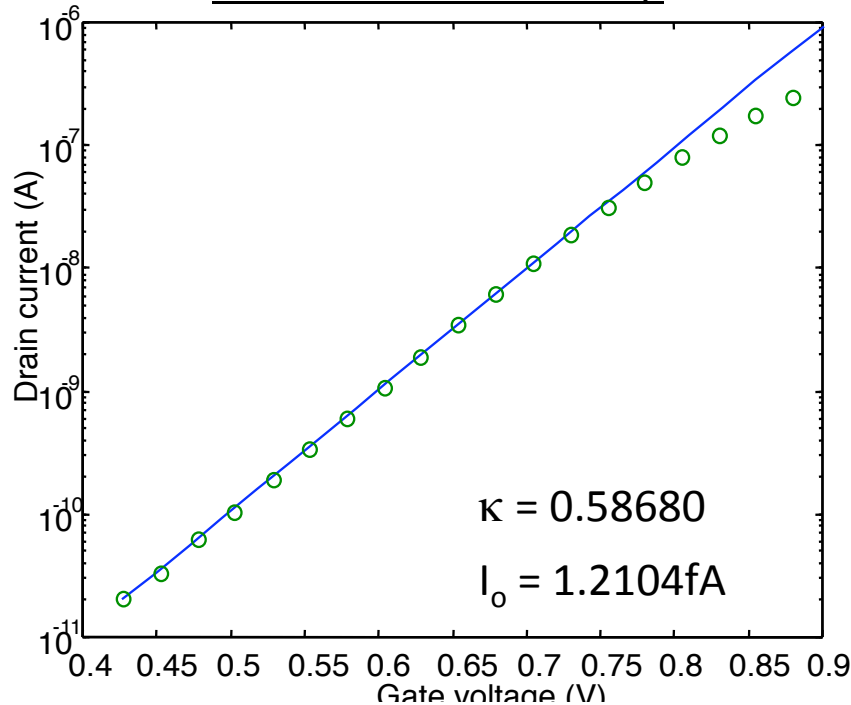
(Saturation, $I_R \sim 0$, $V_{ds} > V_{on}$)

$$I_f = (\mu C_{ox} / \kappa) (W/L) / \left((\kappa(V_g - V_T) - V_s - \sigma V_d) \right)^2$$

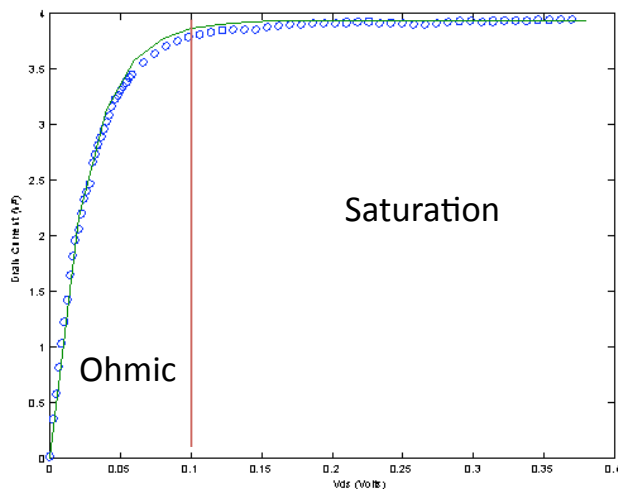
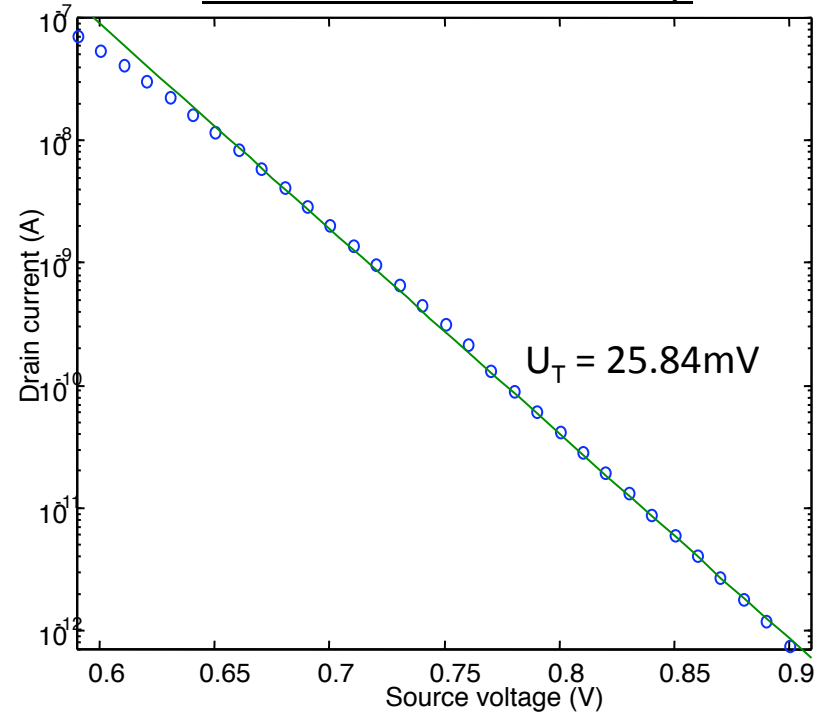


Measured Channel Current

Current for Gate Sweep



Current for Source Sweep



Current for Drain Sweep

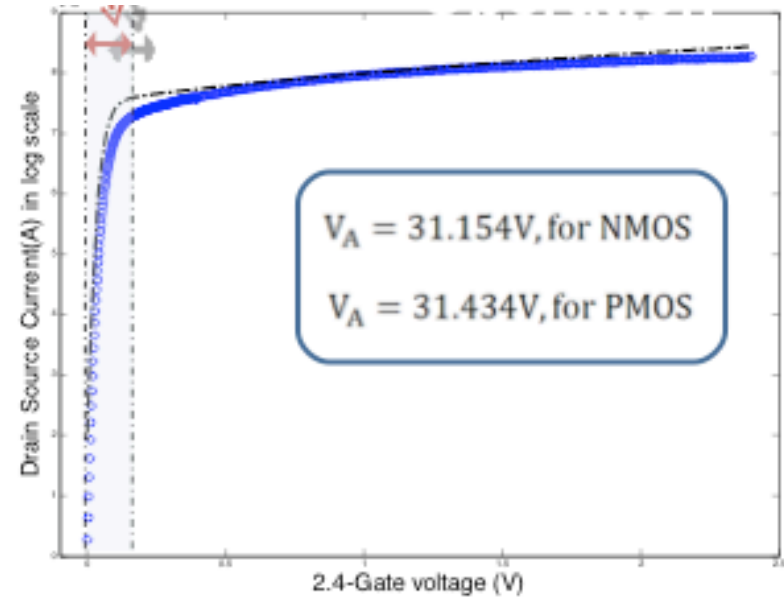
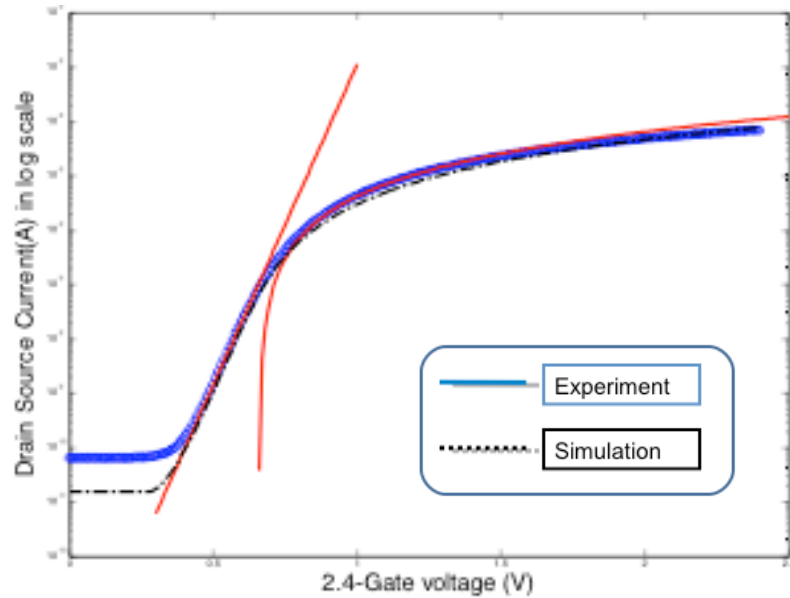
$$I_{ds} = I_0 e^{kV_g / U_T} (e^{-V_s / U_T} - e^{-V_d / U_T})$$

$$= I_0 e^{(kV_g - V_s) / U_T} \quad (V_{ds} > 4 U_T)$$

"Saturation"



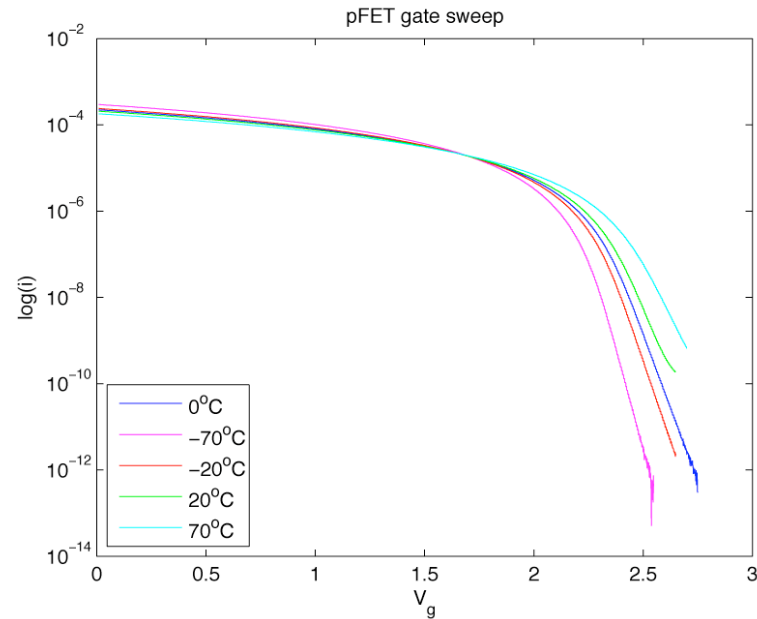
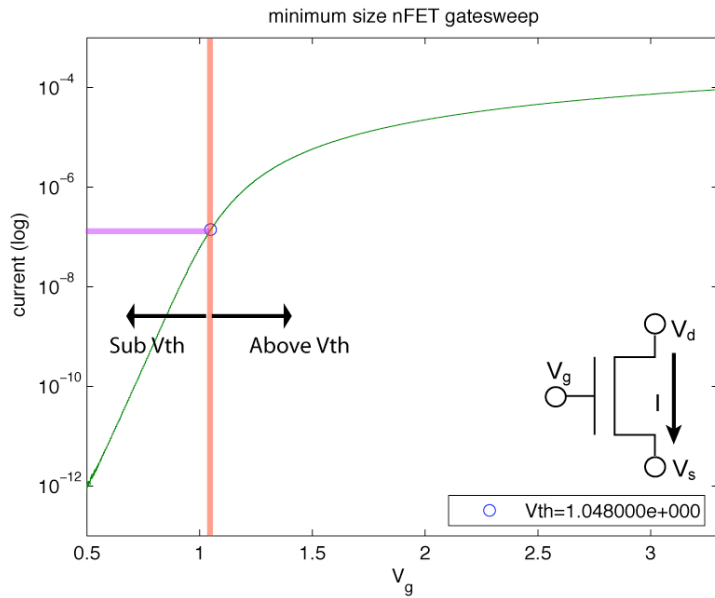
Measured Channel Current



Parameters	NMOS	PMOS
V_{T0} (V)	0.405	-0.620
K' ($\mu\text{A}/\text{V}^2$)	40.6 \rightarrow 55	27.7
γ	0.45	0.38
$2\phi_f$	0.38	0.38



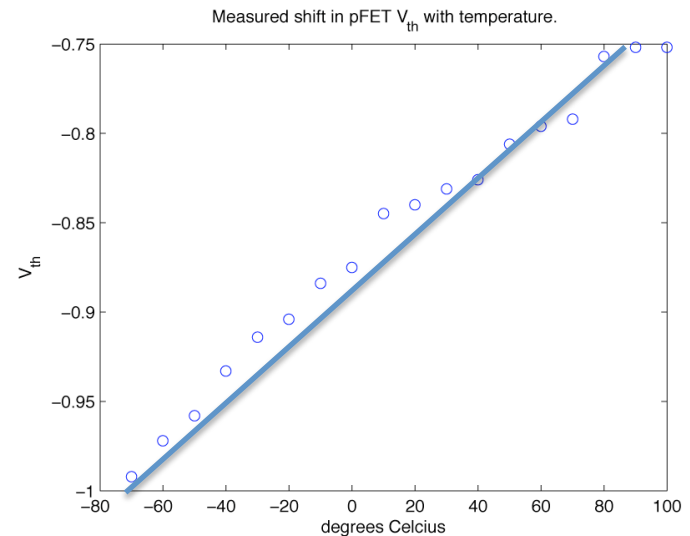
MOSFET Temp Modeling for Circuits



$$I_f = 2 I_{th} \ln^2 \left(1 + e^{(\kappa(V_g - V_T) - V_s - \sigma V_d) / 2U_T} \right)$$

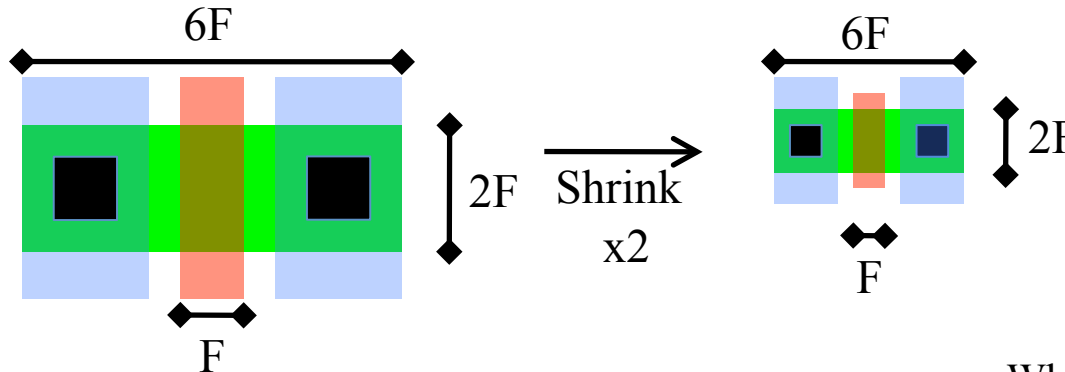
$$I_{th} \sim f(T^{1/2})$$

$$V_{T0} = V_{FB} + \frac{V_{BG}}{\kappa} + 2U_t \ln \left(\frac{N_D}{\sqrt{N_C N_D}} \right)$$



View of Scaling FET Devices

Classic Scaling (1971 –)



F minimum channel length

Tox (min) ~ 2nm (FET)
 ~ 5-6nm (FG FET)
 (multiple oxides available)

Key steps to Shrinking an FET

- Shrink lateral dimensions (lithography)
- To keep gain constant (VA constant), decrease size of depletion regions (x2) increase substrate doping (x4)
- Then, to keep κ (sub VT slope) constant, decrease size of gate oxide

What if we don't follow the steps?



Decreased gain (effective L changes),
 punchthrough (effective L ~ 0)



κ decreases.

If starting $\kappa = 0.75$,

for x2 shrink, $\kappa = 0.67$

for x3 shrink, $\kappa = 0.5$

for x6 shrink, $\kappa = 0.33$



Memory Technologies

RAM

SRAM - Basic latch structure / sense amplifiers

DRAM

ROM

ROM / PROM / EPROM / EEPROM / Flash

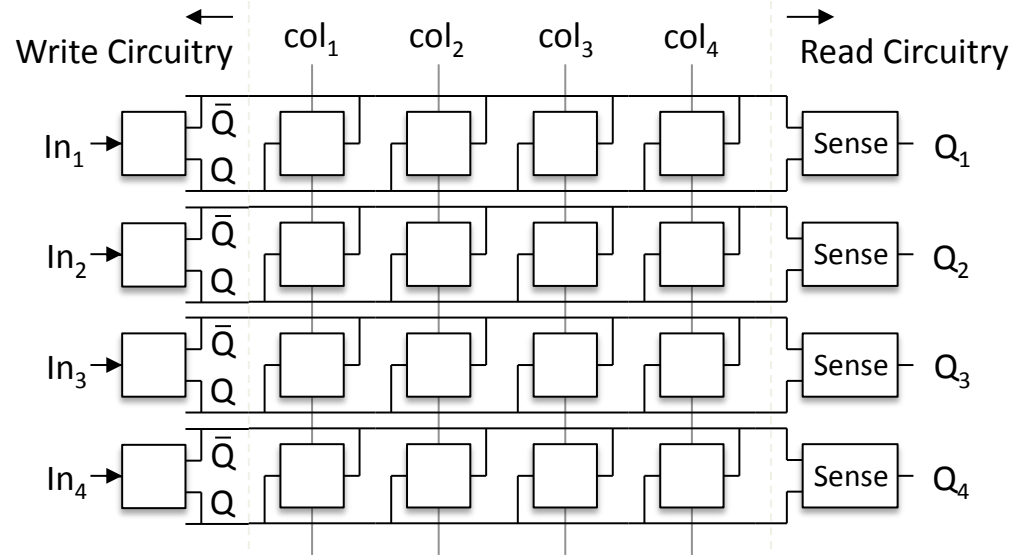
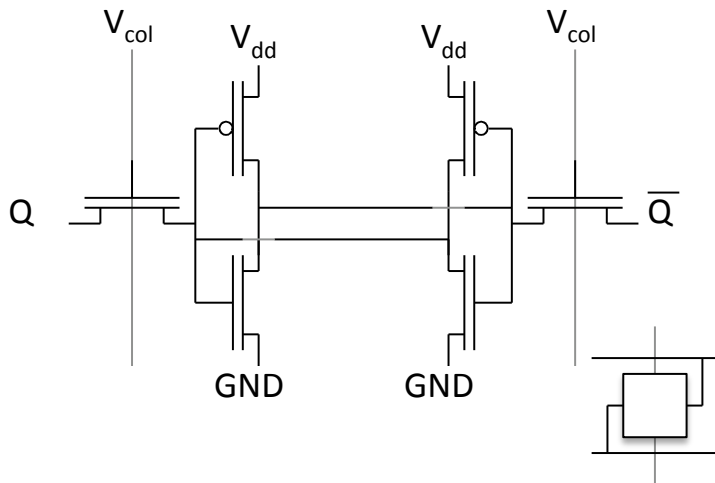
Basic Charge modification – UV, FN electron tunneling, Hot electron injection

Nonvolatile elements used for circuits



SRAM Cell Basics

Basic 6-T SRAM cell



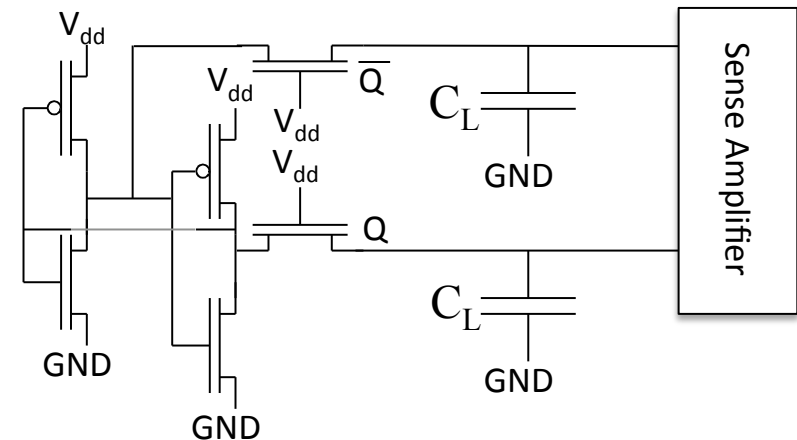
Small latch + minimal transistors to access

Depending on static current for the MOSFETs,
(sub VT currents and gate currents)
can have significant current draw (Power)

Latch restores signals to Power rails

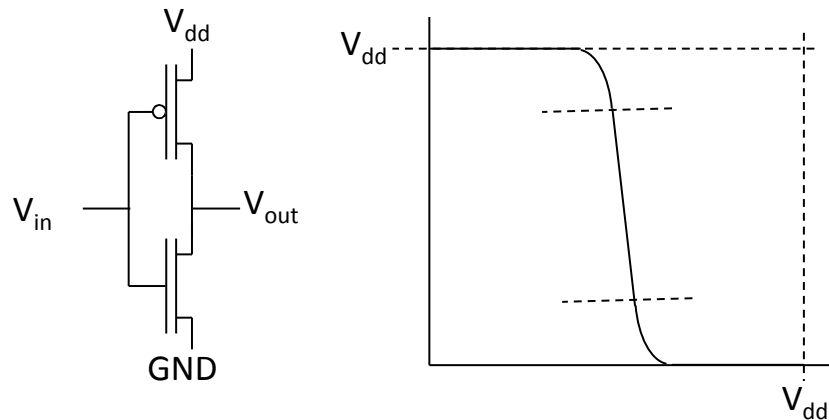
- One input to Latch will be below Vdd

Read Circuitry

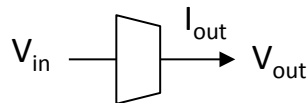


Basic Latch Comparator Structure

Start with two inputs near $V_{dd}/2$
(therefore outputs near $V_{dd}/2$)



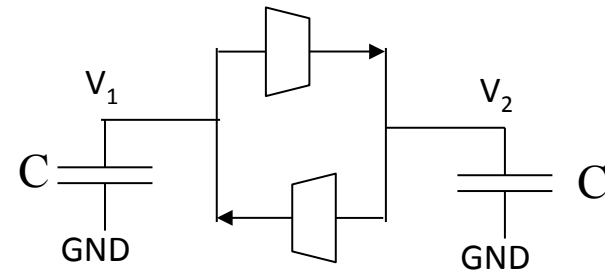
Both transistors saturated
~ current sources



Transconductance
Amplifier

$$I_{out} \sim -G V_{in}$$

Sense Amplifier is a
latch-type comparator circuit



$$C \frac{dV_1}{dt} + G V_2 = 0$$

$$C \frac{dV_2}{dt} + G V_1 = 0$$

$$V_d = V_1 - V_2, \tau = C/G$$

$$\tau \frac{dV_d}{dt} = V_d \longrightarrow V_d(t) = V_d(0) e^{t/\tau}$$

$$t = \tau \ln (V_d(t) / V_d(0))$$

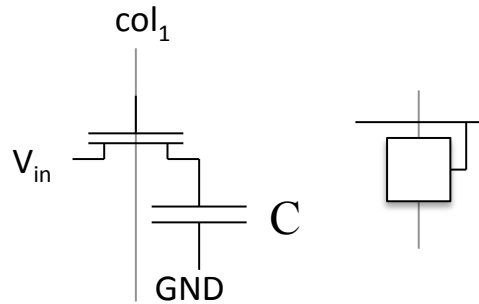
Time to increase a factor of e is τ

One of few circuits using positive feedback



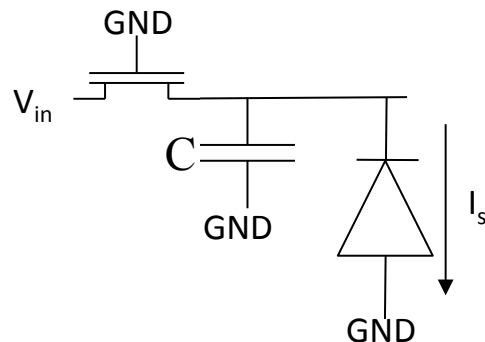
DRAM Cell Basics

Basic 1-T DRAM cell

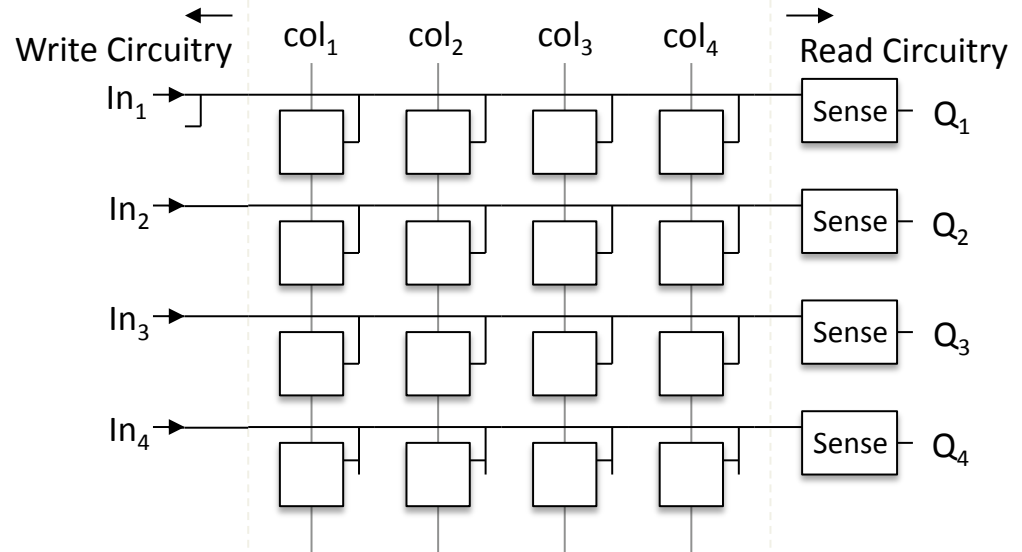


Writing is relatively easy,
Memory Refresh is needed
Reading is hard

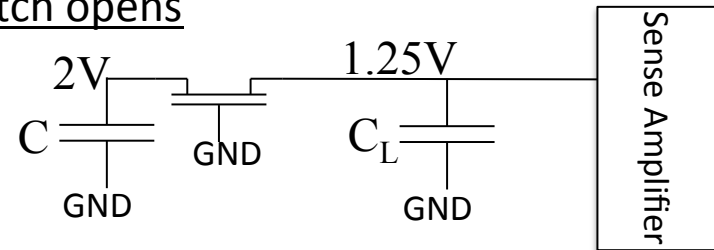
Capacitor is a s-d junction,
or more specialized etched device



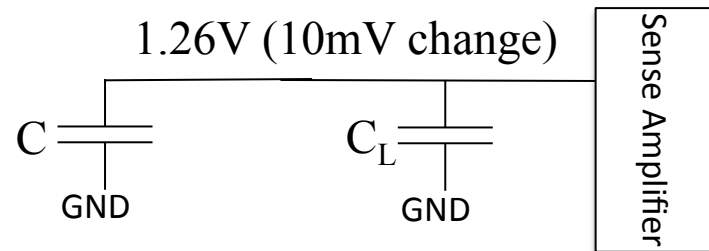
Other leakage
just adds to
this level



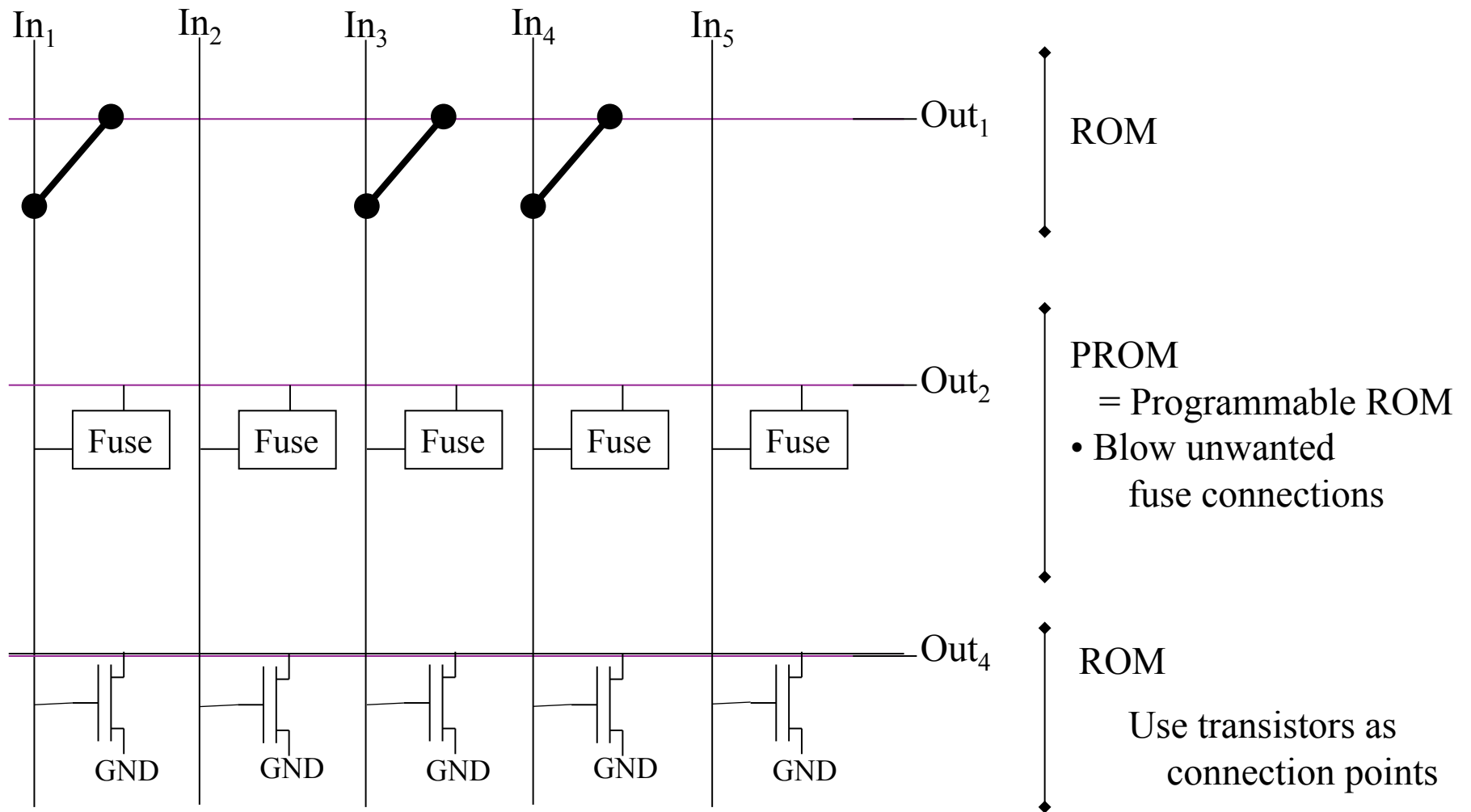
Before switch opens



After switch opens $C_L \gg C$ (lets say 200x)

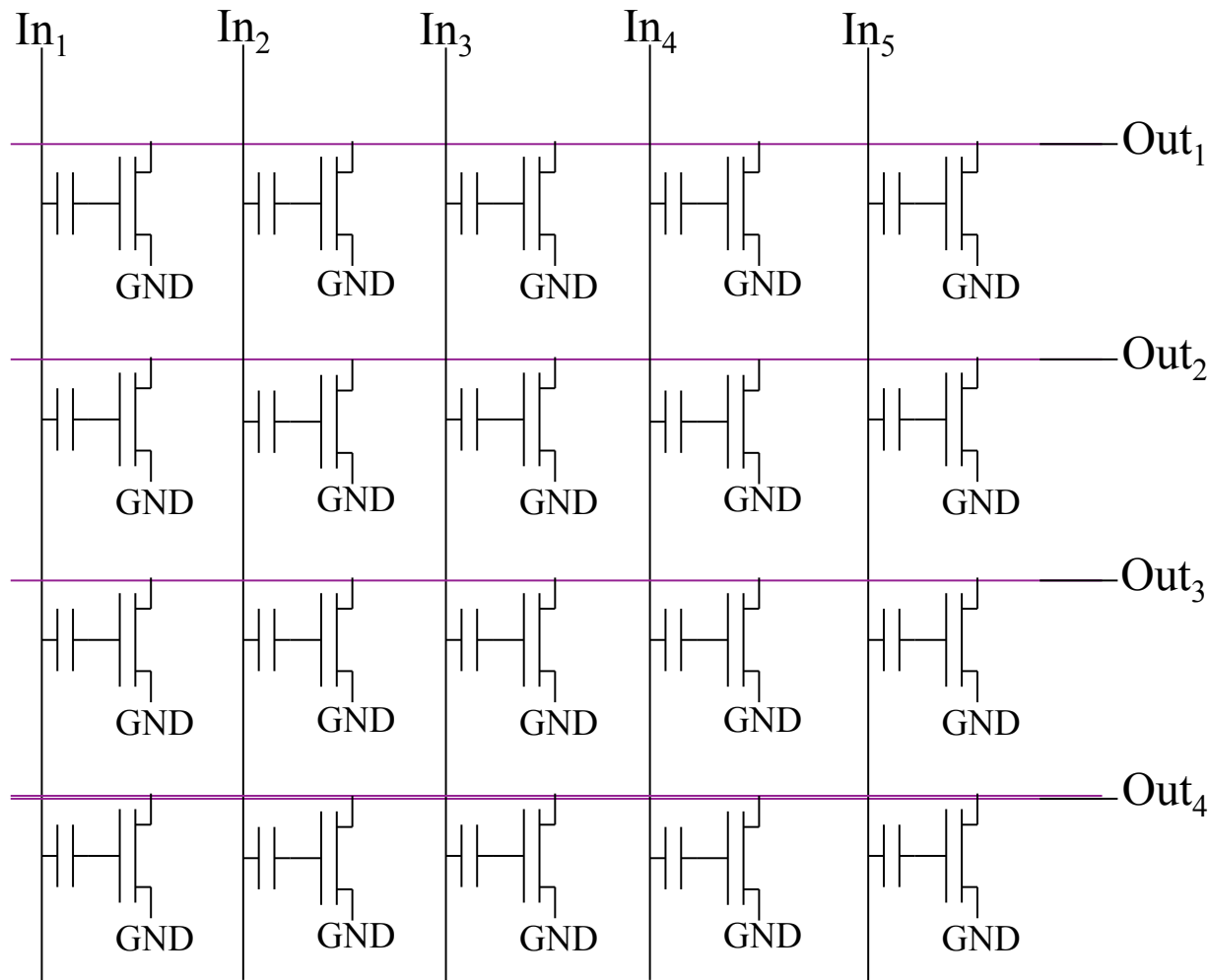


Basic ROM Concept



Basic EPROM Concept

(EPROM = Erasable Programmable ROM)

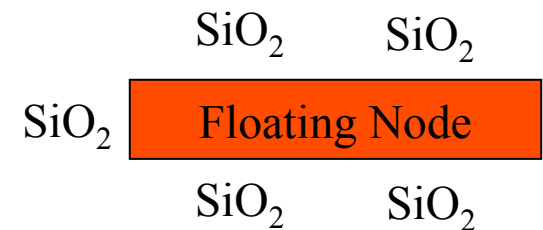


Use a floating-gate transistor between connections

To program a connection:

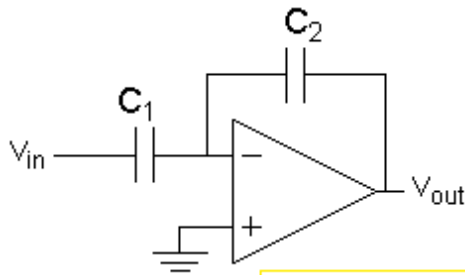
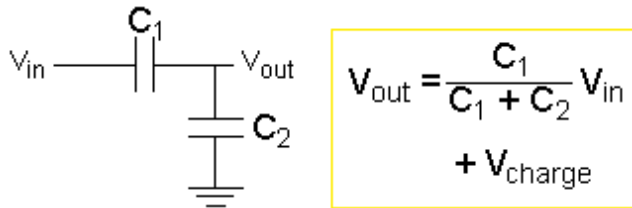
- Tunneling to program
- Erase (the whole IC) through UV

1969 - First EPROM cell (S. Sze, et. al)



Floating-Gate Circuit Basics

Capacitor-Based Circuit Design

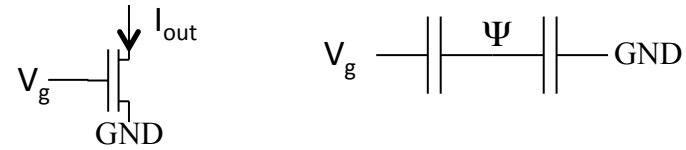


$$V_{out} = -\frac{C_1}{C_2} V_{in} + V_{charge}$$

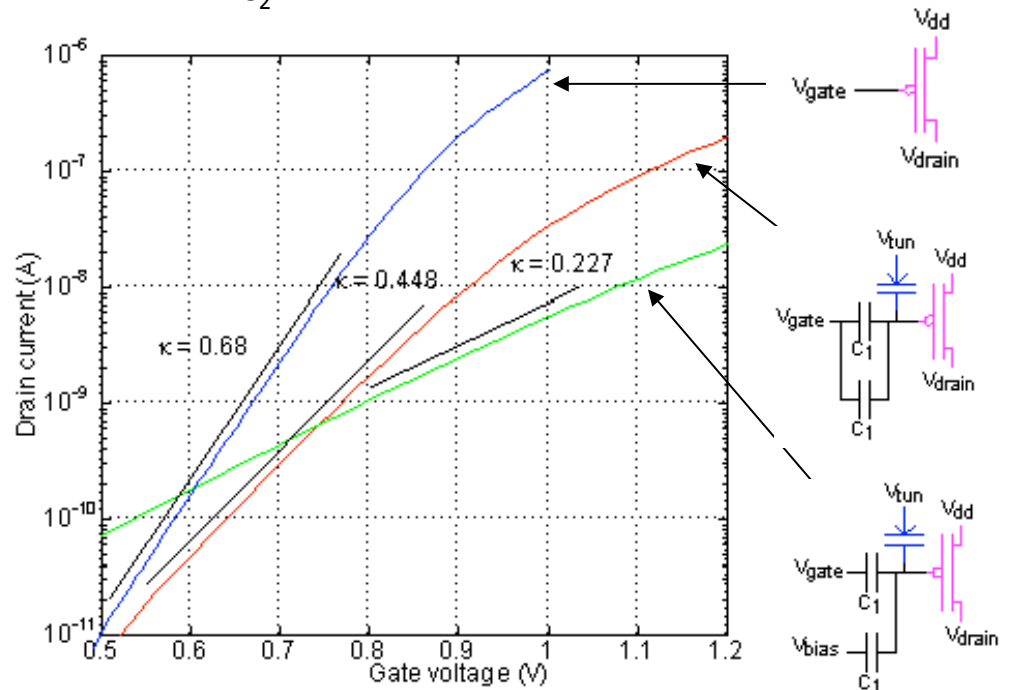
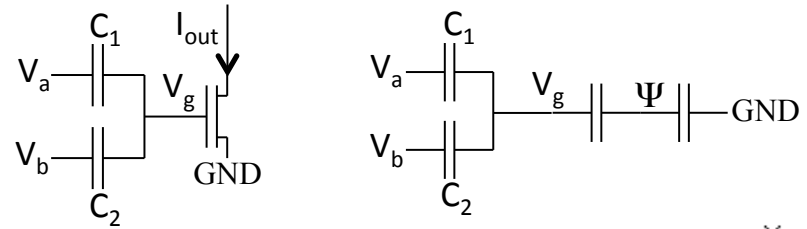
Resistors and Inductors define the circuit dynamics

Capacitors are the natural elements on silicon ICs

Basic MOSFET Transistor

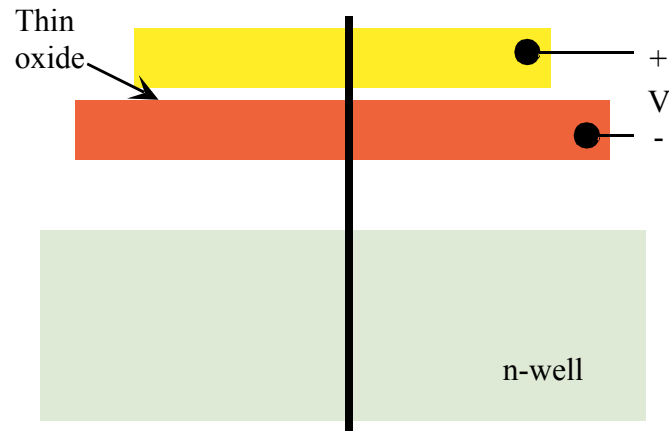


Basic FG MOSFET Transistor

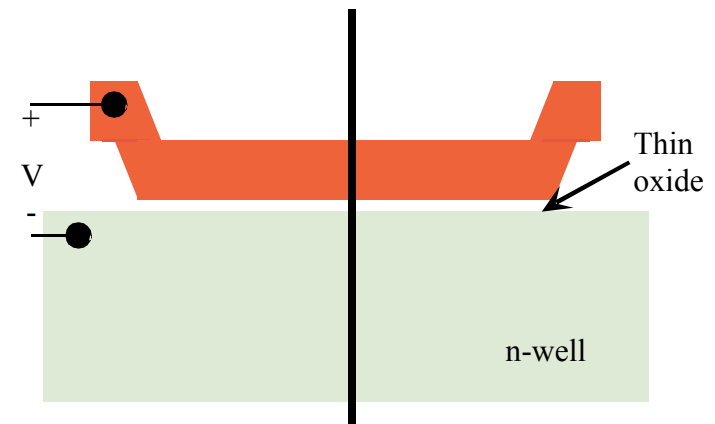
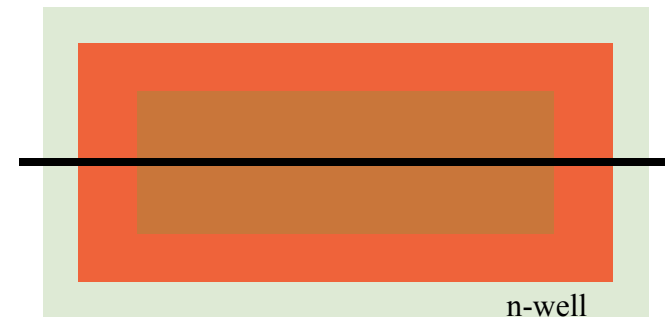


Types of Integrated Capacitors

Double-Poly Capacitors

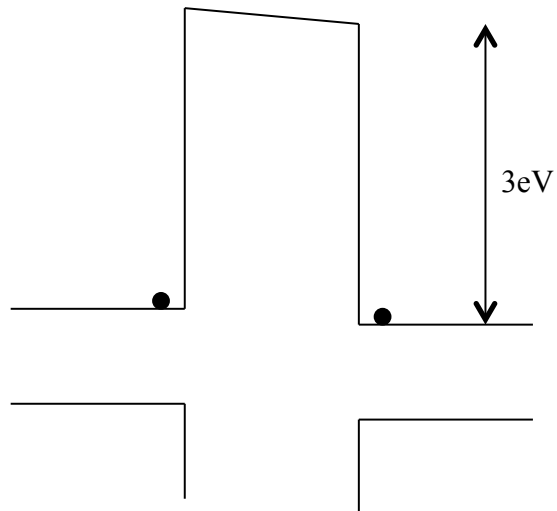
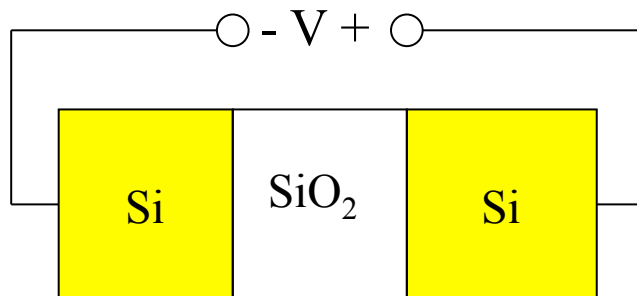


Well-Based MOS Capacitors

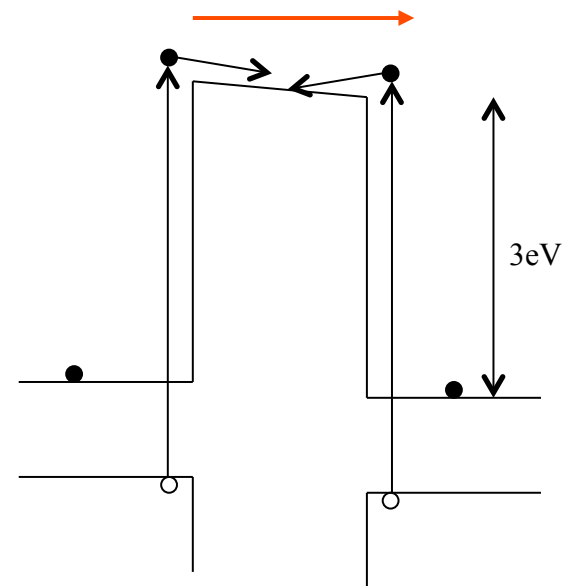
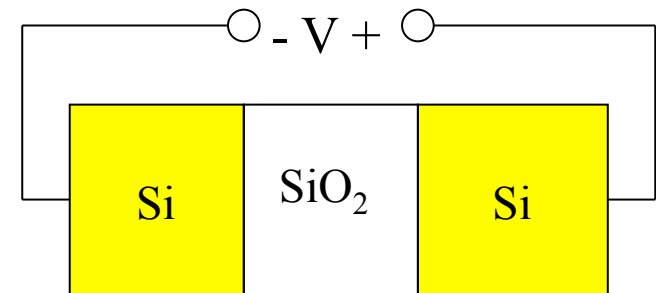


UV Photoinjection

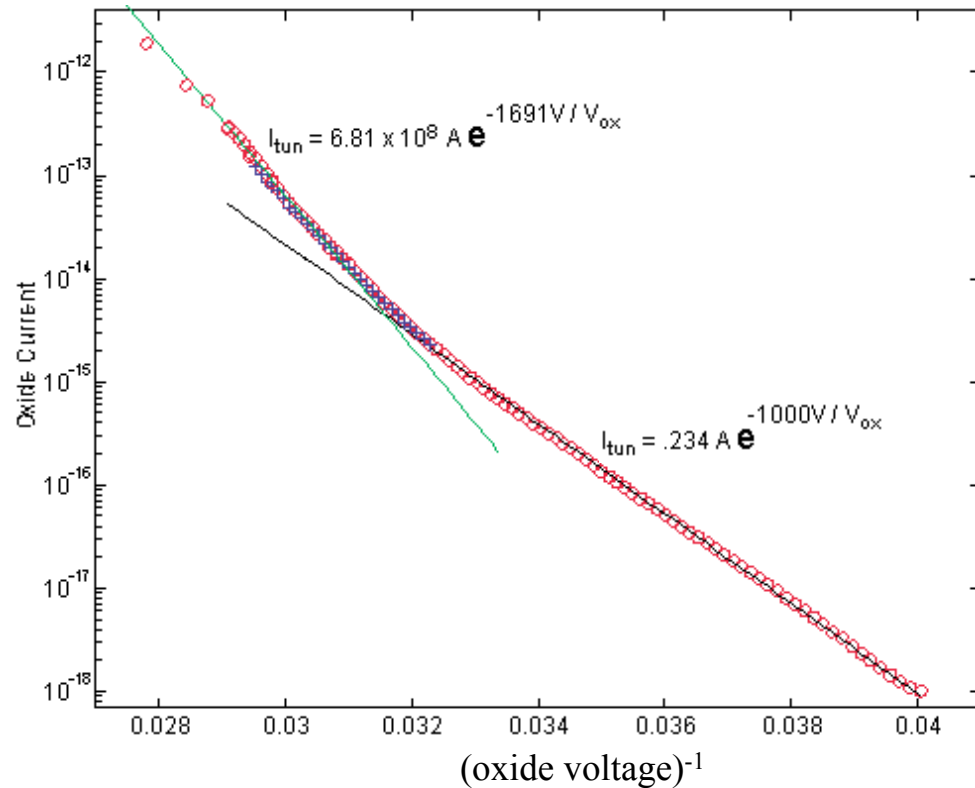
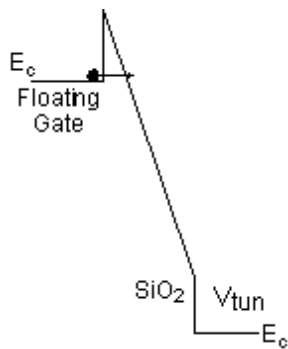
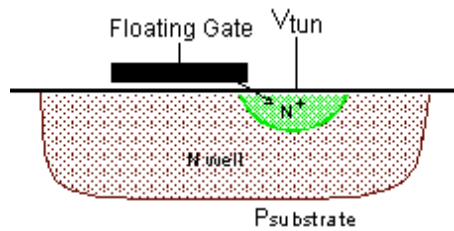
Dark Measurements



UV light (> 4.1eV)



Electron Tunneling



Scaling Theory for Electron

$$I_{tun} = I_{tun0} e^{-E} \\ = I_{tun0} e^{-}$$

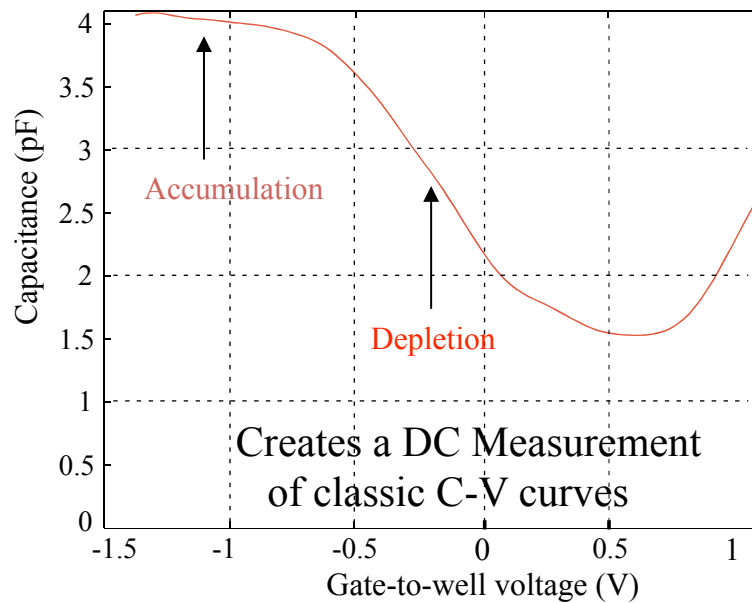
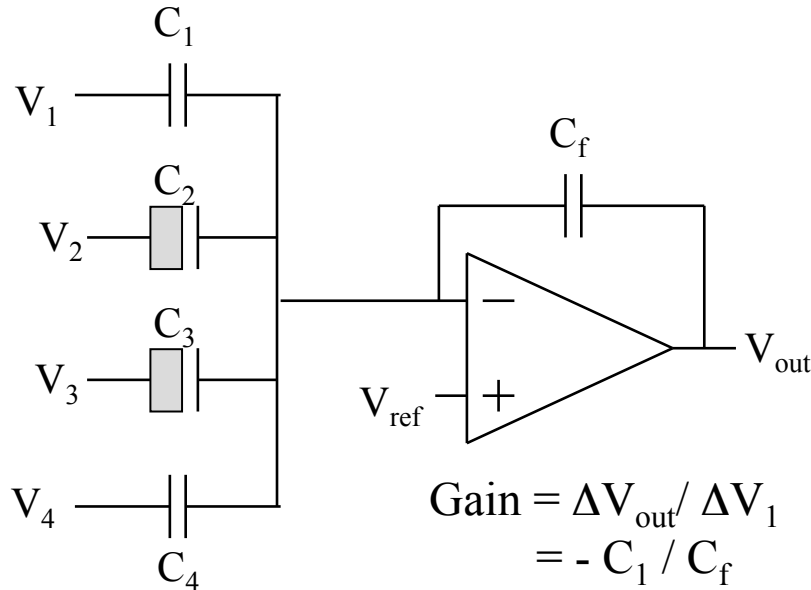
Increasing the applied voltage decreases the effective barrier width
The range of tunneling currents span many orders of magnitude.

Tunneling Curve (Theory) for

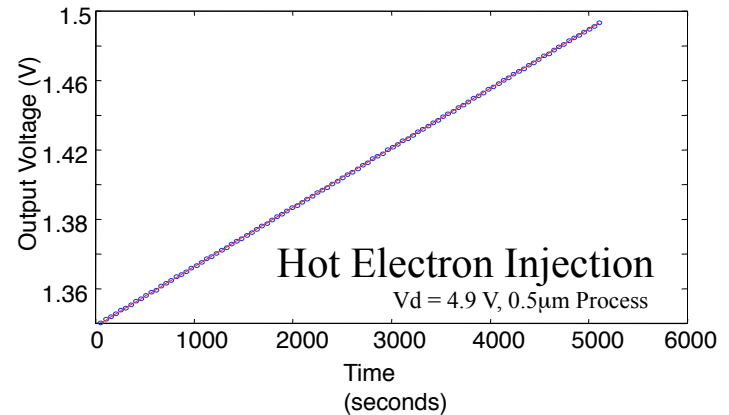
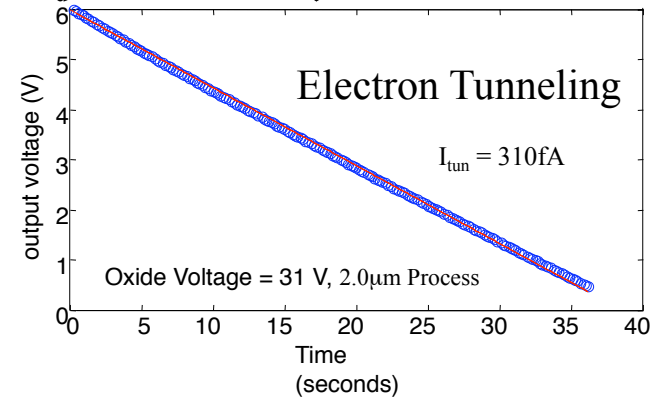
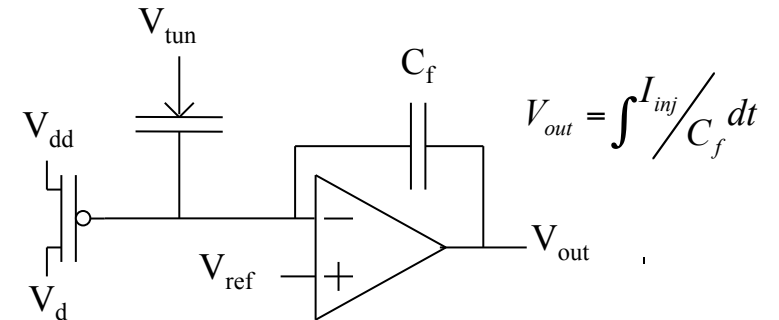
108mV



How to characterize these devices?



FG Current Measurement

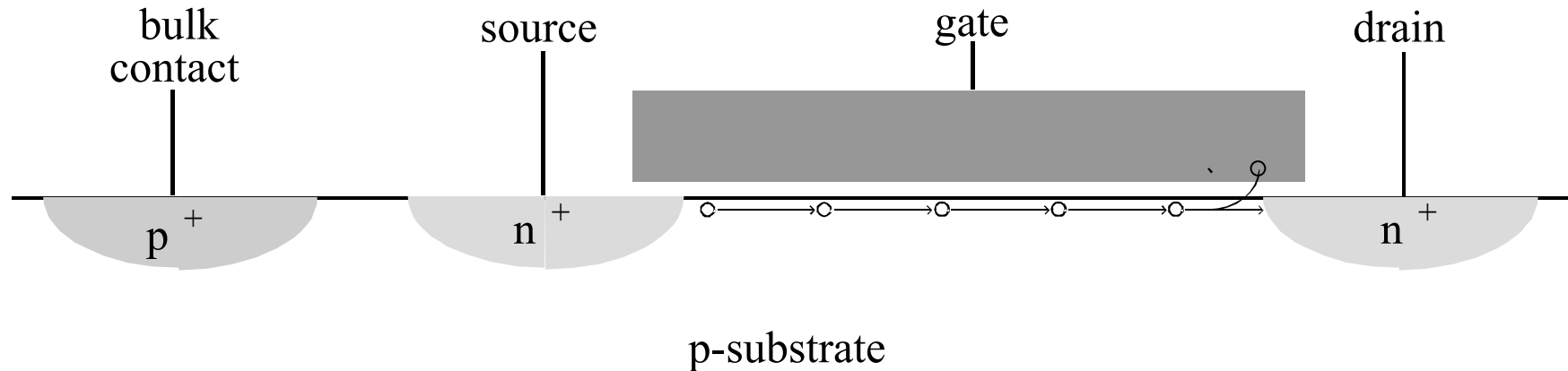


EEPROM Cells

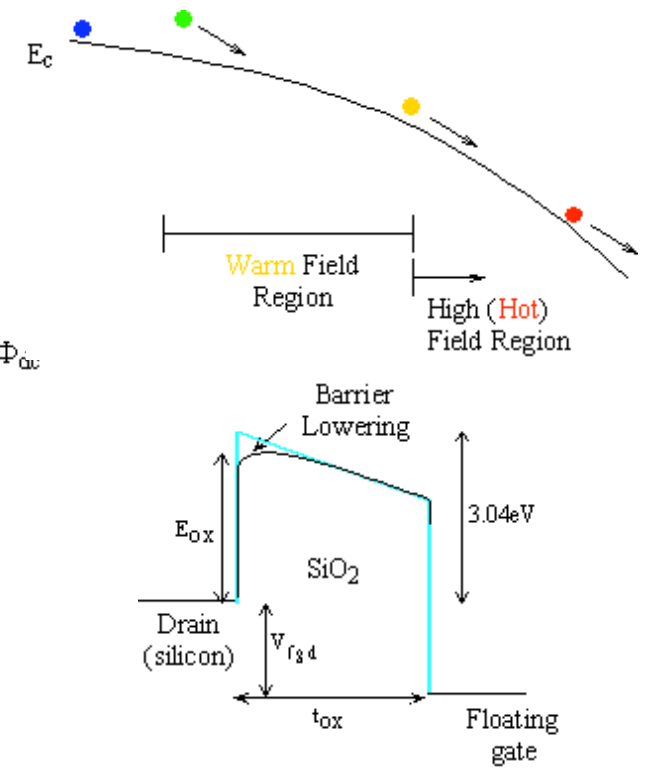
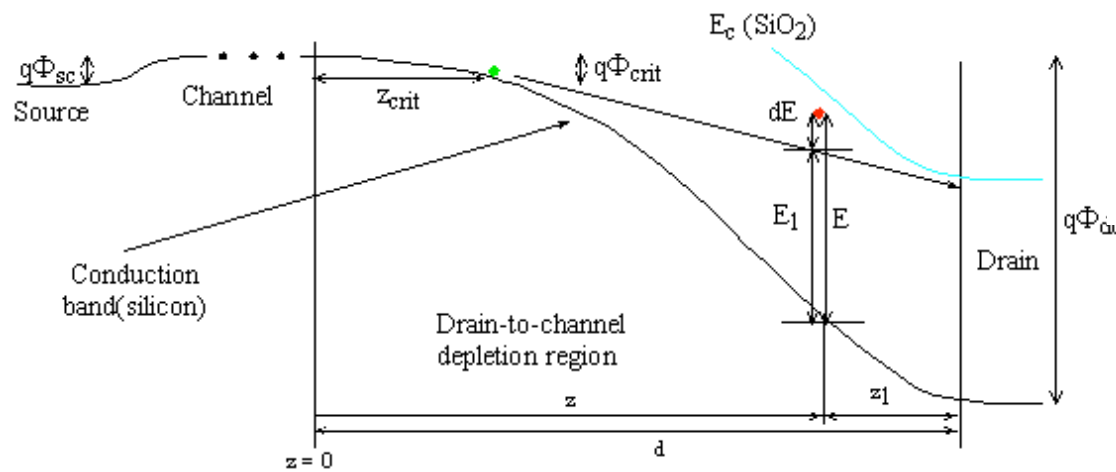
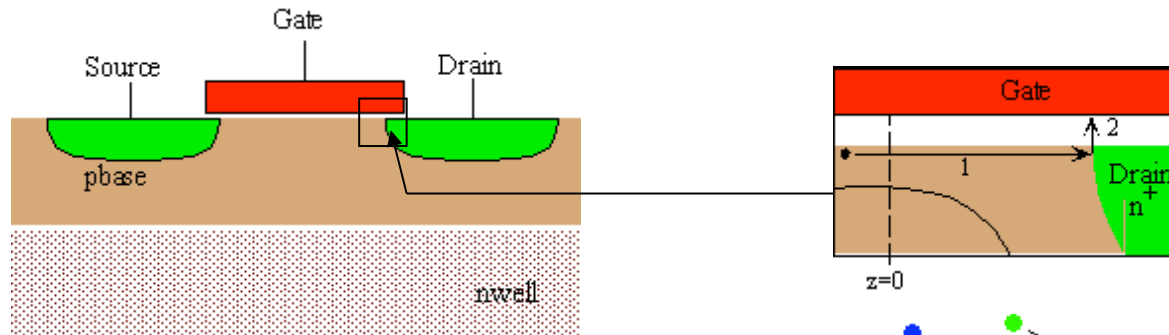
(EEPROM = Electrically Erasable PROM)

Modification of the cell for programming

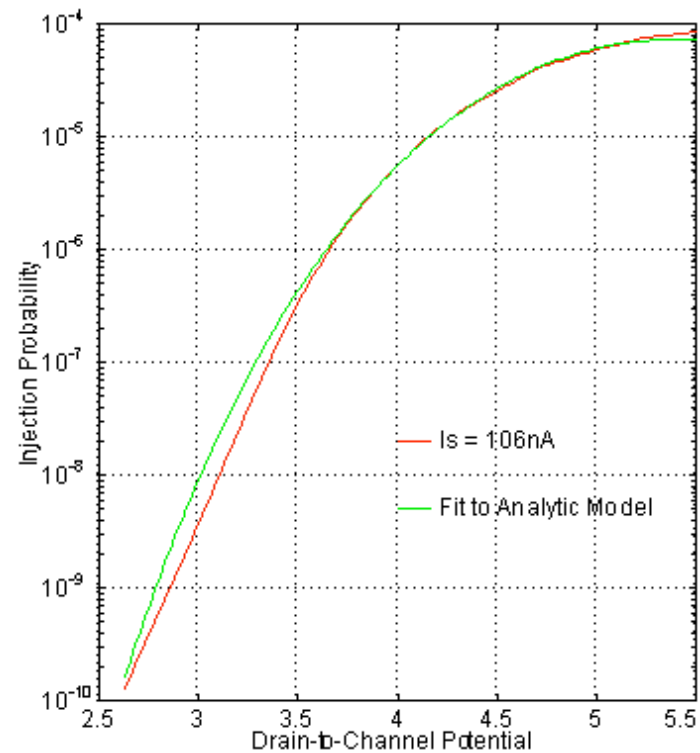
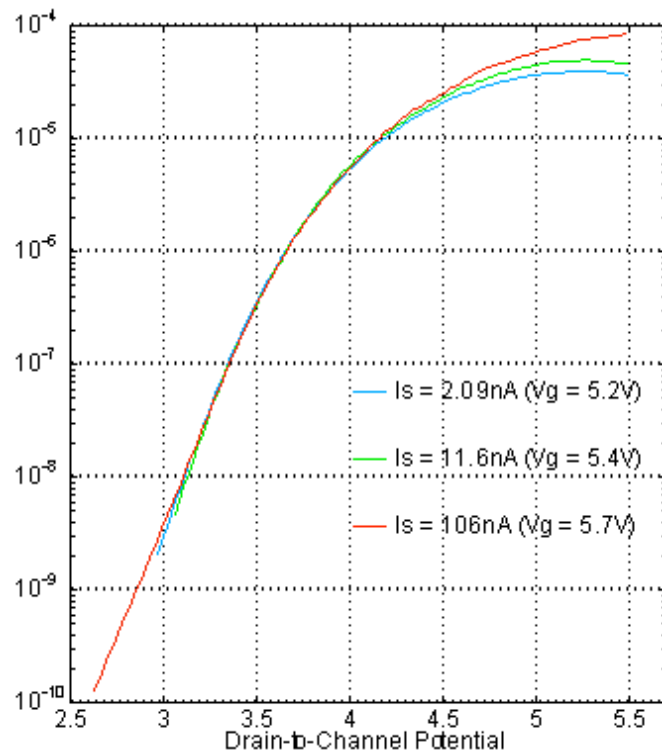
- Eliminate need for UV
- Early cells: Tunneling to program and erase (80's, early 90's)
- Flash EEPROM: Tunneling to program, and Injection for block erase
- Most current cells use injection and tunneling



Electron Transport in a subthreshold nFET



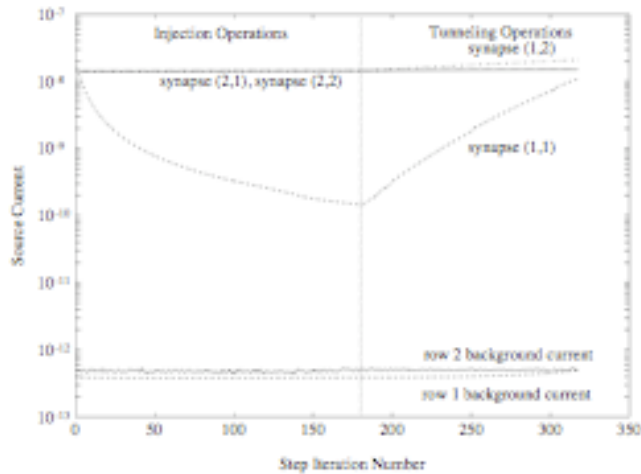
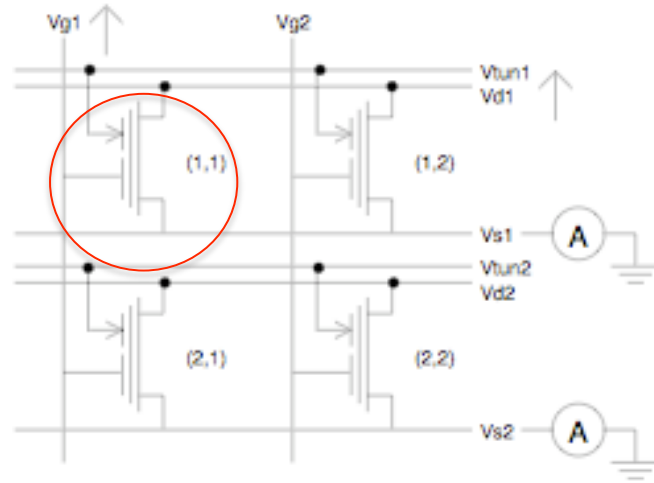
Measurements and Modeling of Hot-Electron Injection



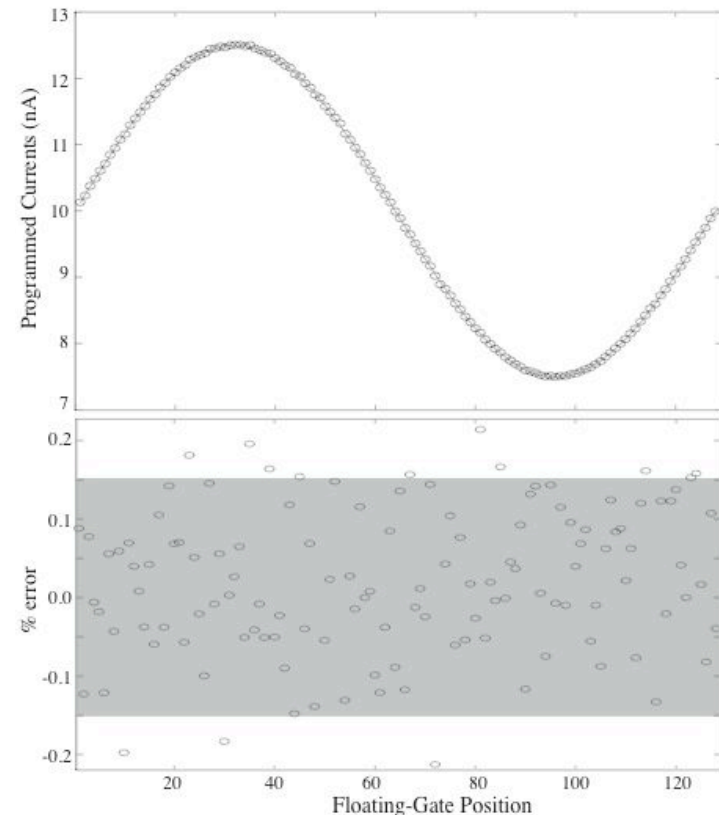
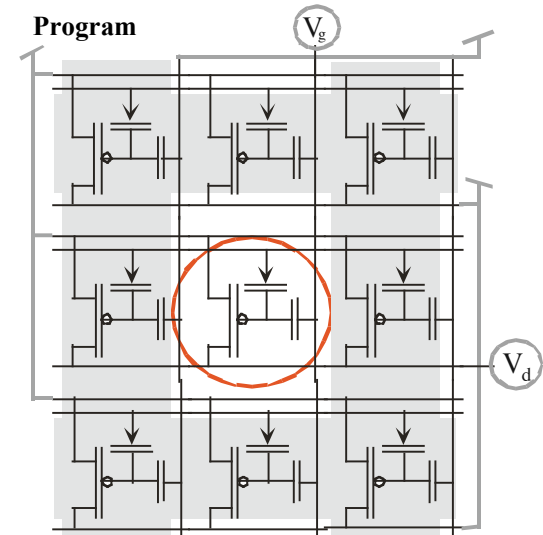
$$I_{inj} = 4.55 \times 10^{-3} I_s e^{-\frac{\lambda}{d - z_{crit}} \left(\frac{E_{ox} - \Phi_{dc} + E_R \frac{\lambda}{d} - \Phi_{crit}}{2 E_R} \right)^2}$$



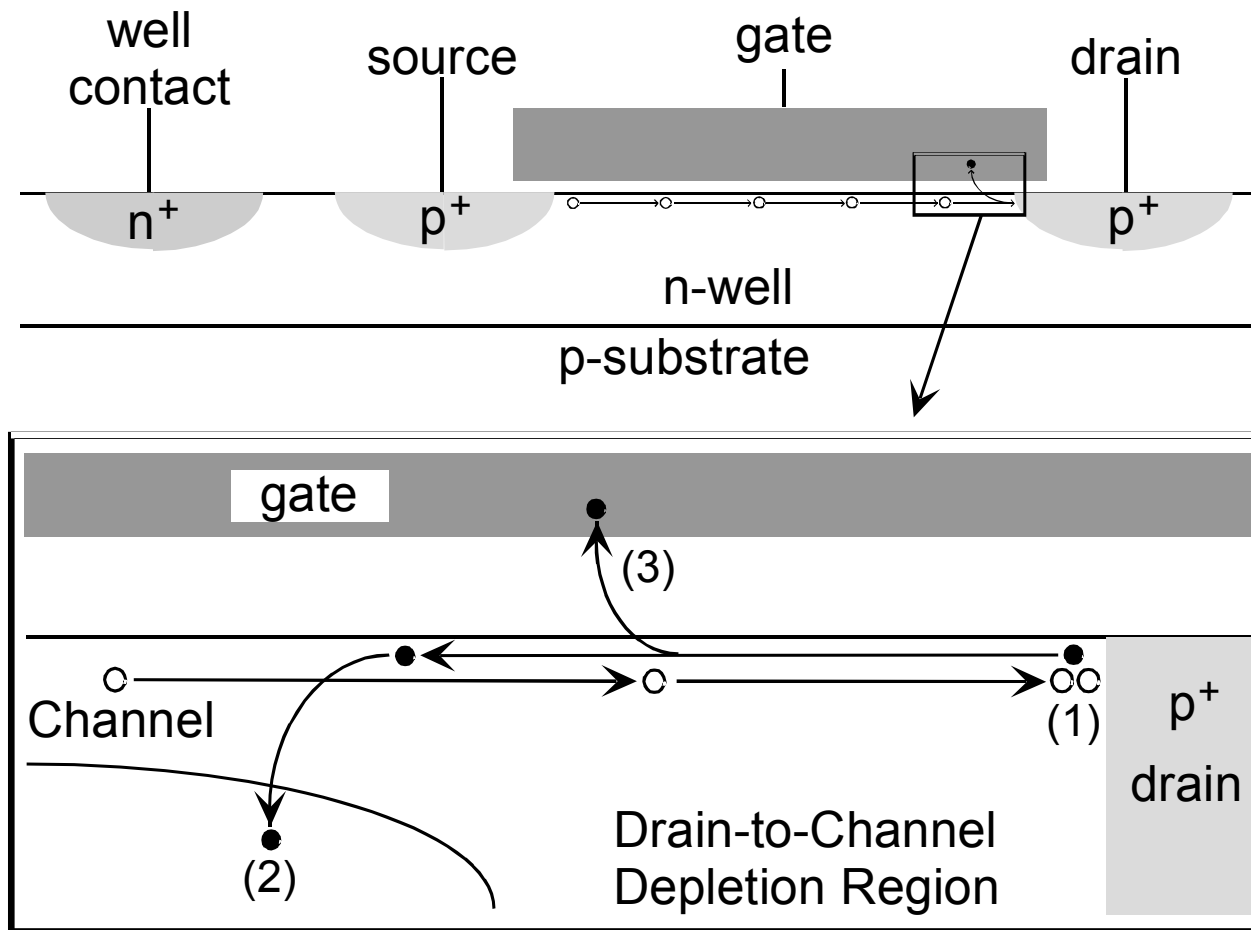
Writing Individual Devices



Injection ~ no interference
 Tunneling has some row interference



pFET Hot-Electron Injection



[Hasler, et. al. 1996, 1997]

[Duffy and Hasler, 2003]



Scaling of EEPROM devices

Wide use: Memory Sticks, Flash Cards (i.e. SD), etc.

Most approaches store multiple levels per cell (2, 4, 8, 16 → 1-4 bits/ cell)

Typical Densities: 70nm Flash – 1-2 G cells / cm² (production)

45nm Flash – 6-7 G cells / cm² (production)

32nm Flash ~ 10 G cells / cm² (development)

(densities include all support infrastructure / readout / programming)

All cells report > 10 year lifetime for storage,

consistent with 5-6nm oxide thicknesses (and our FG measurements as well)

(45nm and below has some modified dielectrics),

with ns read access times and ms (or less) individual cell write times

(consistent with our history of FG devices)

[1] N. Shibata, et. al, “A 70 nm 16 Gb 16-Level-Cell NAND flash Memory”, JSSC, vol. 43, no. 4, 2008 (ScanDisk / Toshiba)

[2] T. Futatsuyama, et. al, “A 113mm² 32Gb 3b/cell NAND Flash Memory,” ISSCC 2009.

[3] C. Trinh, et. al, “A 5.6MB/s 64Gb 4b/Cell NAND Flash Memory in 43nm CMOS,” ISSCC 2009 (ScanDisk / Toshiba)

[4] R. Zeng, et. al, “A 172mm² 32Gb MLC NAND Flash Memory in 34nm CMOS,” ISSCC 2009 (Intel & Micron)



Memory Technologies

MOSFET transistor modeling

RAM

SRAM - Basic latch structure / sense amplifiers

DRAM

ROM

ROM / PROM / EPROM / EEPROM / Flash

Basic Charge modification – UV, FN electron tunneling, Hot electron injection

Nonvolatile elements used for circuits

