

Physics and Transport Modeling in Nanoscale MOS Devices

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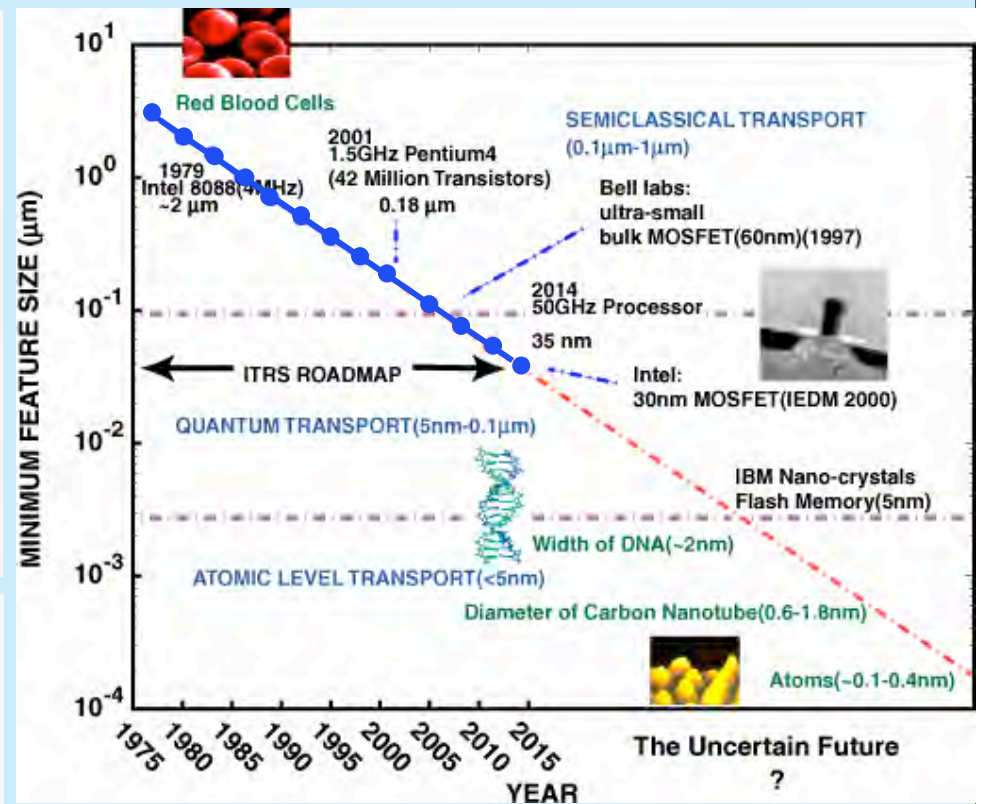
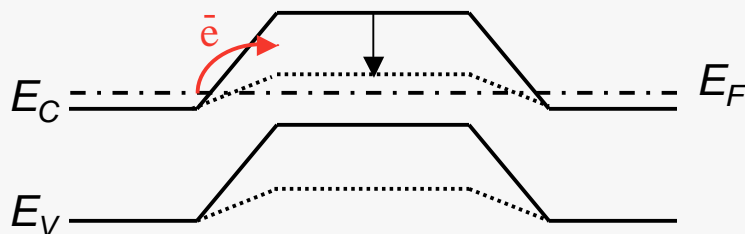
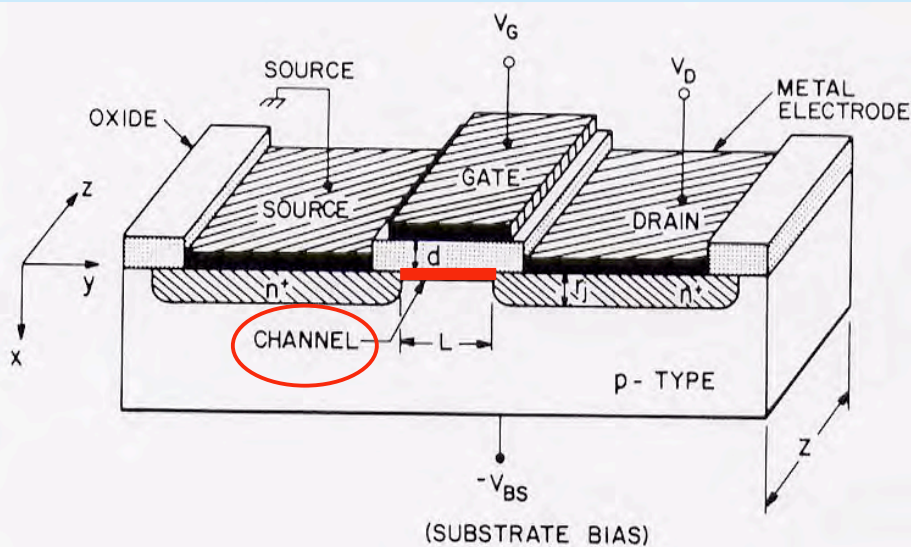
University of Illinois at Urbana-Champaign

Urbana, IL 61801, USA

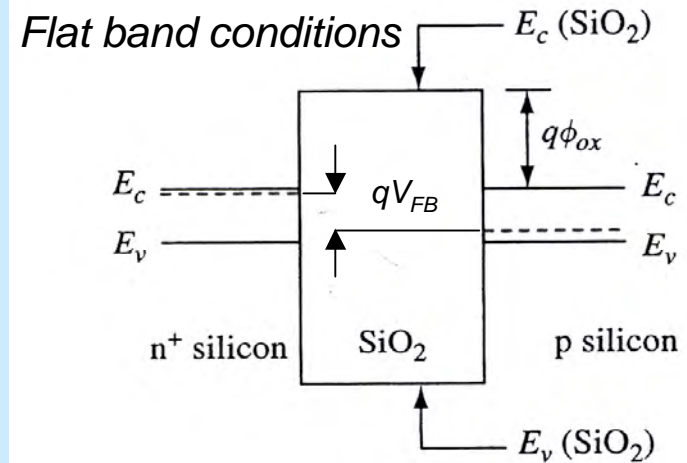
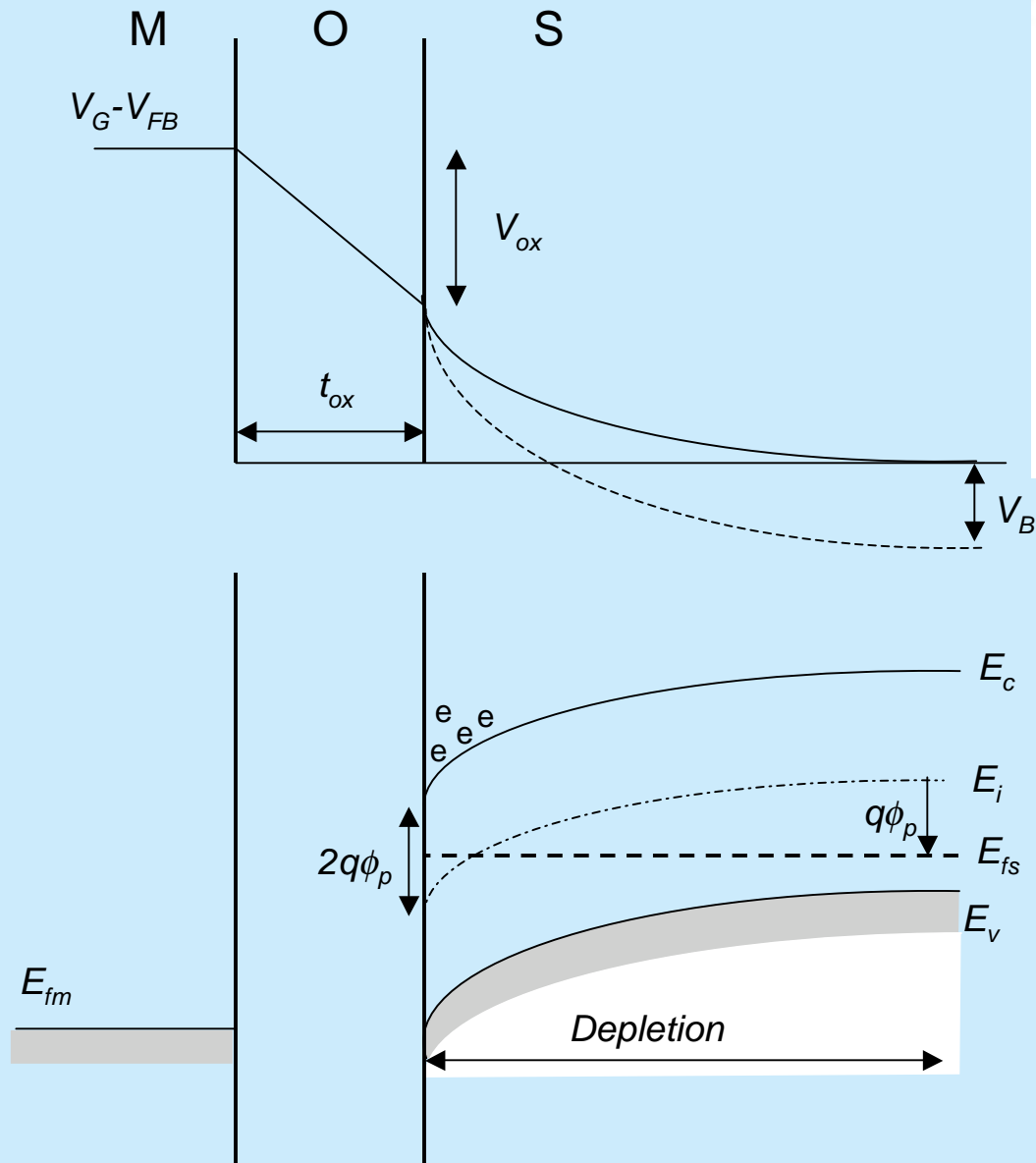


The incredible shrinking transistor

YUAN TAIIR
 Thomas J. Watson
 Research Center, IBM Corp.



Threshold Voltage: Channel Formation



After Y. Taur and T.H. Ning, FMVD, Cambridge, 2d ed.

Channel potential
(non-equilibrium)

Inversion potential

$$V_T = V_{FB} + V_C + 2\phi_p +$$

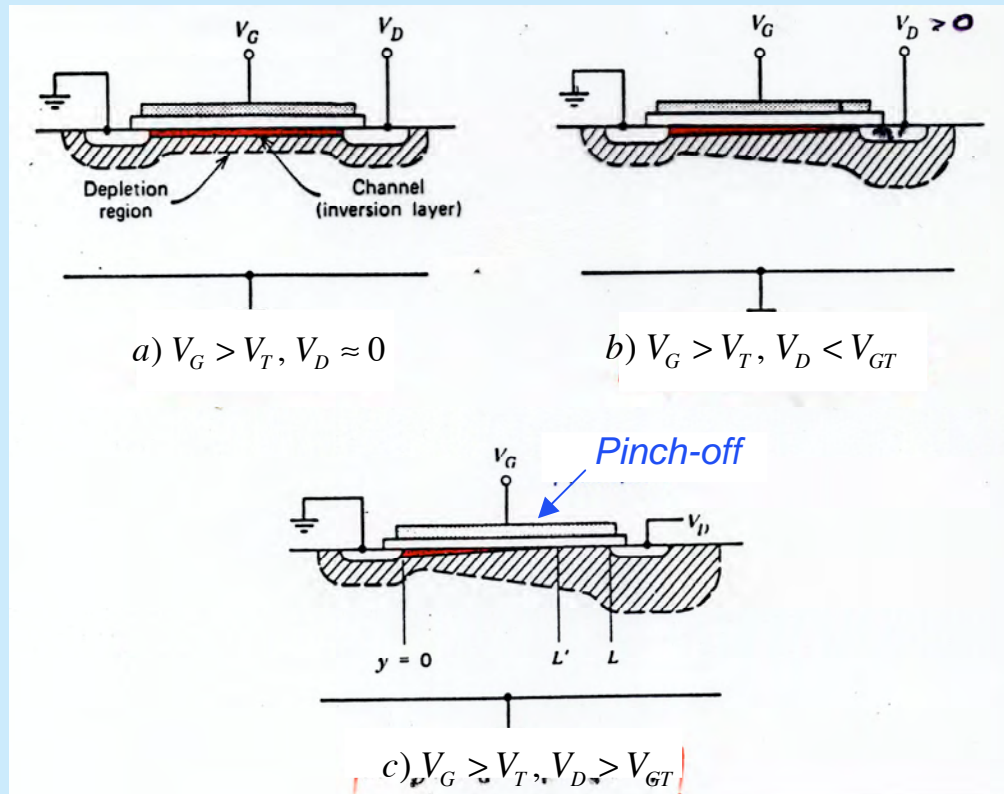
$$\frac{1}{C_{ox}} \sqrt{2\epsilon_0 \epsilon_s q N_a (2\phi_p + V_C - V_B)}$$

Depletion charge



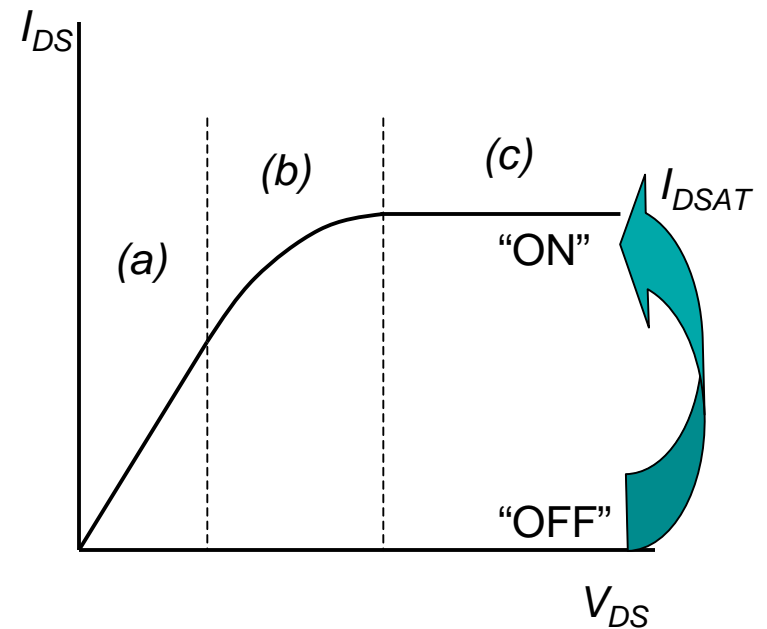
MOSFET Operation Principles*

Charge control operation

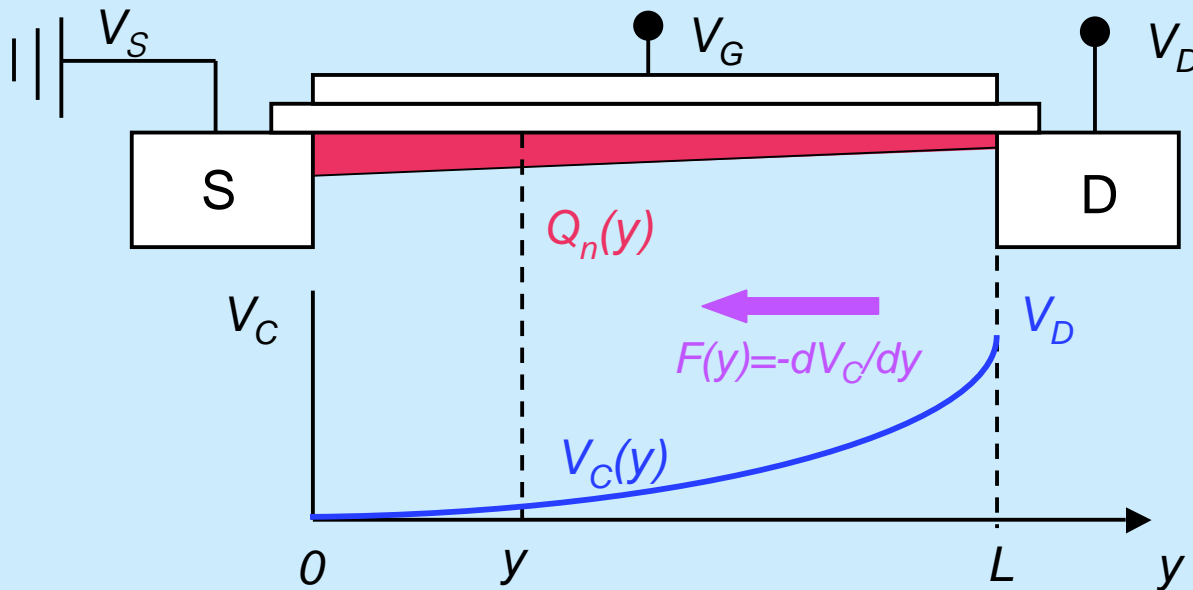


After R.S. Muller and T.I Kamins, DEIC, Wiley, 2d ed.

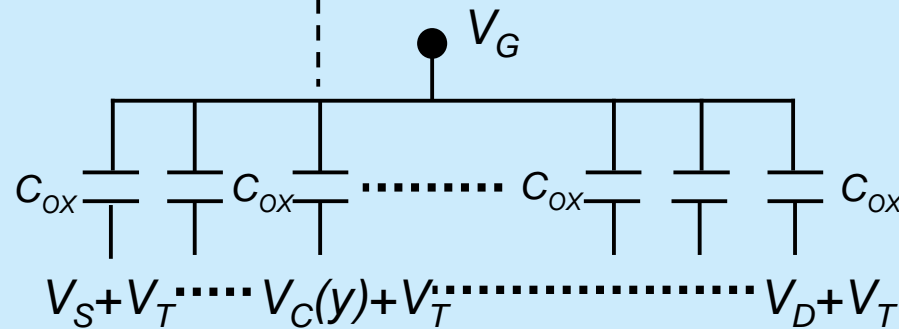
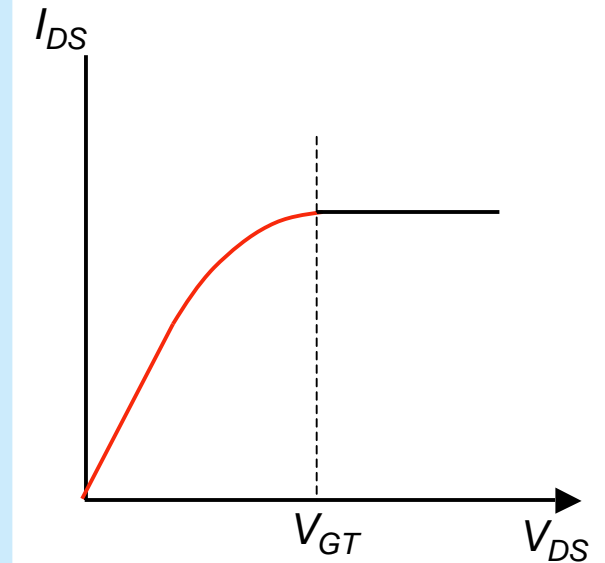
I-V Characteristic



Gradual Channel Approximation ($V_{GT} \geq V_{DS}$)



$$I_{DS} = \frac{W}{L} C_{ox} \mu \left[(V_G - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

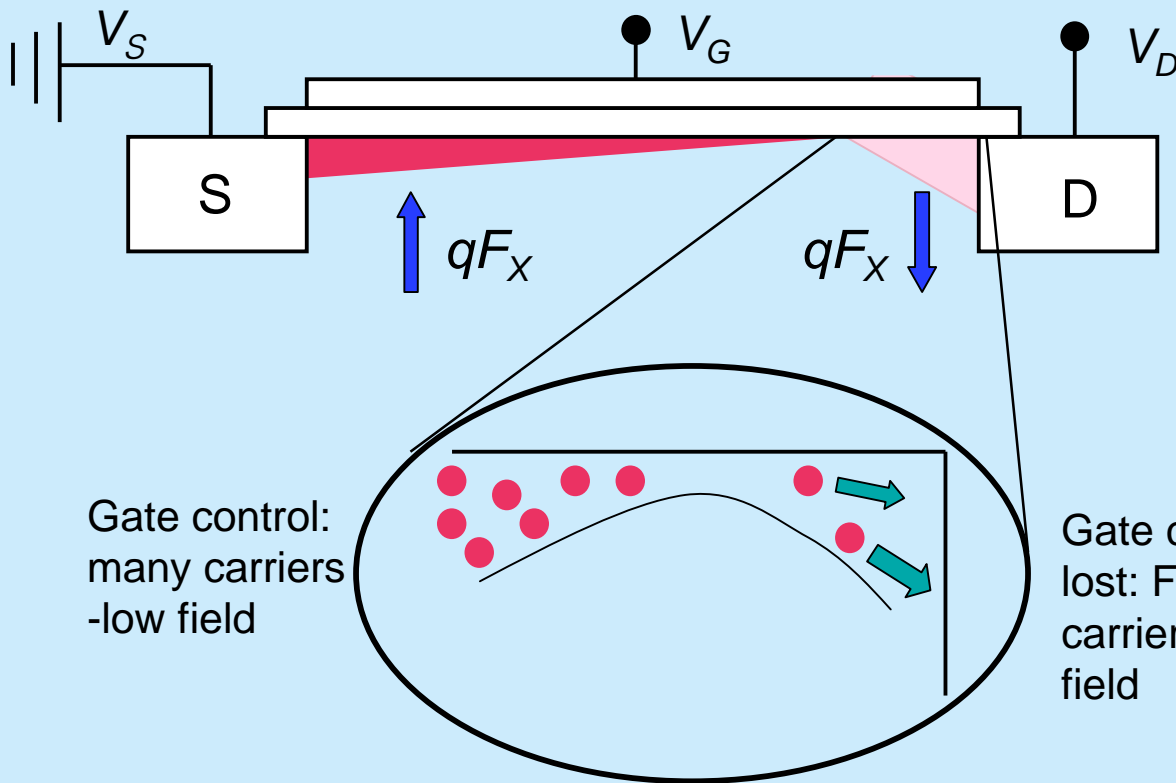


$$Q_n(y) = -C_{ox} [V_G - V_T - V_C(y)]$$

Conditions: $\left| \frac{\partial \phi}{\partial y} \right| \ll \left| \frac{\partial \phi}{\partial x} \right|$ or $|E_y| \ll |E_x|$ $\phi(x,y)$: electrostatic potential

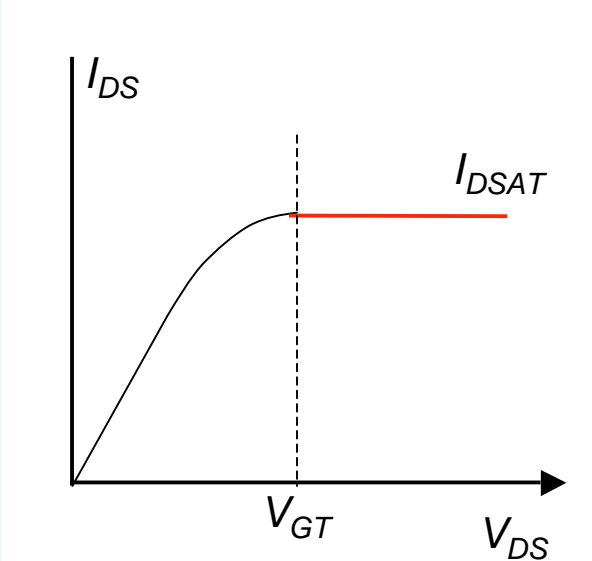


Pinch-Off and Saturation ($V_{GT} < V_{DS}$)

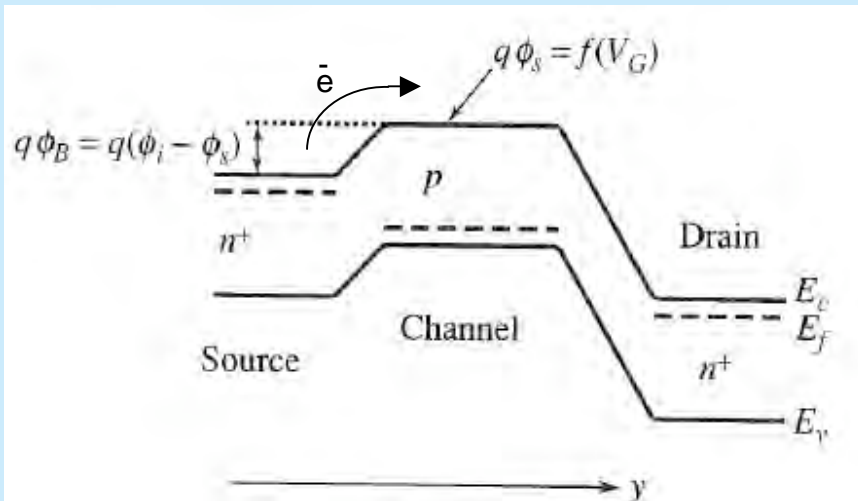


$$I_{DS} = qWn(y)v(y): \text{constant}$$

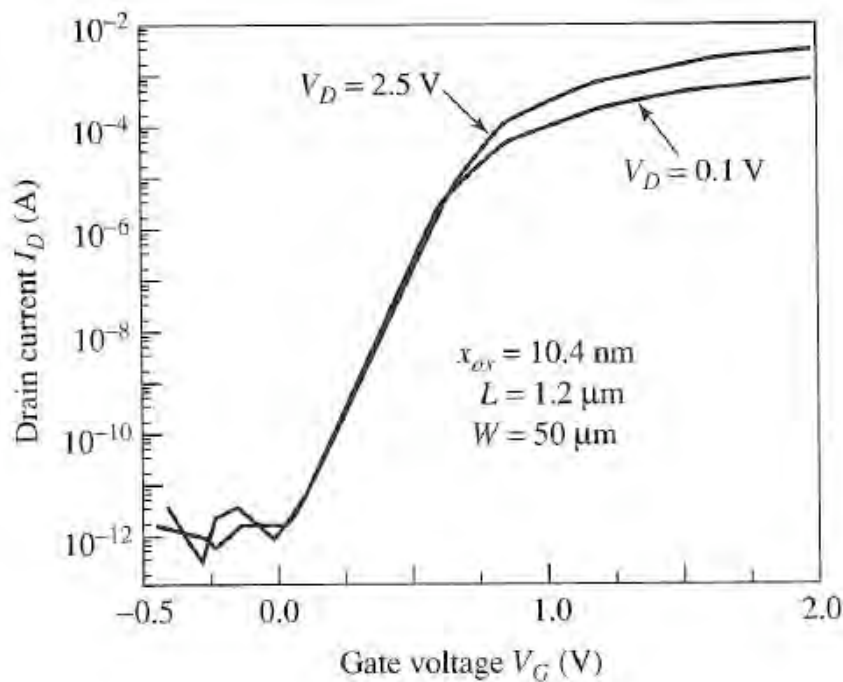
$$I_{DSAT} = \frac{W}{2L} C_{ox} \mu (V_G - V_T)^2$$



Sub-Threshold Conduction*



$$n_s \propto \exp\left(-\frac{q\phi_B}{kT}\right)$$



Normal conduction

Sub-threshold conduction

$$I_D \approx I_{D0} \exp\left(\frac{qV_{GS}}{nkT}\right)$$

(Diffusion)

*After R.S. Muller and T.I Kamins, DEIC, Wiley, 3d ed



MOSFET Scaling (Constant field)*

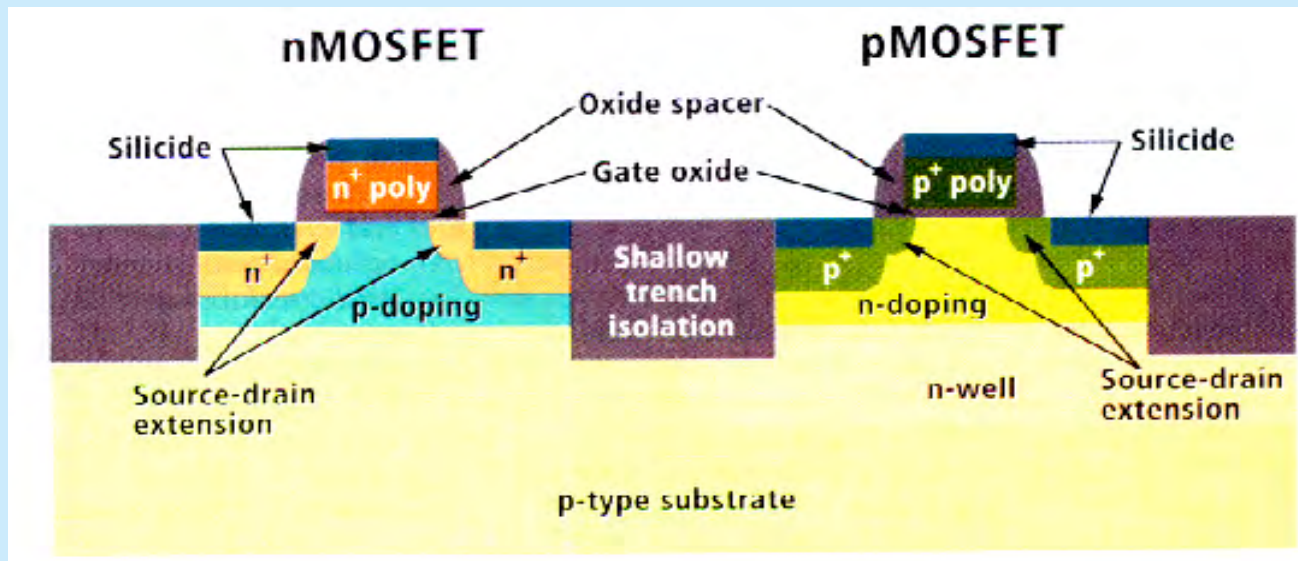
	Device and circuit parameters	Multiplicative factor ($K > 1$)	
Scaling assumptions	Device dimensions (L, W, t_{ox})	$1/K$	
	Doping concentration (N_a, N_d)	K	
	Voltage (except V_T)	$1/K$	
Derived scaling: Device parameters	Electric fields	1	$W_d = \sqrt{\frac{2\epsilon_0\epsilon_s\phi_{depl}}{qN_a}}$
	Carrier velocity	1	
	Depletion layer width (W_d)	$1/K$	
	Capacitance ($C = \epsilon A/t$)	$1/K$	
	Inversion layer charge density	1	
	Current, drift	$1/K$	
	Channel resistance	1	
Derived scaling: Circuit parameters	Circuit delay time ($\tau \sim CV/I$)	$1/K$	<div style="border: 1px solid red; padding: 5px; display: inline-block;">Down scaling of circuit parameters</div>
	Power dissipation ($P \sim VI$)	$1/K^2$	
	Power-delay product ($P\tau$)	$1/K^3$	
	Circuit density ($\sim 1/A$)	K^2	
	Power density (P/A)	1	

*After Y. Taur and T.H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge, 2d edition

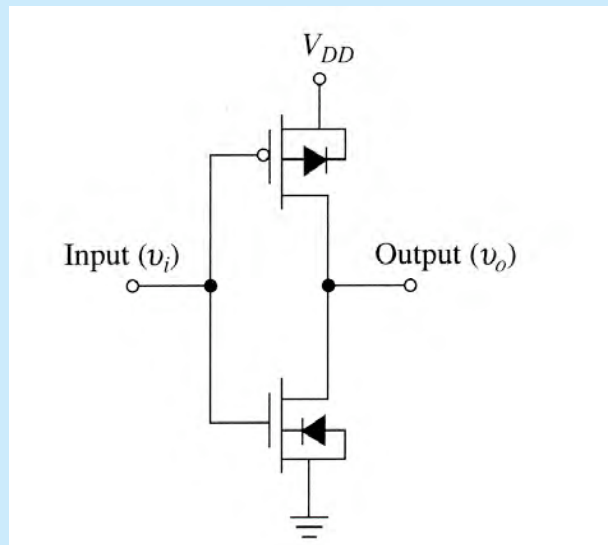
Not scalable: Materials ($E_G, \mu, \text{etc...}$)
Temperature



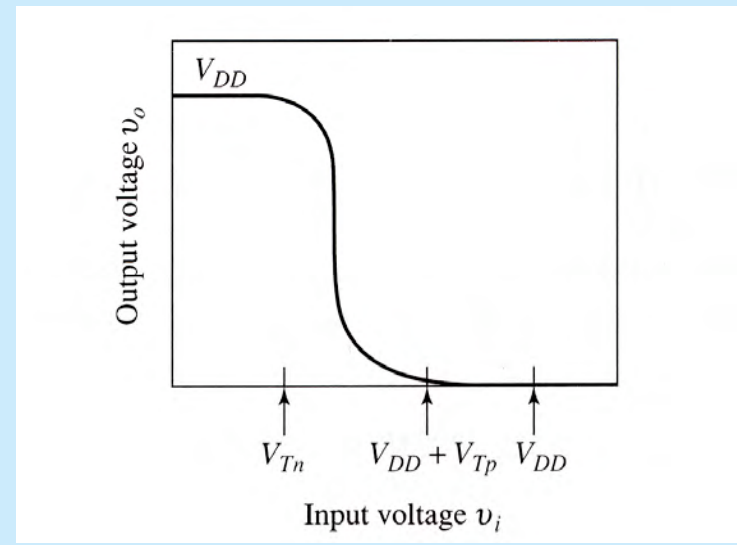
Modern CMOS



CMOS Inverter circuit*

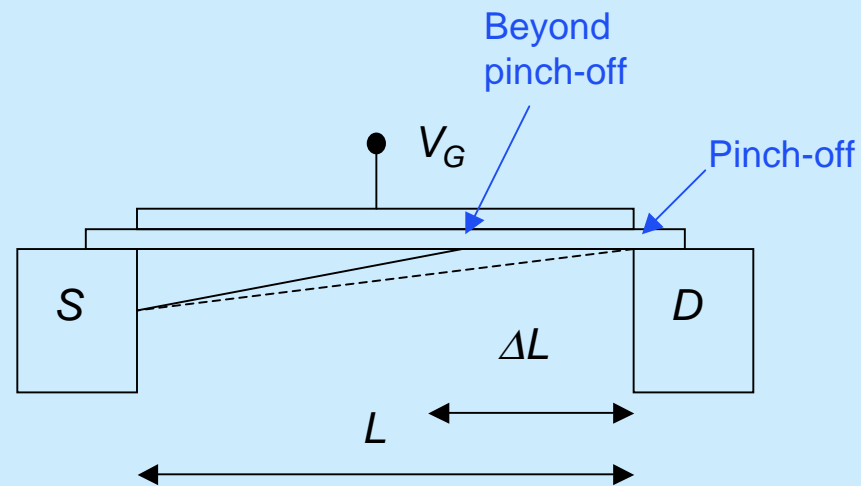
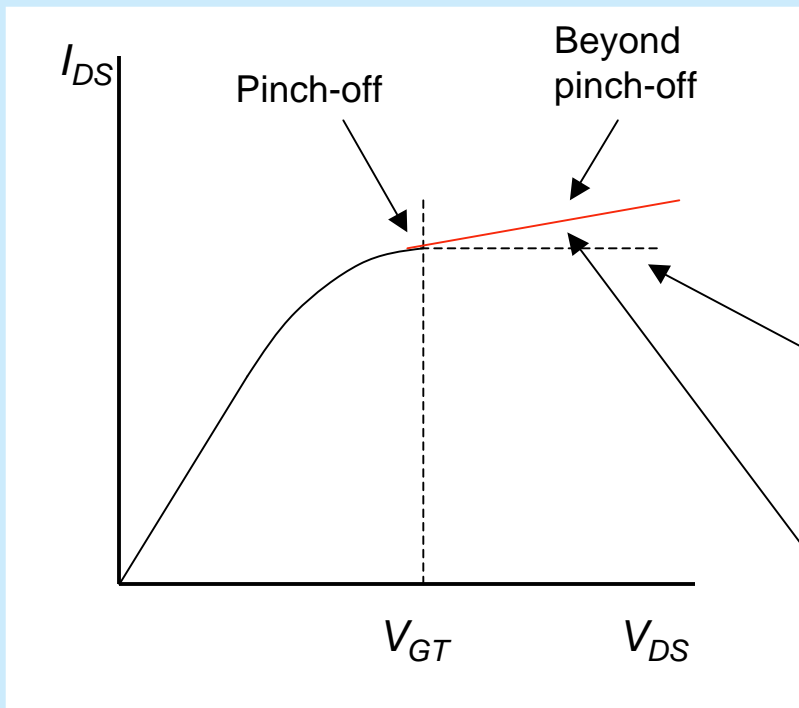


Transfer characteristics*



Short Channel Effects

Channel-length modulation

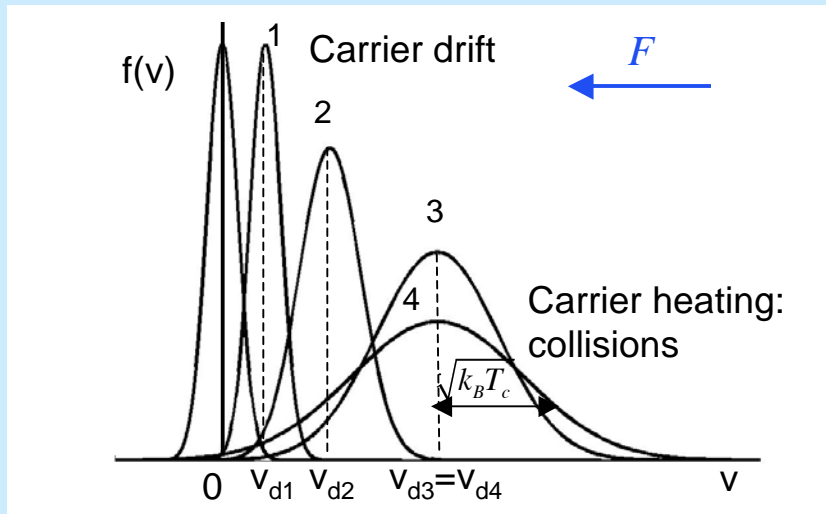


$$I_{DSAT} = \frac{W}{2L} C_{ox} \mu (V_G - V_T)^2$$

$$I'_{DSAT} = \frac{W}{2(L - \Delta L(V_G))} C_{ox} \mu (V_G - V_T)^2 > I_{DSAT}$$

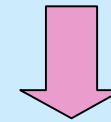


Velocity Saturation (Si-Devices)



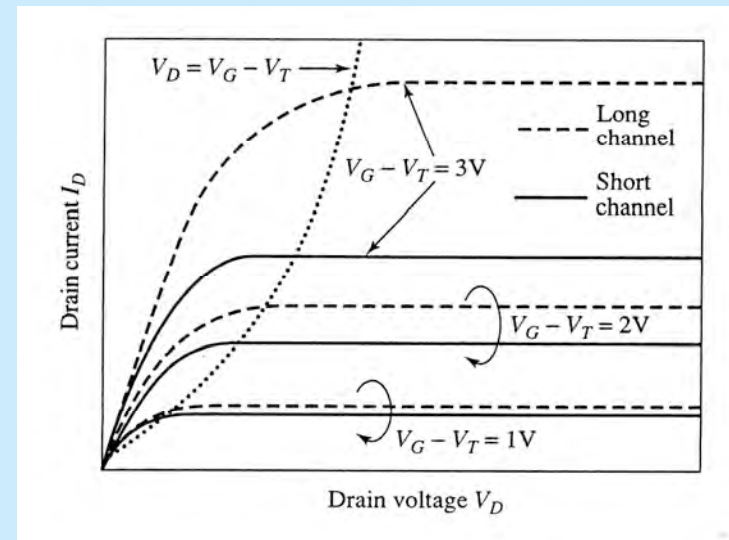
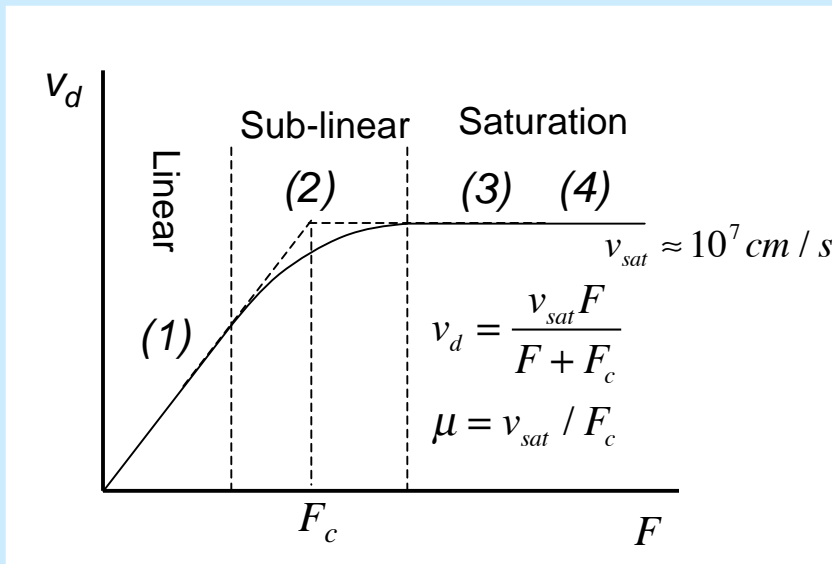
Consequence for MOS Devices

$$I_{DS} = \frac{W}{L} C_{ox} \mu [(V_G - V_T) V_{DS} - V_{DS}^2 / 2]$$



$$I_{DS} = \frac{W}{L + (V_{DS} / F_c)} C_{ox} \mu [(V_G - V_T) V_{DS} - V_{DS}^2 / 2]$$

Velocity saturation induced current reduction



Gate-Induced Mobility Degradation

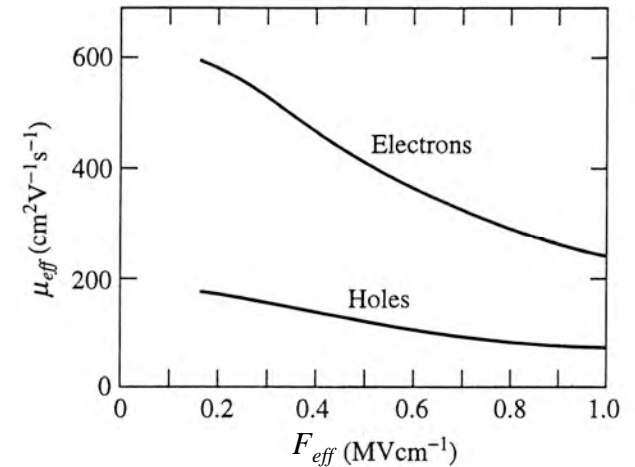
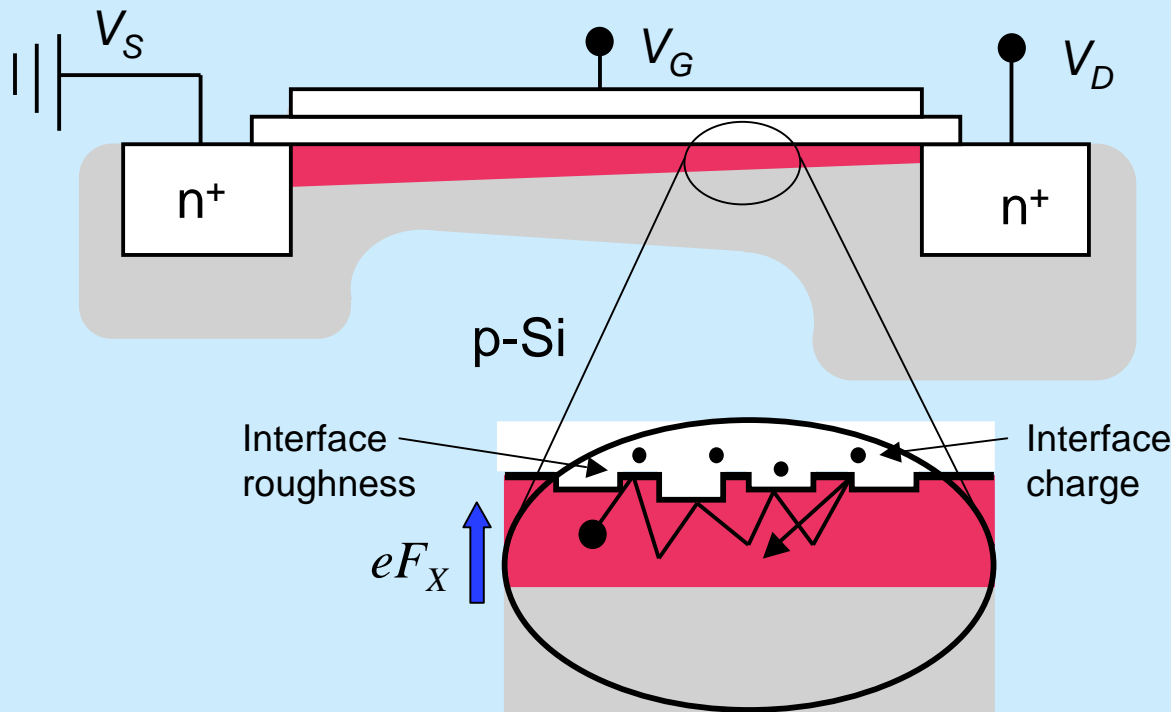


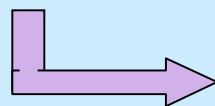
TABLE 9.3 Parameters for effective mobility
© 1986 IEEE [13]

	Unit	Electron (surface)	Hole (surface)	Hole (subsurface)
μ_0	$\text{cm}^2/\text{V}\cdot\text{s}$	670	160	290
F_0	MV/cm	0.67	0.7	0.35
ν		1.6	1.0	1.0

R.S. Muller and T.I Kamins, DEIC, Wiley, 3d ed.

$$F_{eff} = -\frac{1}{\epsilon_0 \epsilon_s} \left(Q_d + \frac{Q_n}{2} \right)$$

$$\mu_{eff} = \frac{\mu_0}{1 + (F_{eff} / F_0)^\nu} \quad \text{with } \mu_0, F_0 \text{ and } \nu \text{ fitting parameters}$$

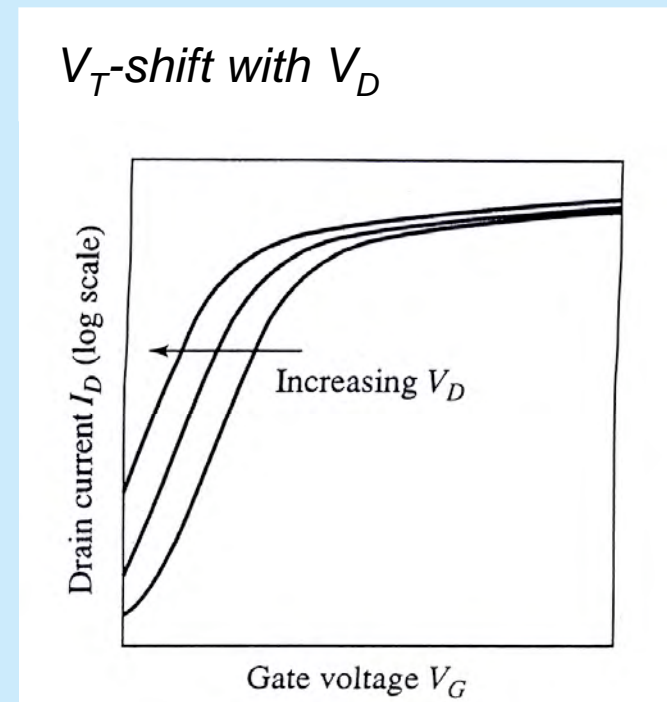
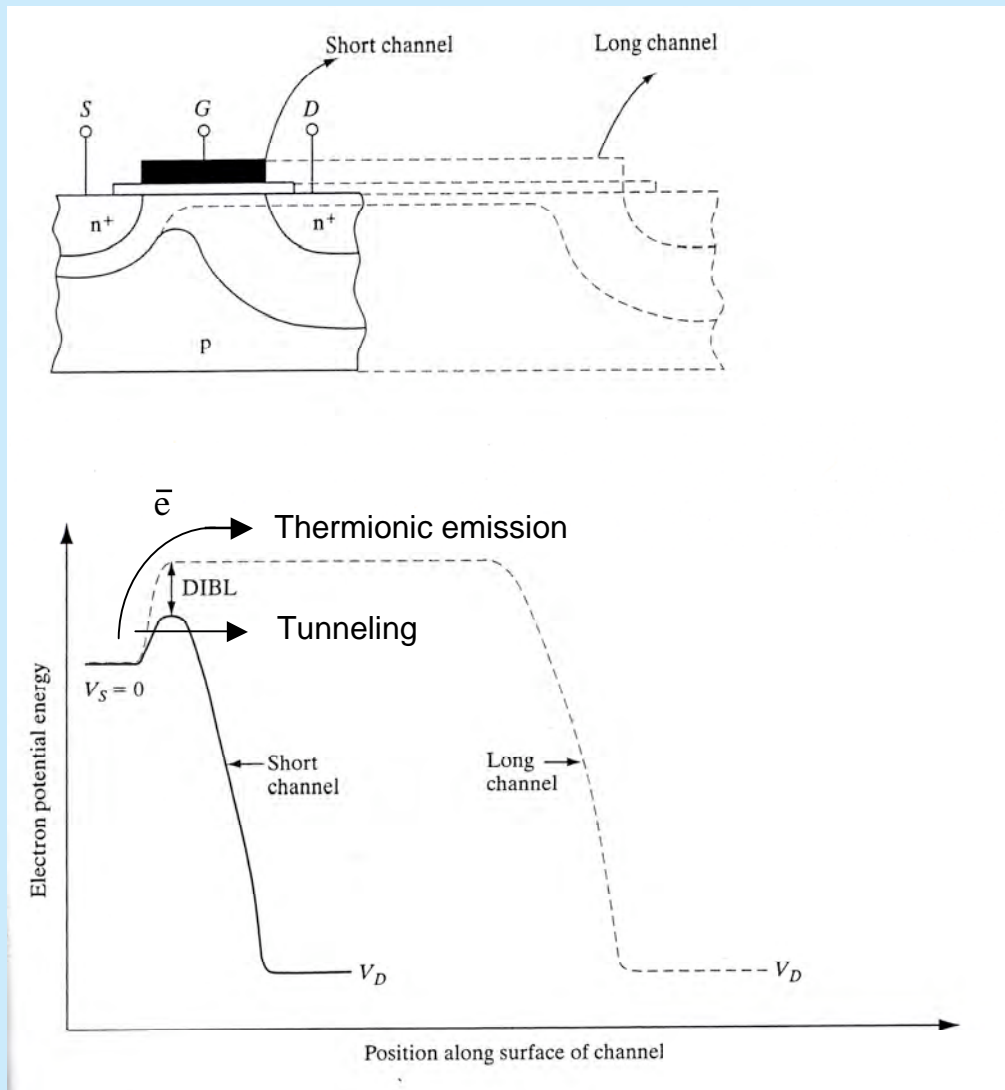


$$\mu_{eff} = \frac{\mu_0}{1 + \theta(V_G - V_T)}$$

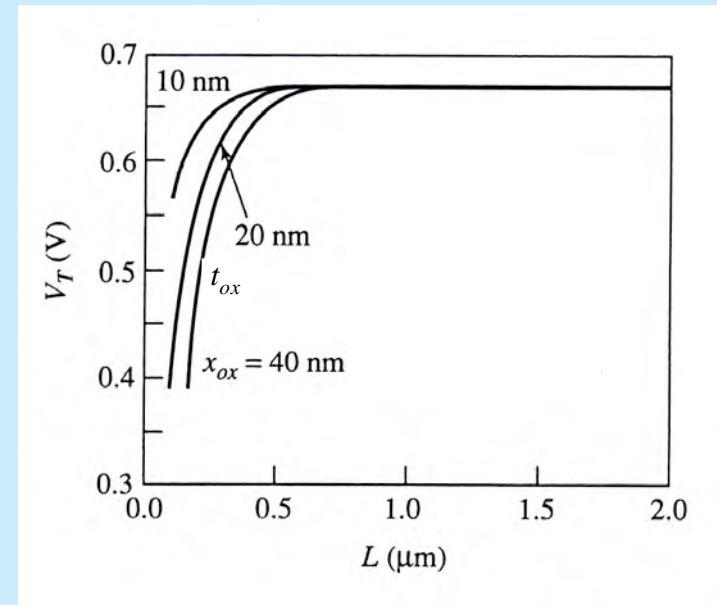
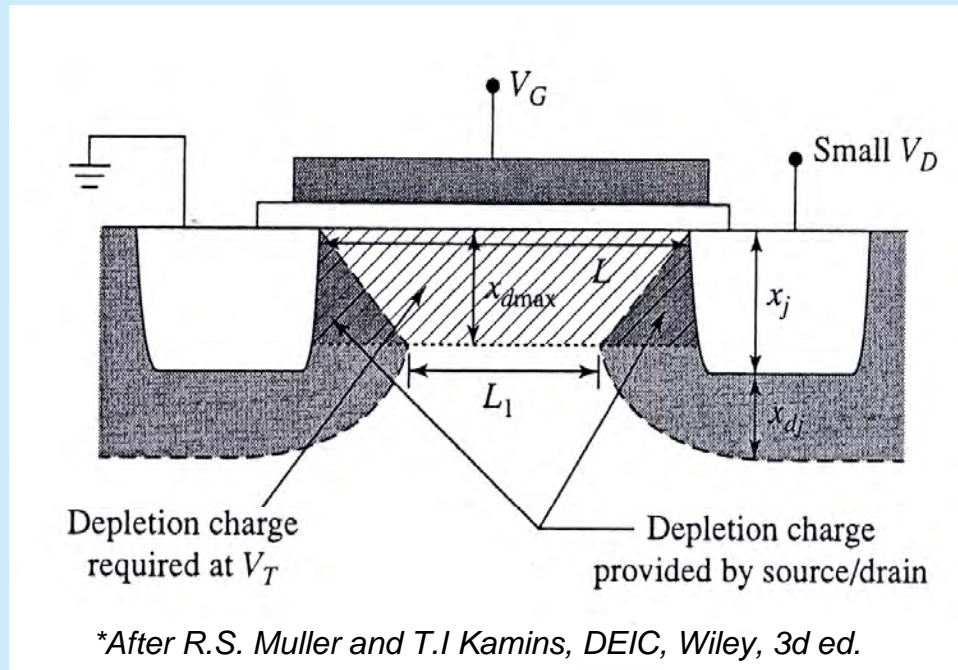
For simulation purpose



Drain-Induced Barrier Lowering (DIBL)*



Source-Drain Charge Sharing Effect: V_T (Gate coupling)-Reduction*



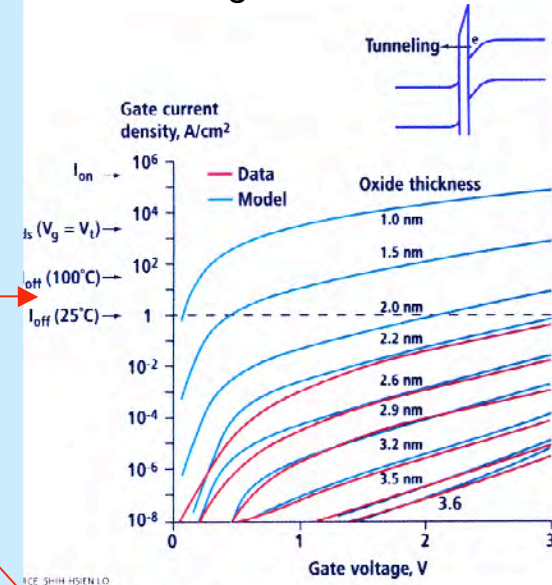
Deep Nanoscale Devices

TABLE 9.2 Past and Predicted Technology Scaling Trends for MOS Technology, from International Technology Roadmap for Semiconductors (1997-2001 editions) [3]

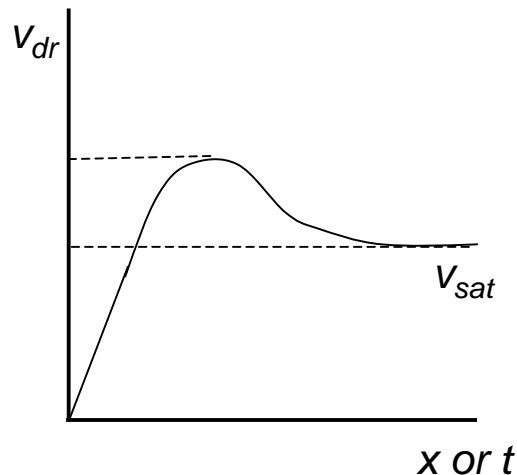
Year of Production	1997	1999	2001	2003	2006	2010	2016
Min. dim. L (μm)	0.25	0.18	0.13	0.1	0.07	0.045	0.022
DRAM density (Gbits/cm ²)	0.18	0.38	0.42	0.91	1.85	4.75	28.85
Logic V_{DD} (V)	2.5-1.8	1.8-1.5	1.2	1.0	0.9	0.6	0.4
Equivalent x_{ox} (nm)	4-5	1.9-2.5	2.3	2.0	1.9	1.2	0.9
Junction depth x_j (nm)	50-100	45-70	30-60	26-52	20-40	15-30	10-20
Local wire pitch (nm)	600	500	350	245	130	105	30
Metal aspect ratio	1.8	2	1.6*	1.6	1.7	1.8	2.0
max. I_{Dsat} (NIMOS)	600	750	900	900	900	900	900
($\mu\text{A}/\mu\text{m}$) PMOS	280	350	420	420	420	420	420

* Switching to copper Manufacturable solution yet to be found.

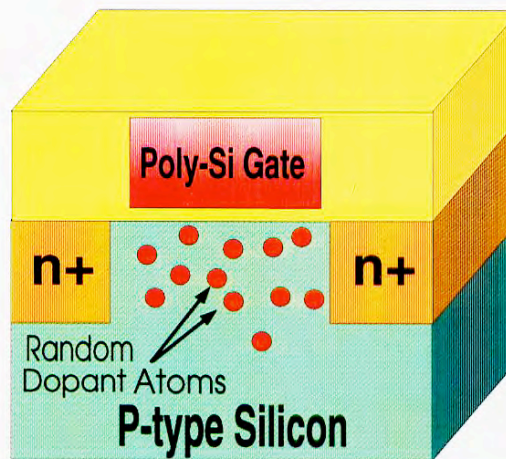
Oxide leakage



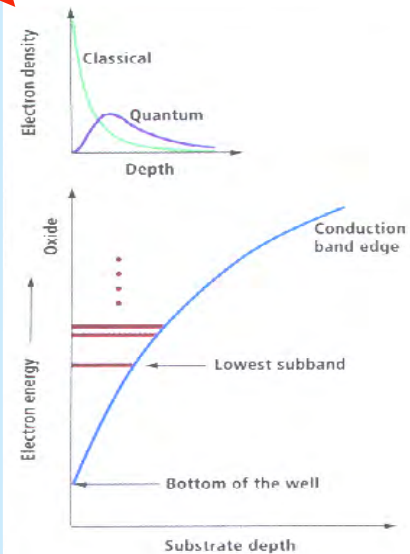
Velocity Overshoot



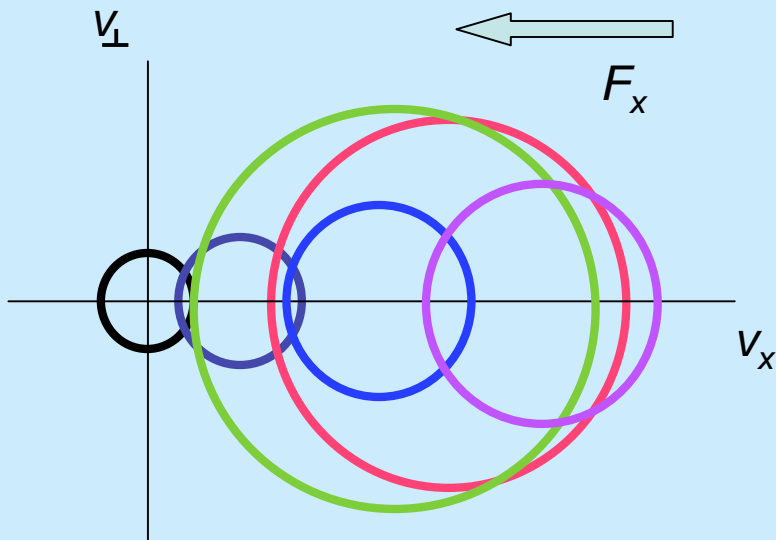
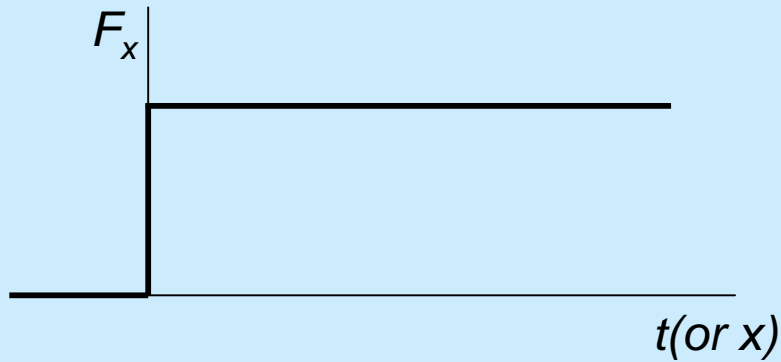
Dopant granularity



Quantum Charge

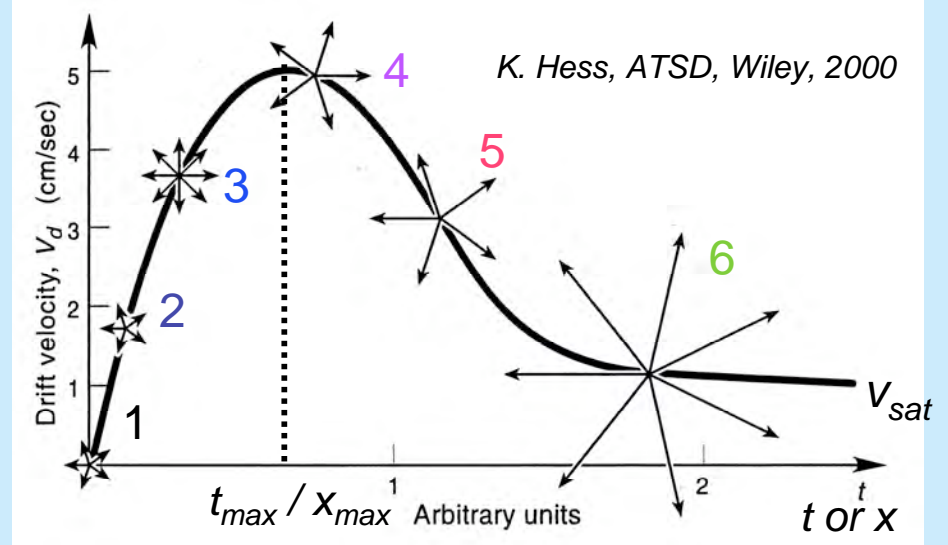


Velocity Overshoot (Transient)



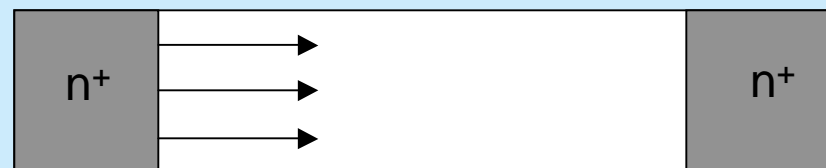
Increasing scattering rates with carrier energy

J.P. Leburton, IWSG-2009, IITB, India



In III-V Compnds : $t_{max} \sim 1\text{ps} \Rightarrow x_{max} \sim 100\text{nm}$
 $v_{max} \sim 4-5 \times 10^7 \text{cm/s}$

In Si: $t_{max} \sim 0.1\text{ps} \Rightarrow x_{max} \sim 10-20\text{nm}$
 $v_{max} \sim 2 \times 10^7 \text{cm/s}$



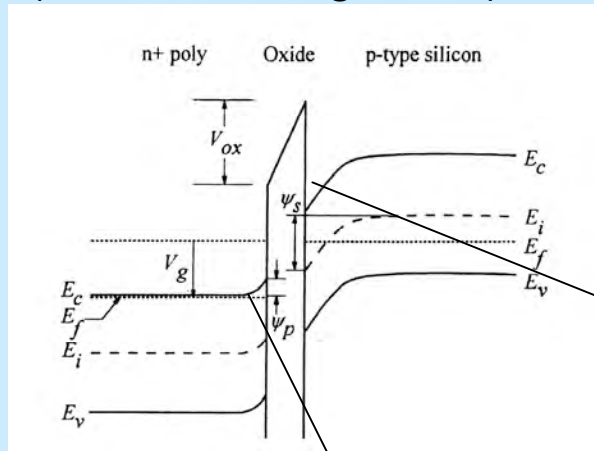
$$L = x_{max}$$

High speed-high current!!

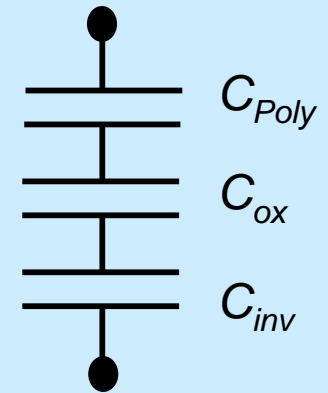
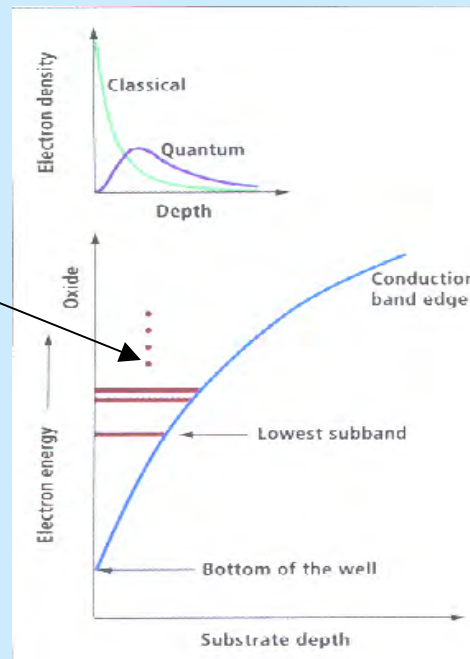


Depletion and Quantum Capacitance: Gate Coupling Reduction

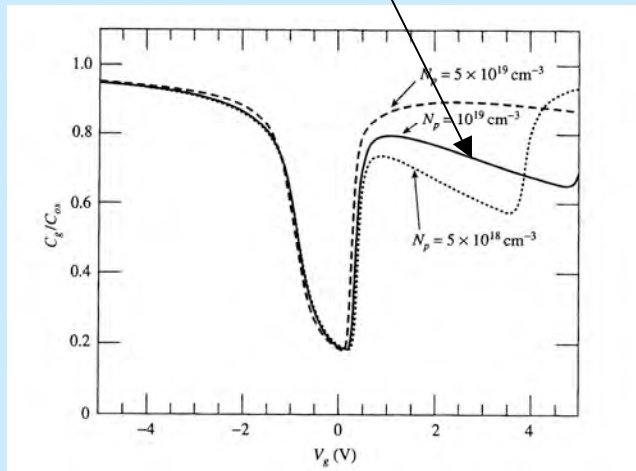
Poly-Si gate*
(All-Si&self-alignment)



Quantized inversion
layer



C-V curve*



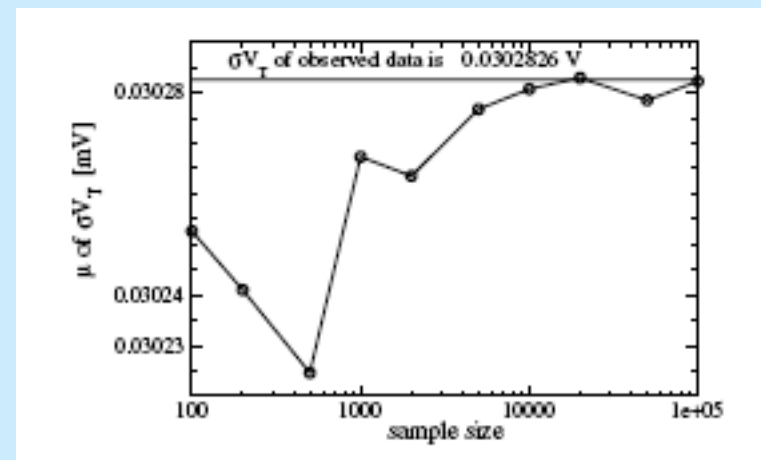
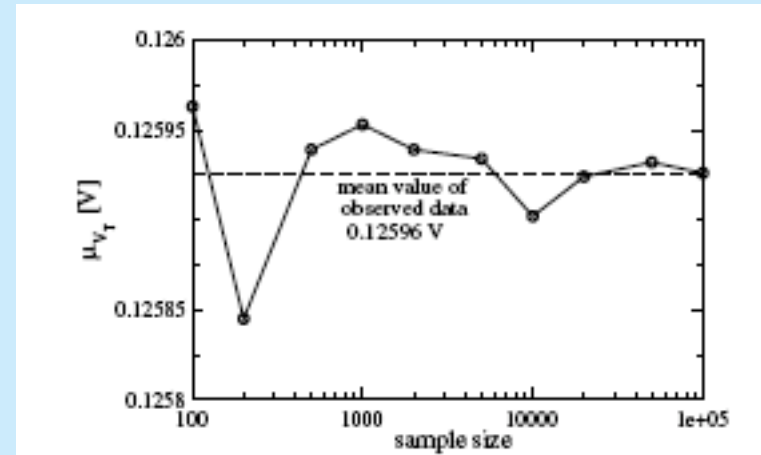
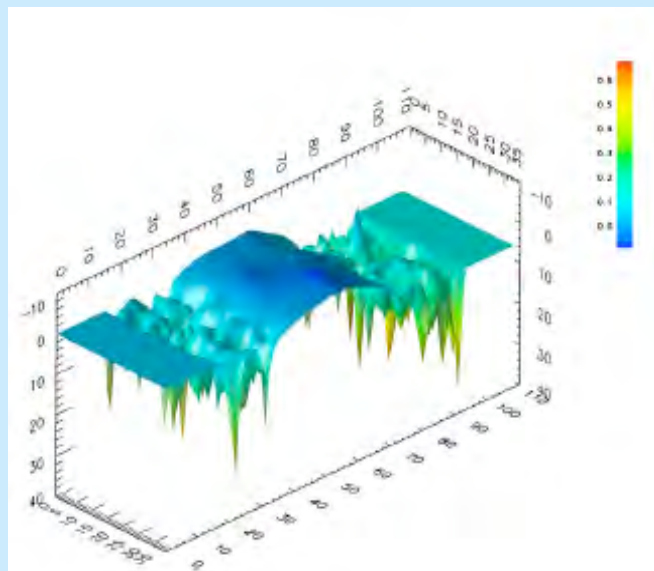
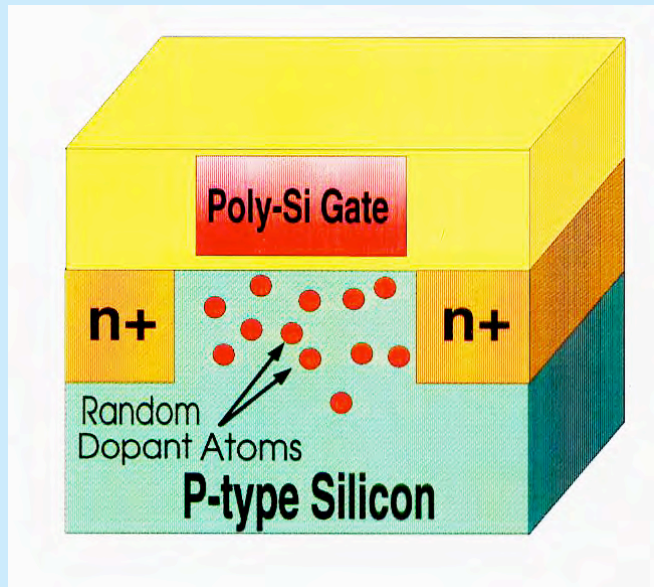
$$\frac{1}{C_g} = \frac{1}{C_{poly}} + \frac{1}{C_{ox}} + \frac{1}{C_{inv}}$$

$$\Rightarrow C_g < C_{ox}$$

*After Y.Taur and T.H. Ning, FMVD, Cambridge, 2d ed.

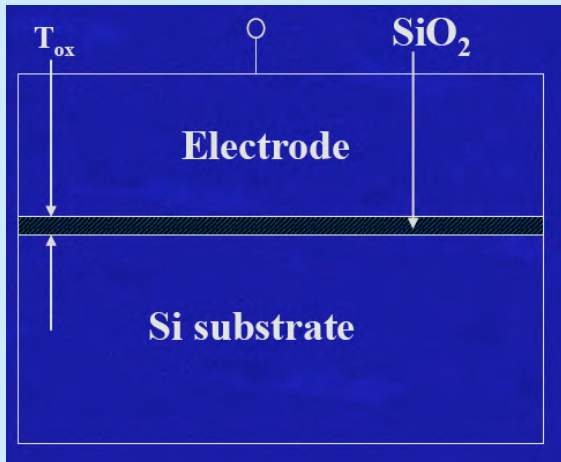


Dopant Granularity: V_T -Fluctuations*



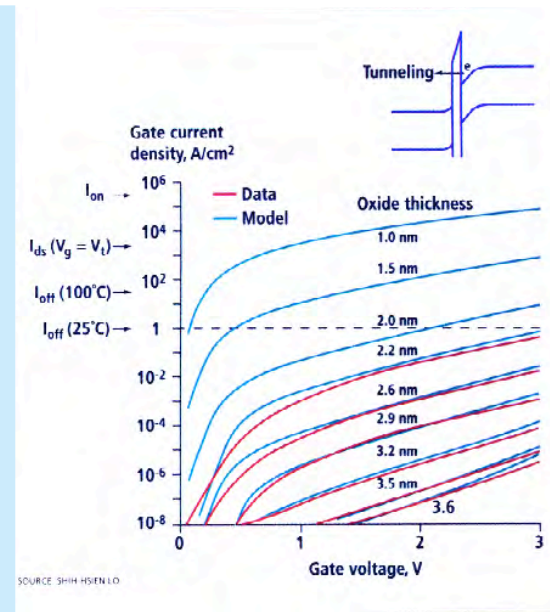
t_{ox} -Scaling => High-K Dielectrics*

$t_{ox} \downarrow$
 $C_{ox} = \frac{\epsilon_0 \epsilon_{ox}}{t_{ox}} \uparrow$



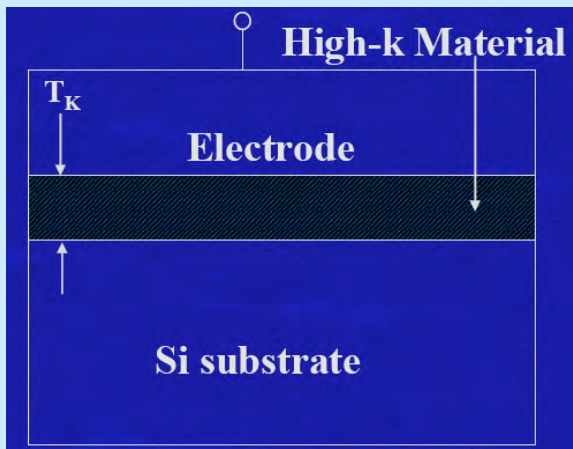
But

Tunneling-induced dissipation

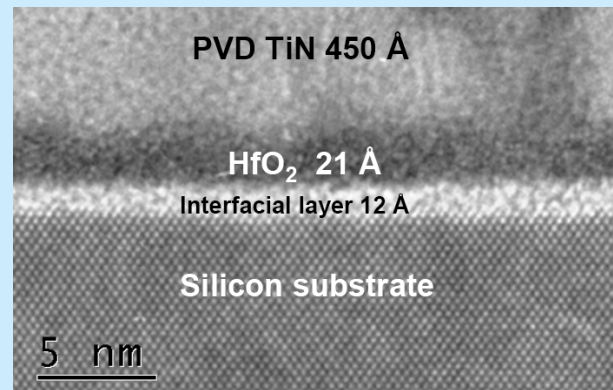


High-K dielectrics

$$C_{ox} = \frac{\epsilon_0 \epsilon_{SiO_2}}{t_{SiO_2}} = \frac{\epsilon_0 \epsilon_{high-K}}{t_{high-K}}$$



*P. Zeitzoff and H. Huff, 2005 ICCMUT, Dallas, TX



$$t_{high-K} = (\epsilon_{high-K} / \epsilon_{SiO_2}) t_{SiO_2} \gg t_{SiO_2}$$

Reduces Tunneling



High-K Dielectric Phonons

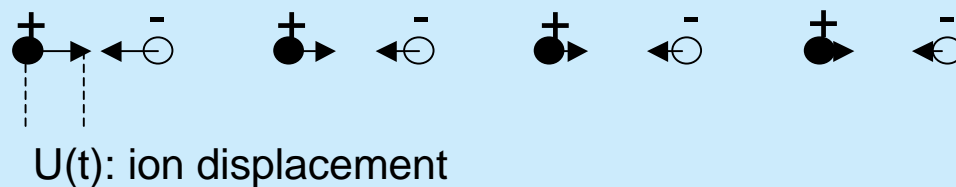
High-K: Large $\epsilon \Rightarrow$ large polarization \vec{P}

$$\vec{P} = \vec{P}_{\text{ionic}} + \vec{P}_{\text{electronic}}$$

Me/Si-O bond \nearrow $\propto E_G^{-n}$ (direct)

negligible in insulators (large E_G)

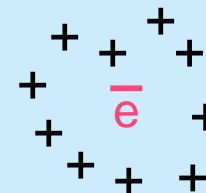
Polar Optic Phonons



Si-O bond: strong \rightarrow "hard" phonons $\left\{ \begin{array}{l} \text{High energy} \\ \text{Low } \epsilon_0 \end{array} \right.$

Me-O bond: weaker \rightarrow "soft" phonons $\left\{ \begin{array}{l} \text{Low energy} \\ \text{Large } \epsilon_0 \end{array} \right.$

Electron-phonon interaction



Interaction strength (Frohlich)

$$\alpha \propto \hbar \omega_{SO} \left[\frac{1}{\epsilon_{ox}^{\infty}} - \frac{1}{\epsilon_{ox}^0} \right] \propto P^2$$

Electronic contribution (fast)

Ionic contribution (slow)

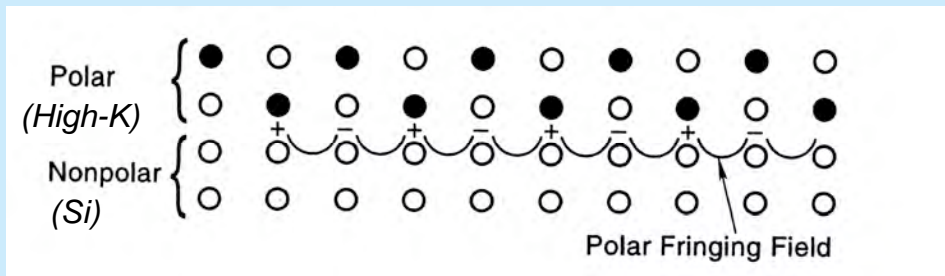
Quantity (units)	Material					
	SiO ₂ ^a	Al ₂ O ₃ ^b	AlN ^c	ZrO ₂ ^{d-f}	HfO ₂ ^{f,g}	ZrSiO ₄ ^h
ϵ_{ox}^0 (ϵ_0)	3.90	12.53	9.14	24.0 ⁱ	22.00	11.75
ϵ_{ox}^i (ϵ_0)	3.05	7.27	7.35	7.75	6.58	9.73
ϵ_{ox}^{∞} (ϵ_0)	2.50	3.20	4.80	4.00	5.03	4.20
ω_{TO1} (meV)	55.60	48.18	81.40	16.67	12.40	38.62
ω_{TO2} (meV)	138.10	71.41	88.55	57.70	48.35	116.00
α_1	0.0248	0.0788	0.0248	0.2504	0.3102	0.0322
α_2	0.0113	0.0814	0.0423	0.0779	0.0362	0.2942

M. Fischetti et al., JAP 90, 4587 (2001)



High-K Dielectric Remote Phonons

Remote Interface Phonons



K. Hess, ATSD, Wiley, 2000

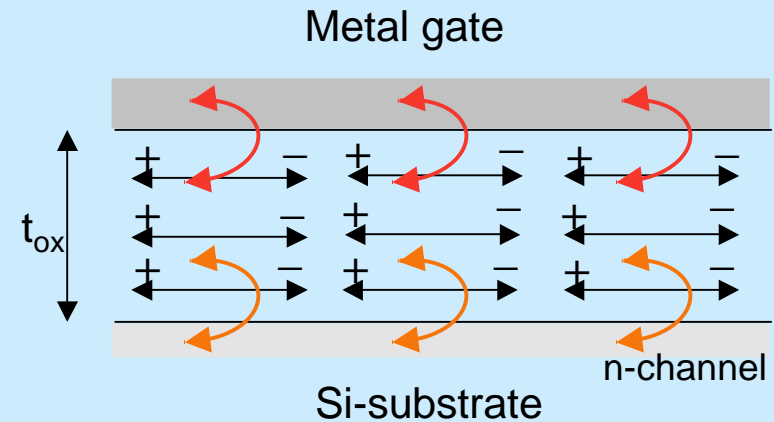
Interaction between electron in Si and remote phonons in High-K dielectric !!!!

Interaction strength
(image charge)

$$\alpha \propto \hbar\omega_{SO} \left[\frac{1}{\epsilon_{ox}^{\infty} + \epsilon_{Si}^{\infty}} - \frac{1}{\epsilon_{ox}^0 + \epsilon_{Si}^0} \right]$$

Q. Wang & G.D. Mahan, PRB 6, 4517 (1972)

Plasmon-RIP coupling*



*M. Fischetti et al., JAP 90, 4587 (2001)

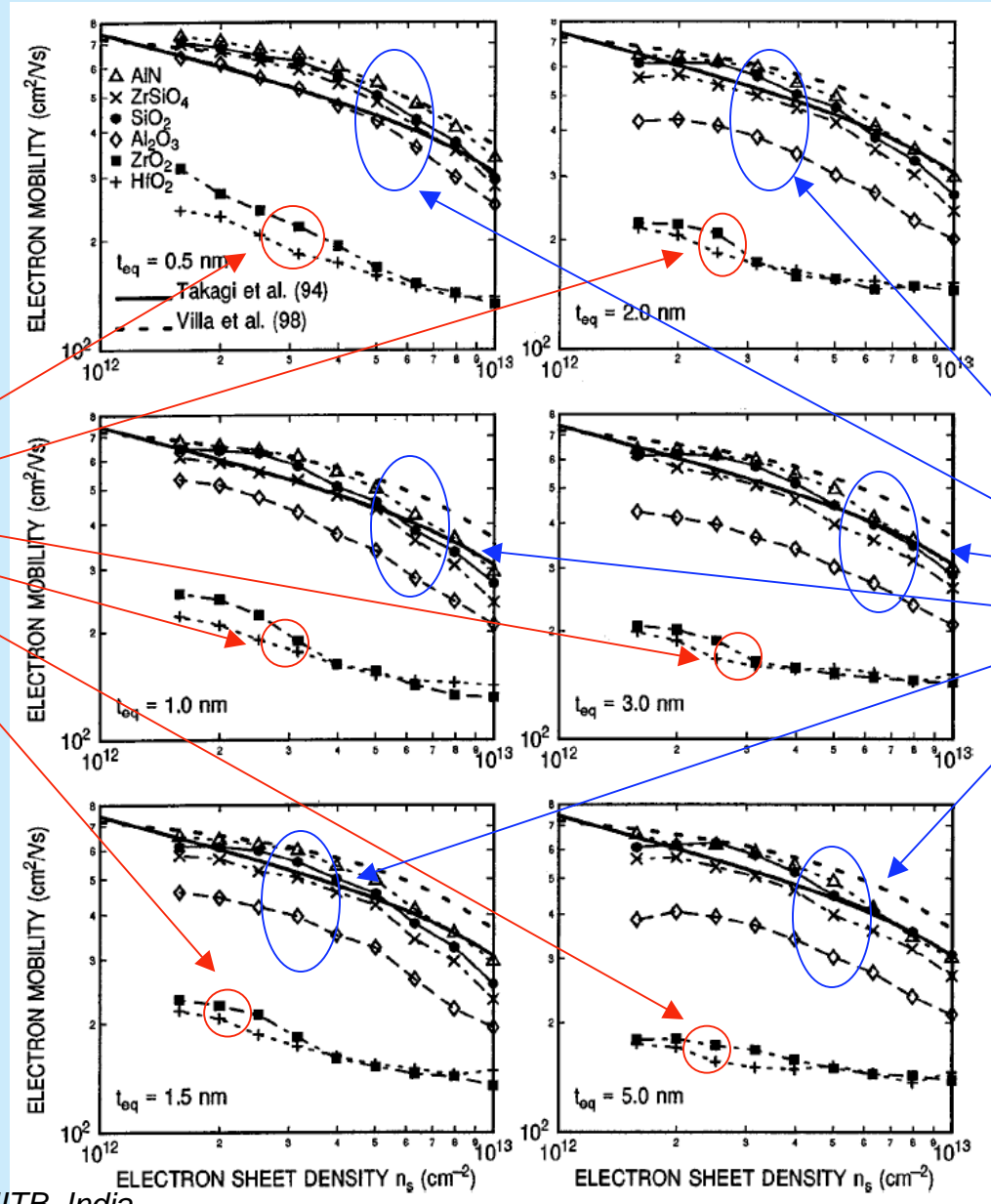
Quantity (units)	Material					
	SiO ₂ ^a	Al ₂ O ₃ ^b	AlN ^c	ZrO ₂ ^{d-f}	HfO ₂ ^{f,g}	ZrSiO ₄ ^h
ϵ_{ox}^0 (ϵ_0)	3.90	12.53	9.14	24.0 ⁱ	22.00	11.75
ϵ_{ox}^i (ϵ_0)	3.05	7.27	7.35	7.75	6.58	9.73
ϵ_{ox}^{∞} (ϵ_0)	2.50	3.20	4.80	4.00	5.03	4.20
ω_{TO1} (meV)	55.60	48.18	81.40	16.67	12.40	38.62
ω_{TO2} (meV)	138.10	71.41	88.55	57.70	48.35	116.00
α_1	0.0248	0.0788	0.0248	0.2504	0.3102	0.0322
α_2	0.0113	0.0814	0.0423	0.0779	0.0362	0.2942

weak

strong



High-K Dielectric Remote Phonon Scattering



Strong RIP scattering (ZrO₂&HfO₂)

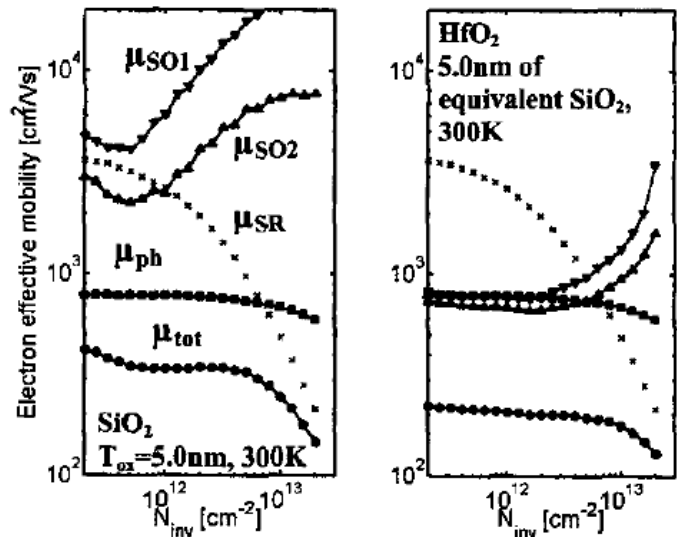
Weak (bare or plasmon screened) RIP scattering

RIP-Limited Channel Mobility: SiO_2 vs. HfO_2^*

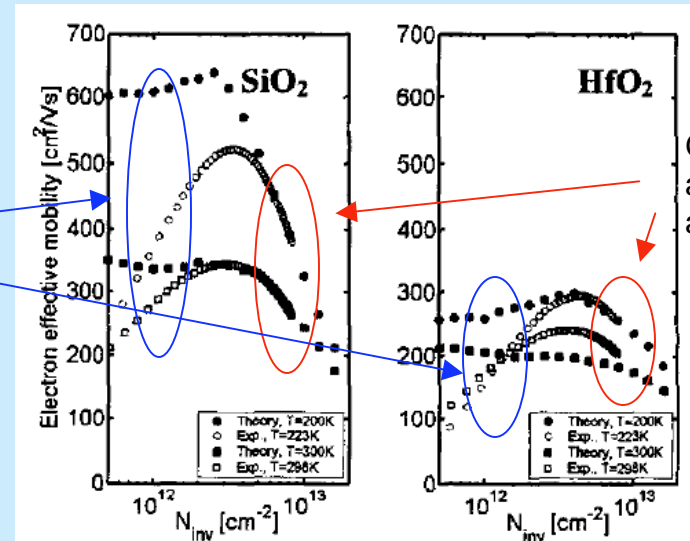
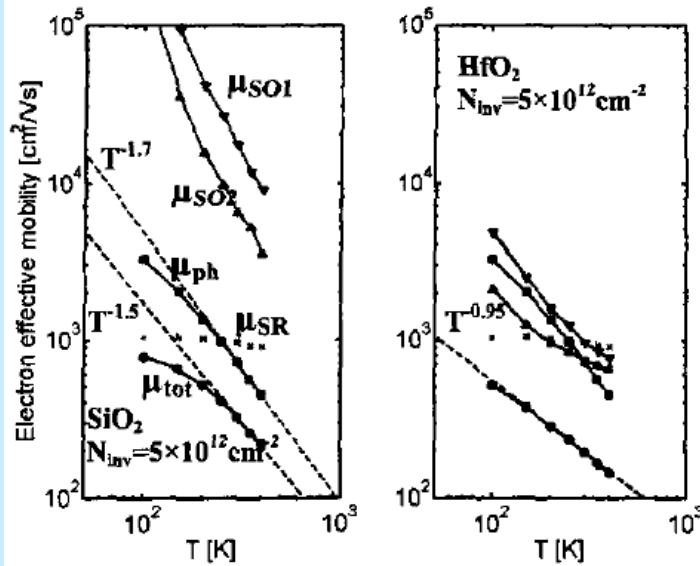
Simulated

Theory vs Experiment

N_s -dependence



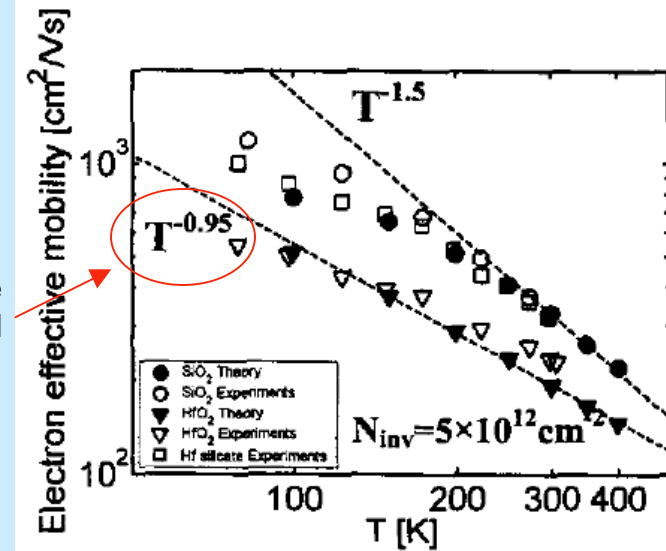
T-dependence



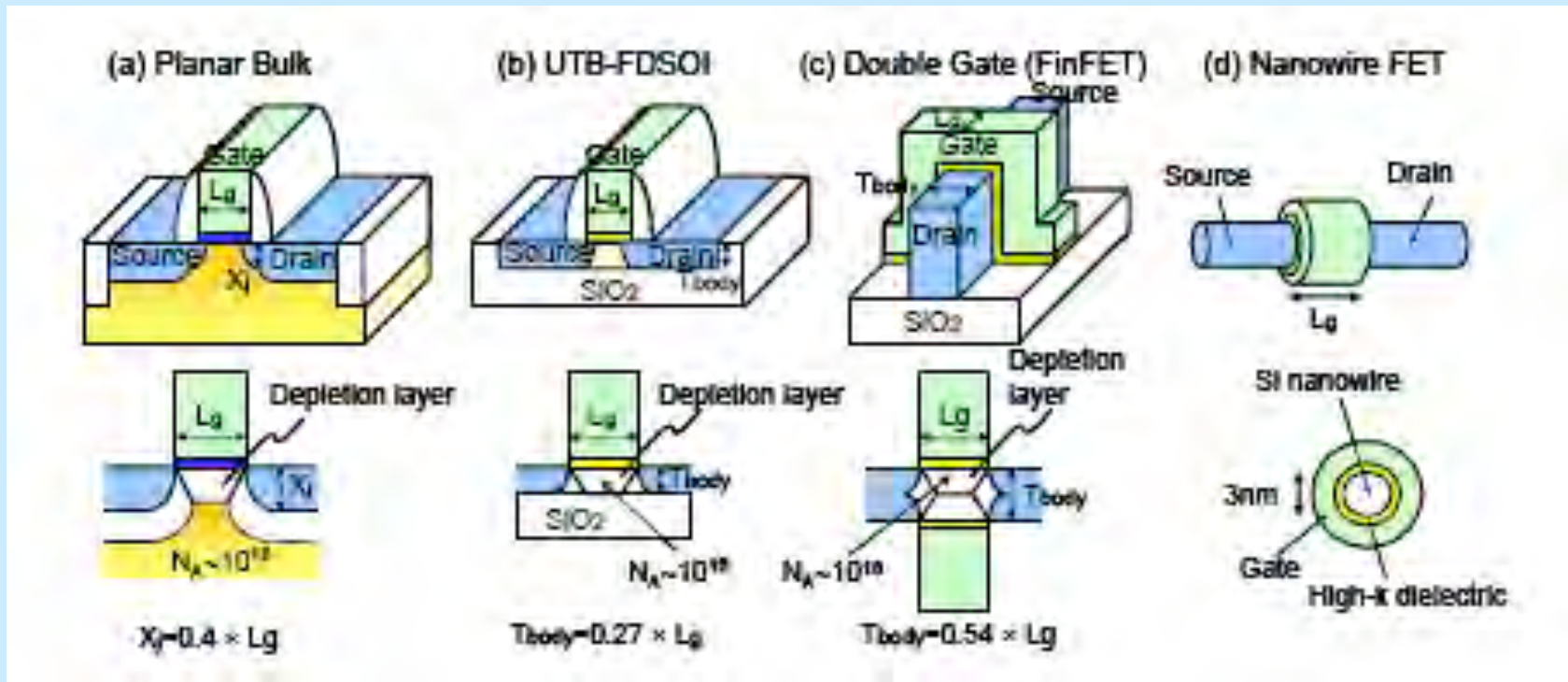
coulomb scattering neglected in the model

Good agreement at high N_s

Weaker T-dependence for Hf-based insulators



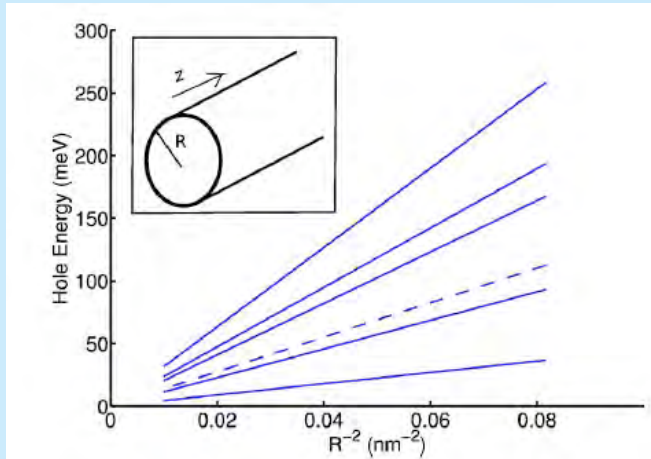
Alternative (Future) MOSFET Structures*



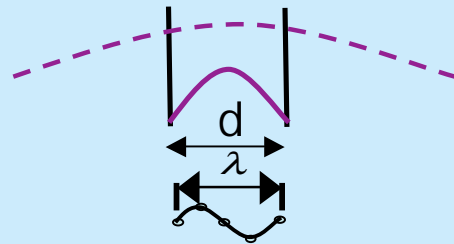
* After K. Imai, Proc. Of SPICE vol. 7028

Depleted devices for - Reduction of V_T -fluctuations
 - "Ballistic" transport
 + III-V on Si for high mobility

Confined Phonons in Quantum Wires*



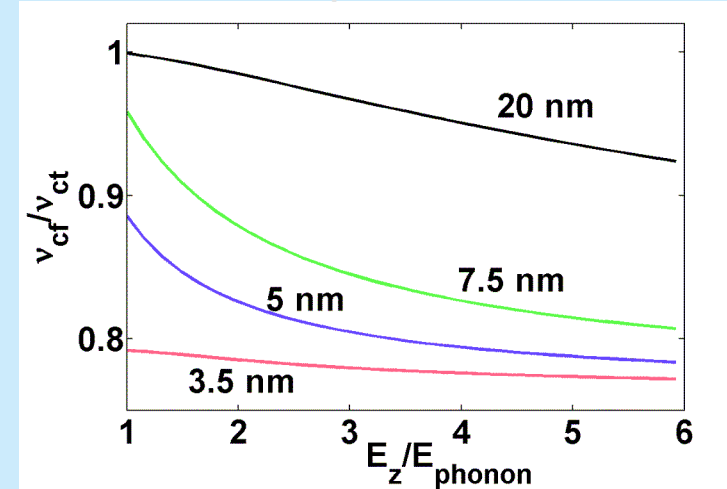
Carrier confinement, but also
phonon confinement $\lambda_{\perp} < 2d$



$$\text{Bulk: } \frac{1}{\tau} \Rightarrow \int_0^{\infty} \dots q_{\perp} dq_{\perp}$$

$$\text{Confined: } \frac{1}{\tau} \Rightarrow \sum_{n=1}^N \dots \rightarrow q_{\perp} = \frac{n\pi}{2R}, R = Na_0$$

Confined/bulk phonon scatt. ratio



Forward/backward scattering ratio

