

Germanium for High Performance MOSFETs and Integrated Optical Interconnects

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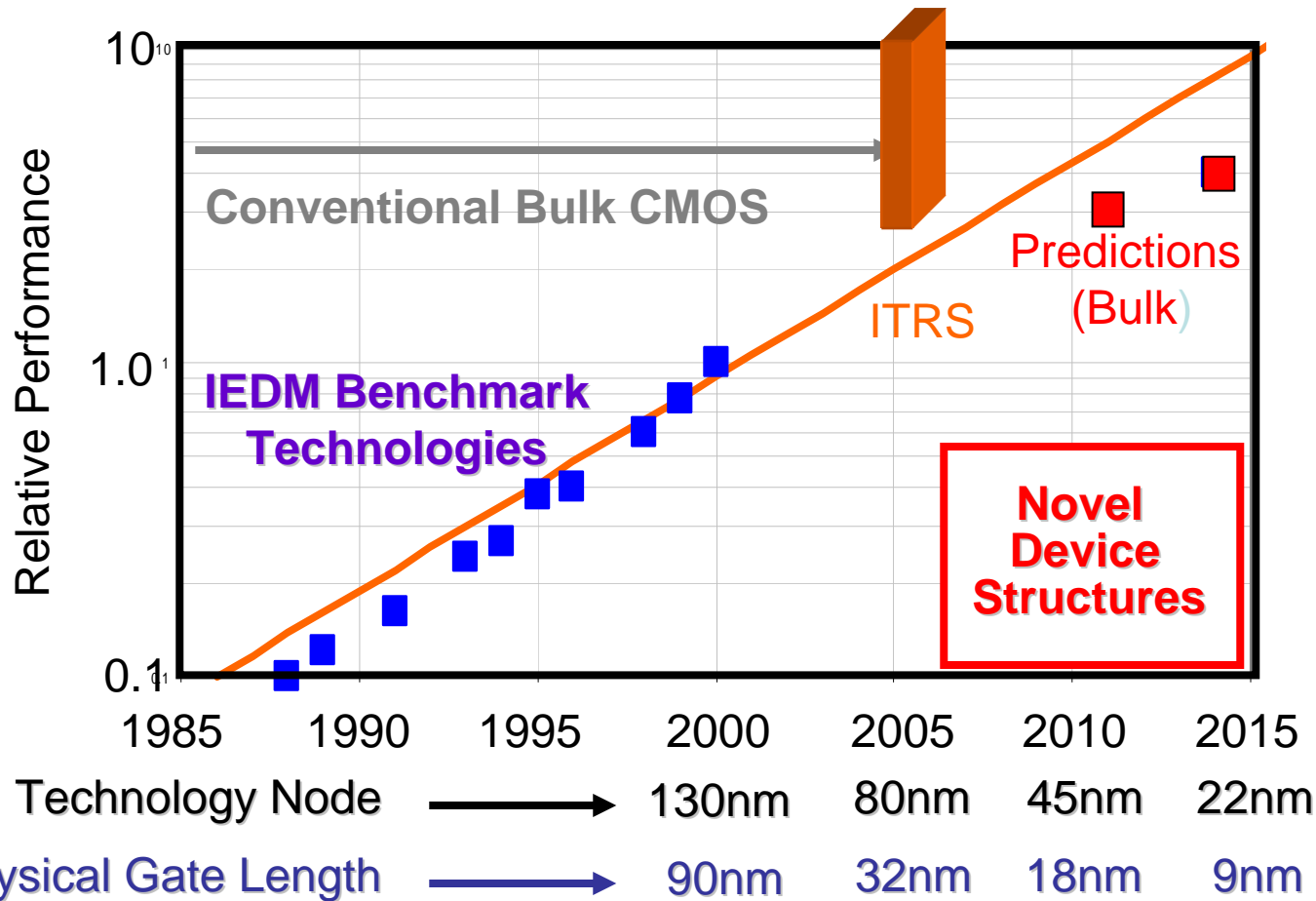
Funding sources: DARPA, MARCO, NSF, SRC and CIS

Research Centers/Programs

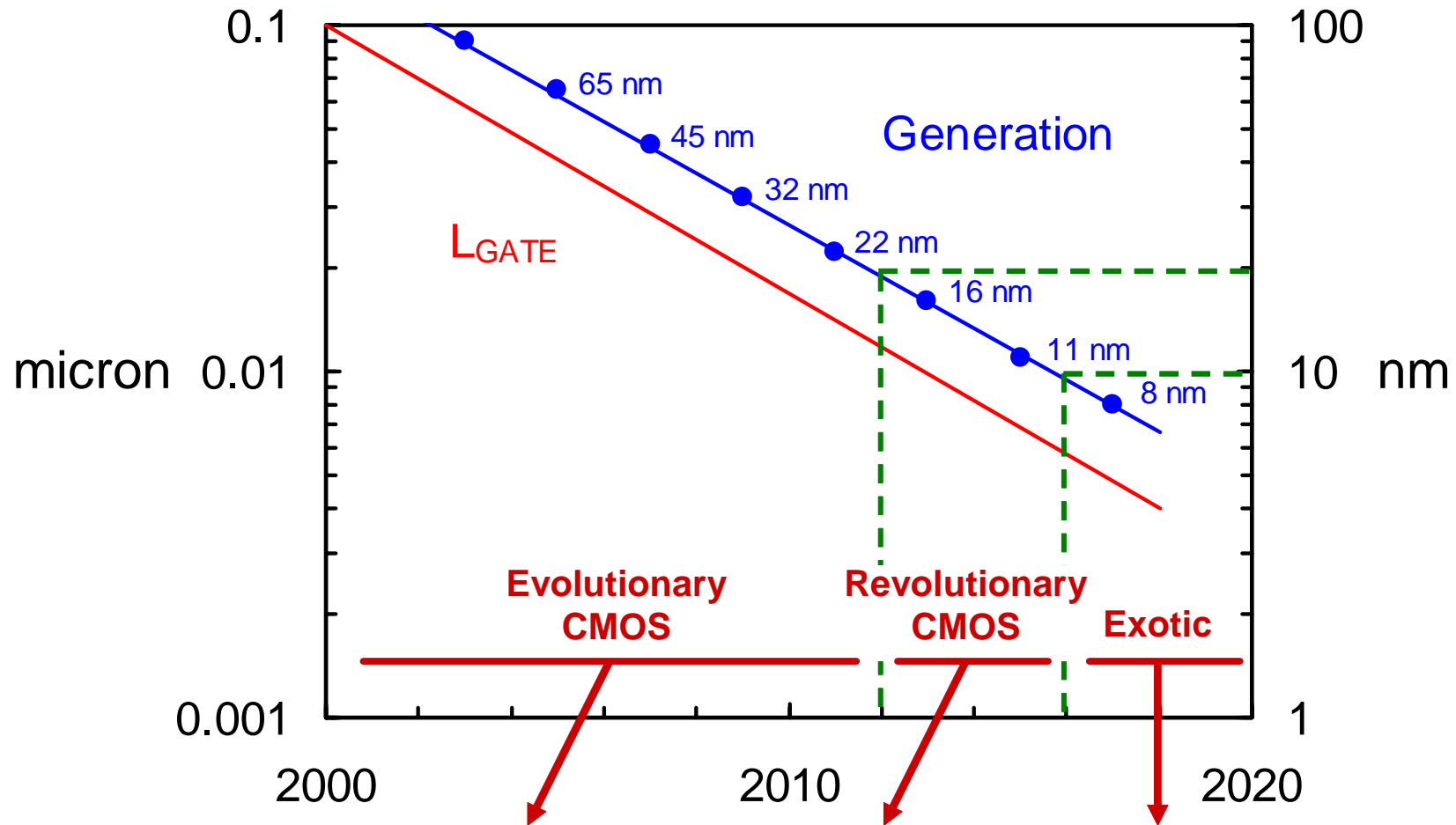
- ❑ MARCO Focus Center for Materials, Structures and nano-Devices
- ❑ MARCO Interconnect Focus Center
- ❑ NSF/SRC Engineering Center for Environmentally Benign Manufacturing of Semiconductors
- ❑ Stanford Center for Integrated Systems
- ❑ DARPA HGI and 3D program

Bulk-Si Performance Trends

- Maintaining historical CMOS performance trend requires new semiconductor material and structures by 2008-2010...
- Earlier if current bulk-Si data do not improve significantly



Nanotechnology Eras

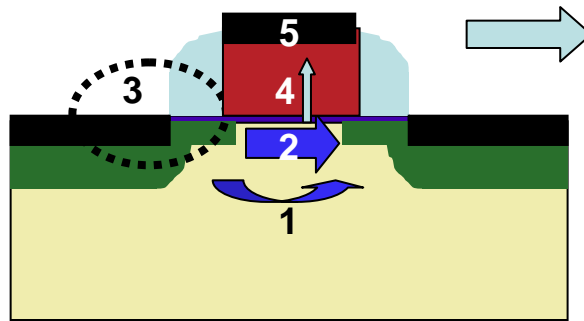


Reasonably Familiar

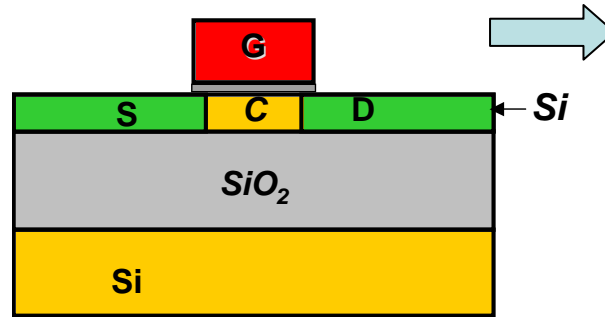
Nanotubes
Nanowires

Really Different

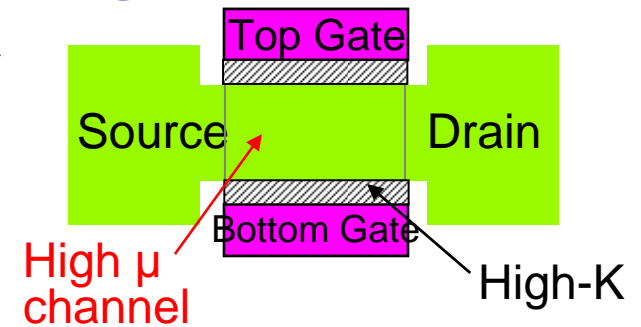
New Structures and Materials for Nanoscale MOSFETs



BULK

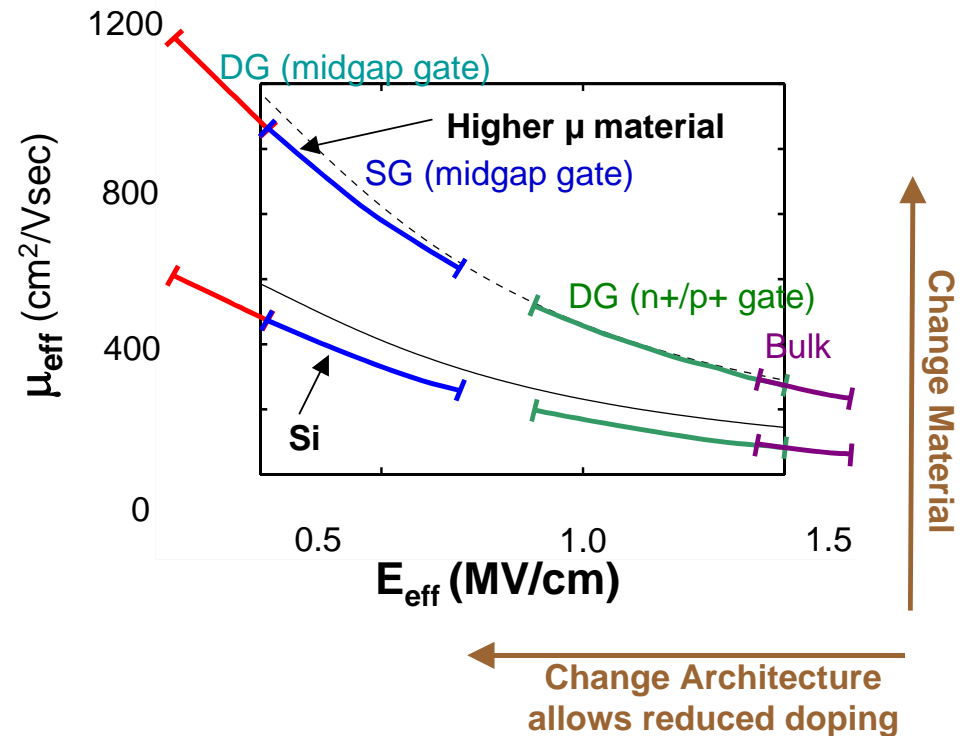


SOI



Double gate

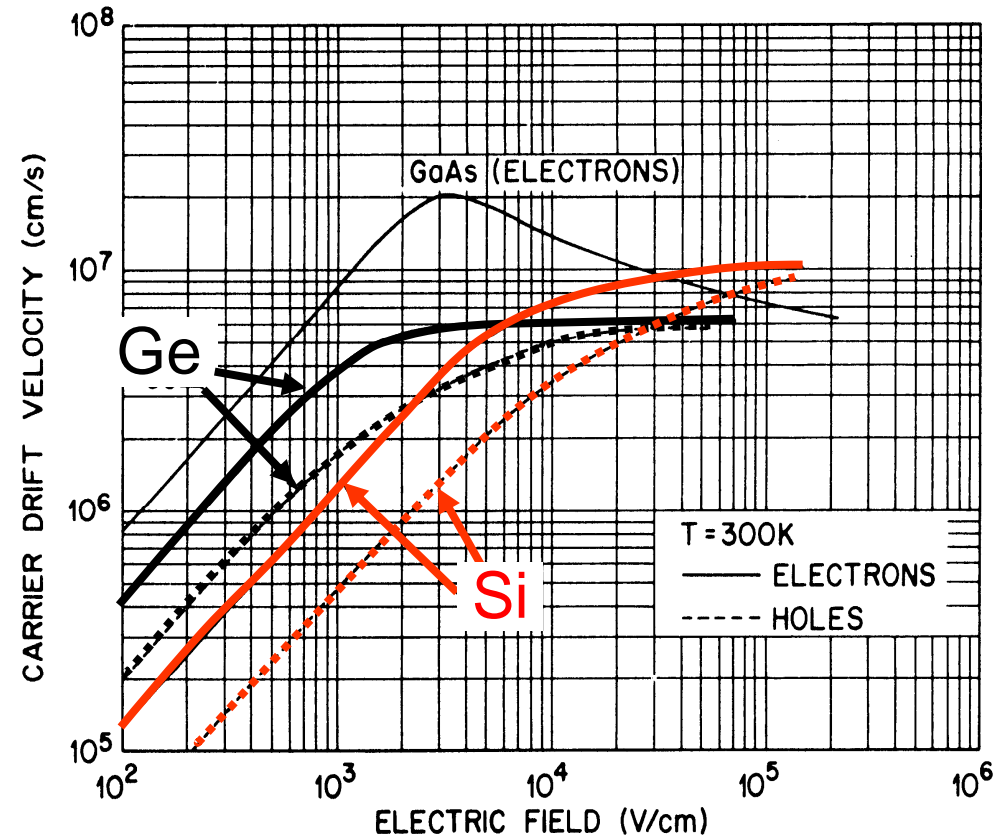
- 1. Electrostatics - Double Gate**
 - Retain gate control over channel
 - Minimize OFF-state drain-source leakage
- 2. Transport - High Mobility Channel**
 - High mobility/injection velocity
 - High drive current for low intrinsic delay
- 3. Parasitics - Schottky S/D**
 - Reduced extrinsic resistance
- 4. Gate leakage - High-K dielectrics**
 - Reduced power consumption
- 5. Gate depletion - Metal gate**



Why Germanium MOS Transistors?

Electronic Properties:

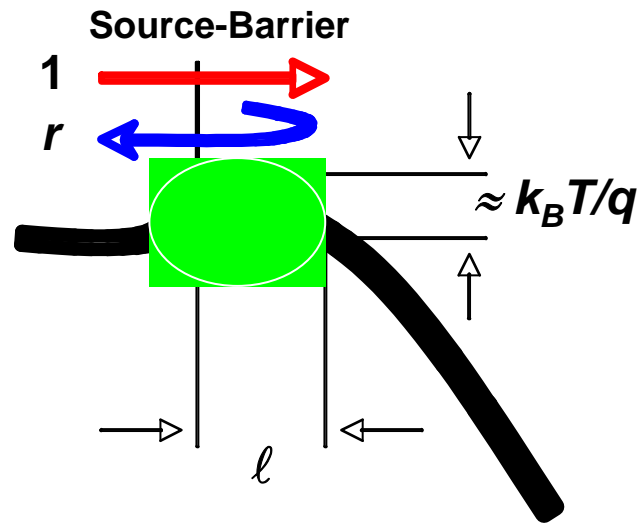
- More symmetric and higher carrier mobilities (low-field)
 - ⇒ More efficient source injection
(due to lighter m^*)
 - ⇒ ↓ CMOS gate delay
- Smaller energy bandgap
 - ⇒ Survives V_{DD} scaling
 - ⇒ ↓ R with ↓ barrier height
- Lower temperature processing
 - ⇒ 3-D compatible



(Sze, *Phys. of Semicond. Devs. 2nd Ed.*, p.46, 1981)

CMOS Performance Boost with Ge

MOSFET Channel Energy Band:



Drive Current & Gate Delay:

$$I_{ON} = \frac{W}{L_{gate}} \times Q_{inv} \times v_{inj}$$

$$\frac{C_{LOAD} V_{DD}}{I_D} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}}$$

$$v_{inj} \propto \mu$$

- Mobility (μ) at source edge is related to the backscattering coefficient (r).
- Increasing μ_s brings us closer to the *ballistic limit*

High- κ Dielectric on Germanium

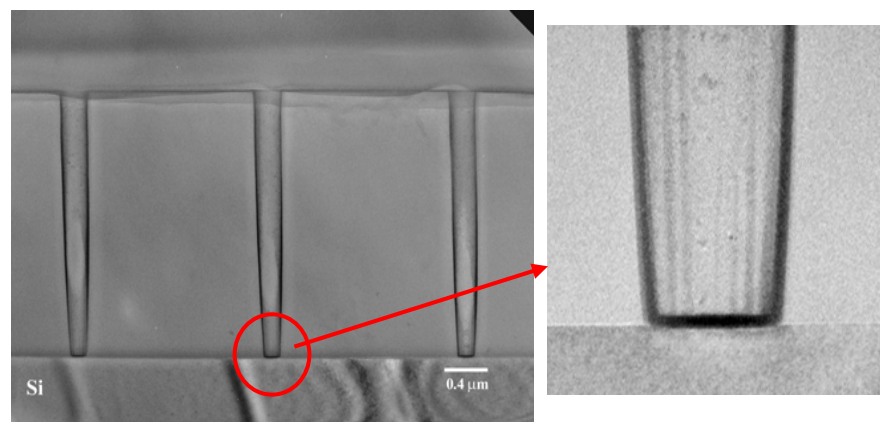
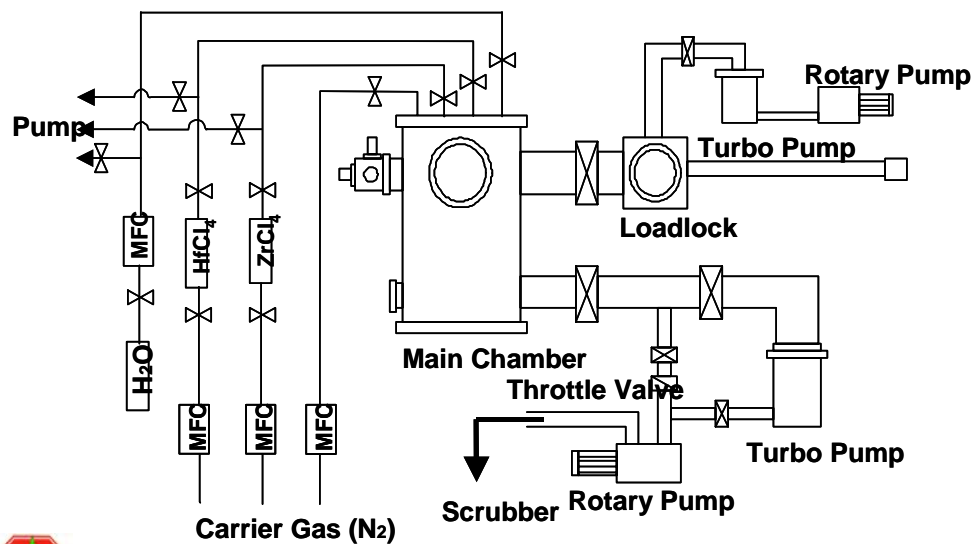
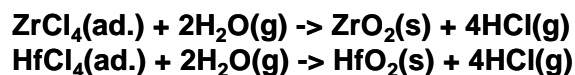
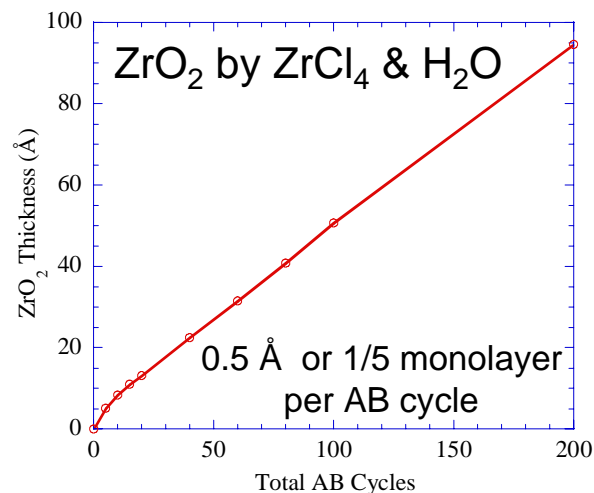
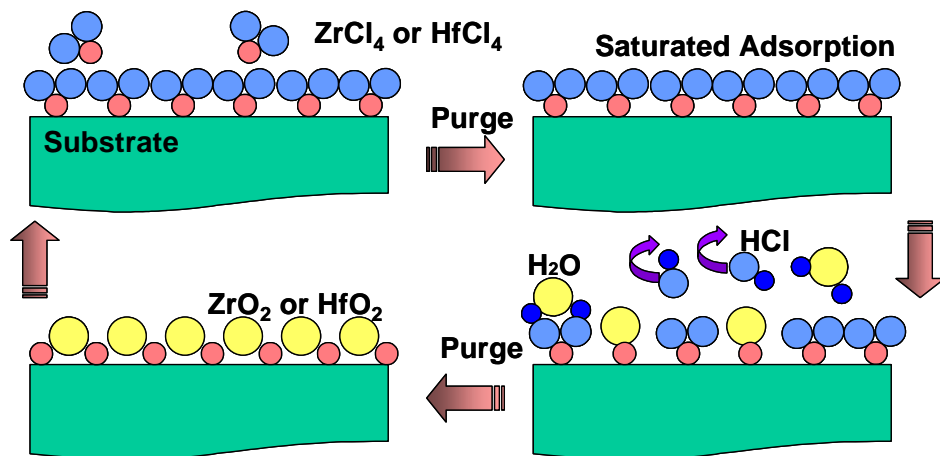
Problems:

- Common hexagonal phase of GeO_2 is a poor passivation for Ge
⇒ water soluble and volatile
- Prior attempts in the last 40 years
 - SiO_2 , GeO_x , GeO_xN_y , Ge_3N_4 , and Al_2O_3 etc.
 - Not scalable beyond 32 nm node

The Passivation Solution:

- **High- κ** dielectrics are deposited on Si, not thermally grown, why not on Ge?
- Volatility of Ge surface oxides or sub-oxides makes surface cleaning easier for **high- κ**
- Gate dielectric stack free of the performance limiting, lower- κ , interfacial GeO_x layer could be possible

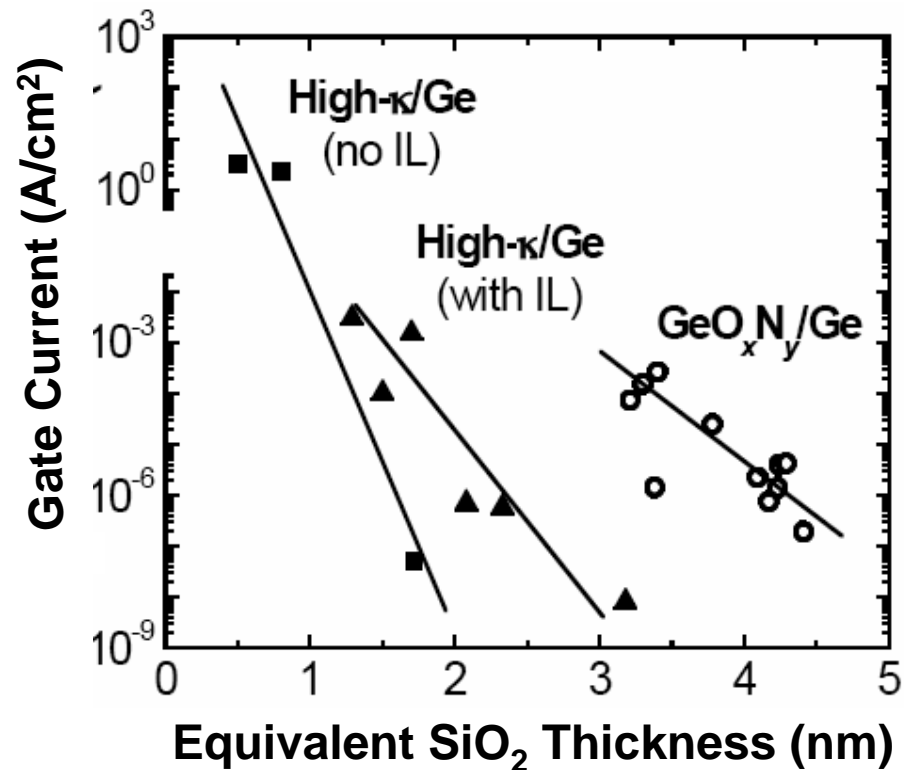
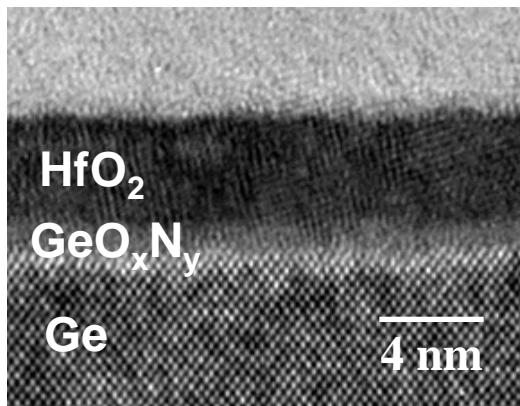
Atomic Layer CVD of Hi-κ Dielectric



(McIntyre, Saraswat, Stanford)

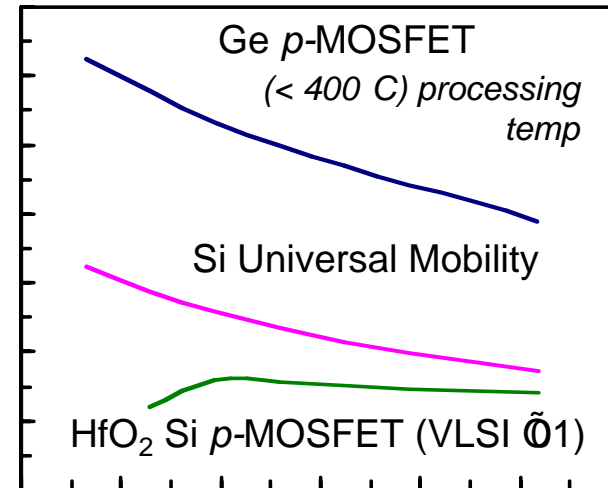
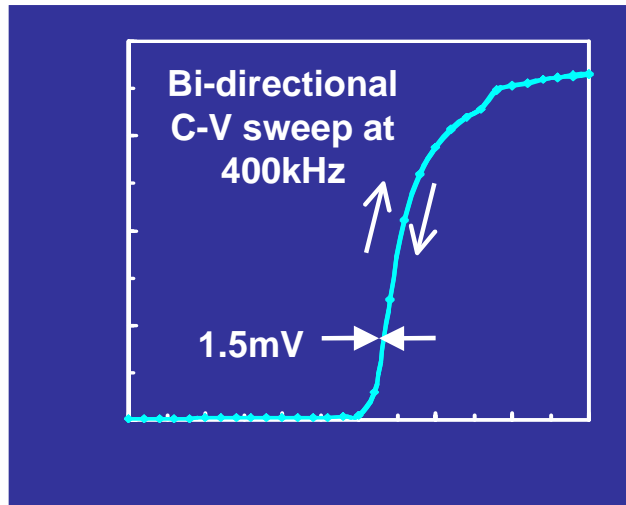
Gate Dielectric Leakage

Optimum Dielectric Stack for Ge MOSFETs



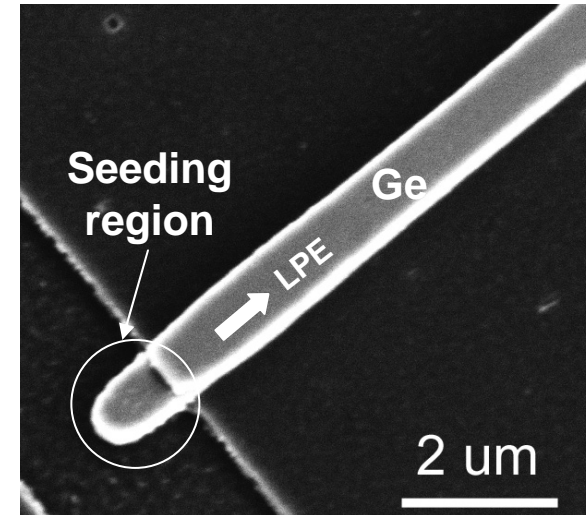
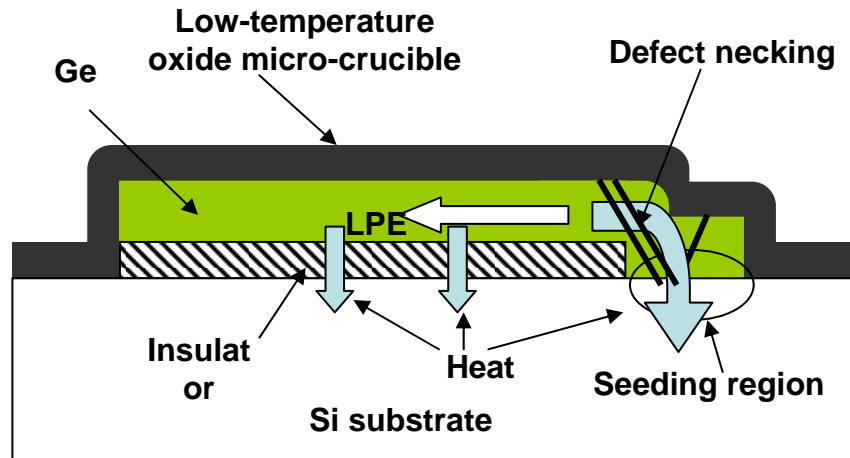
- Several orders of magnitude reduction in gate leakage
- Similar reduction on Si

High Mobility Ge PMOSFETs with ZrO₂ Gate Dielectric

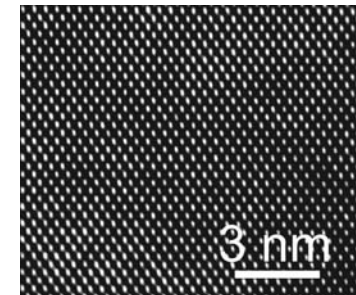
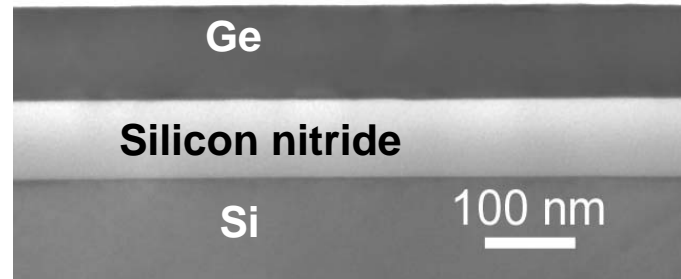
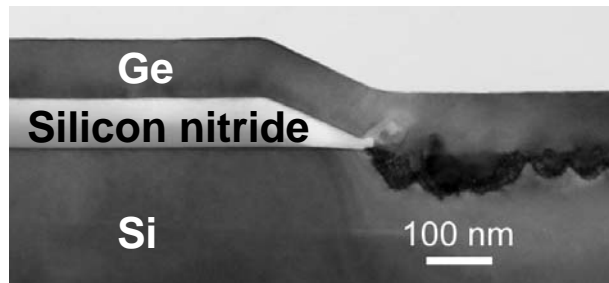


- **1st demo of metal gate and hi- κ on Ge MOSFETs**
- **EOT upto 0.5 nm demonstrated**
- **3 \times mobility vs. Hi-k Si p-MOSFETs**
- **400 $^{\circ}$ C maximum temperature process**

Liquid Phase Crystallization GOI Technology



Liquid phase epi with a micro-crucible provides seeded growth of GOI on Si.

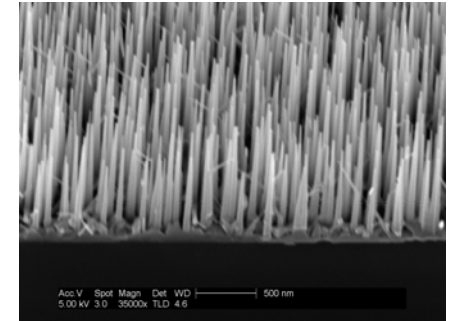
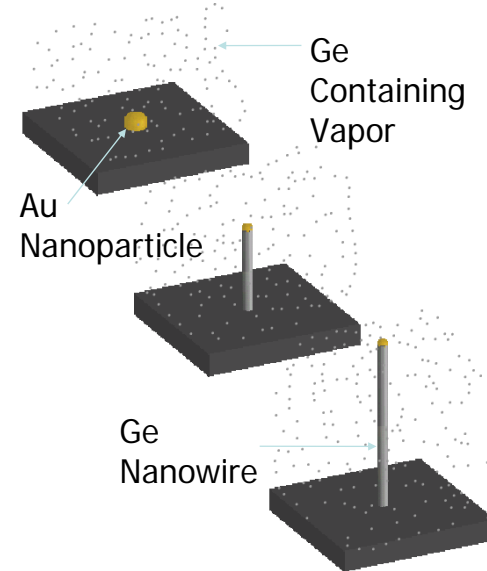
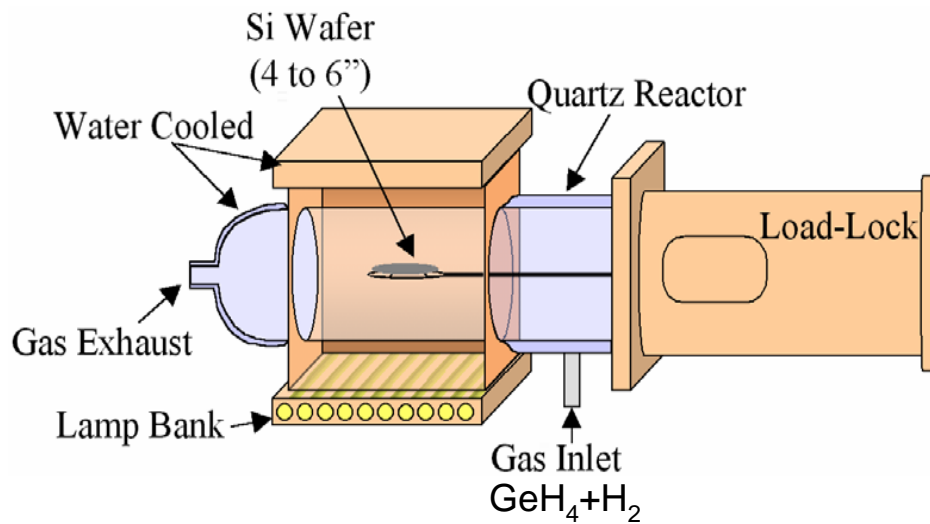


- Defect-free GOI thin films grown on (100) and (111) Si substrates.
- Initial PMOS transistors fabricated in GOI thin films show good characteristics.

Key Challenge: Low temperature defect free crystallization

(Ref: Liu and Plummer, APL March 2004)

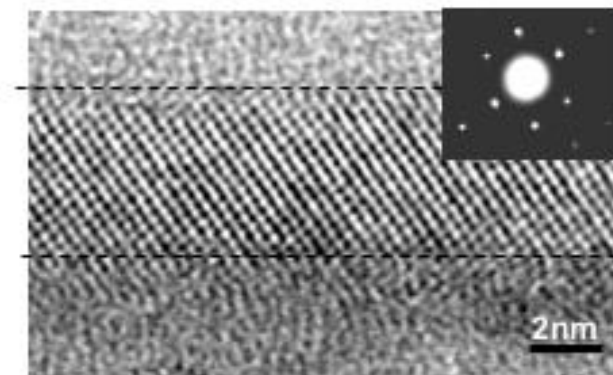
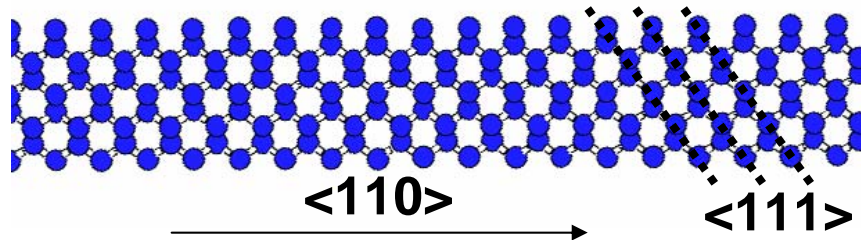
CVD synthesis of Ge nanowires



Vertical Ge NW growth on $\langle 111 \rangle$ Si

Growth Temperature: $\sim 265^\circ\text{C} - 325^\circ\text{C}$

Catalyst: Au



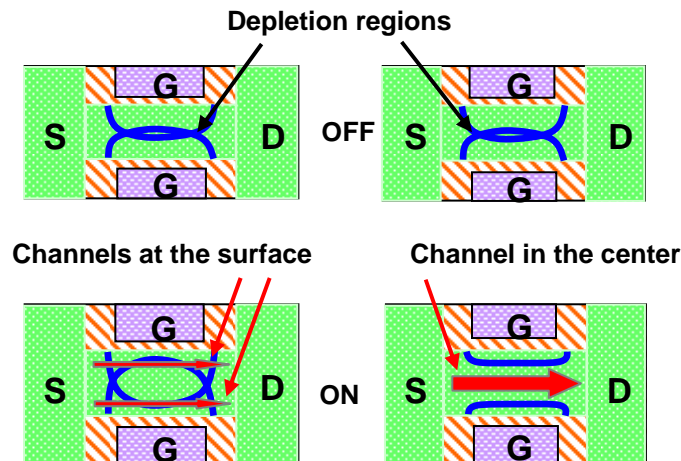
5nm Crystalline Ge nanowires

Courtesy: Hongjie Dai, Paul McIntyre, Stanford University

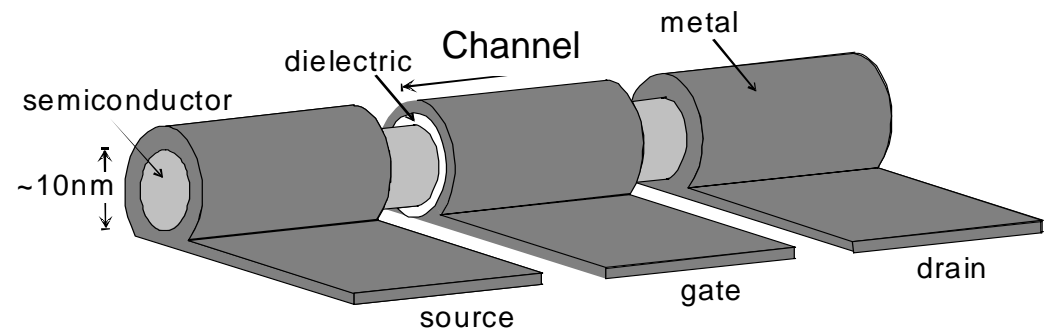
Ge Nanowire FET with High K gate dielectric

Conventional DG

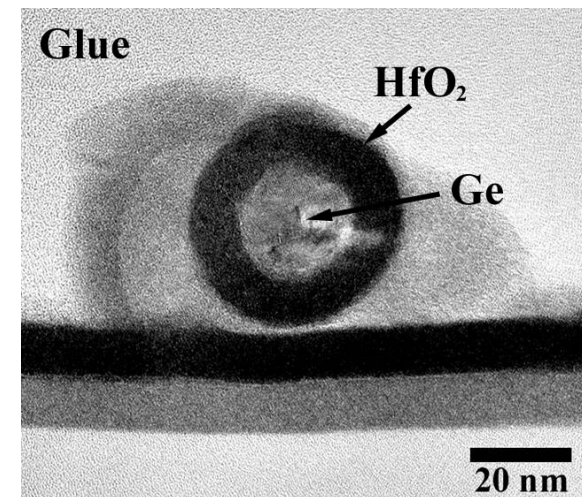
Depletion-Mode DG



Ge NW MOSFET



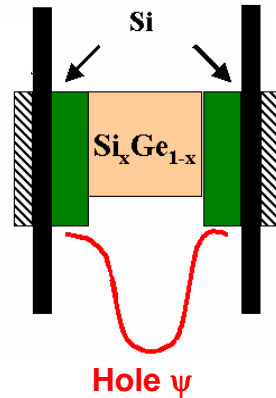
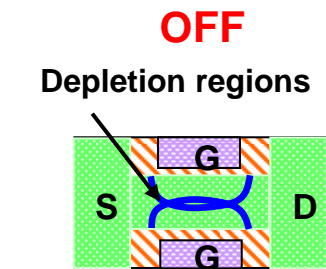
ALD HfO₂ Coating of Ge NW



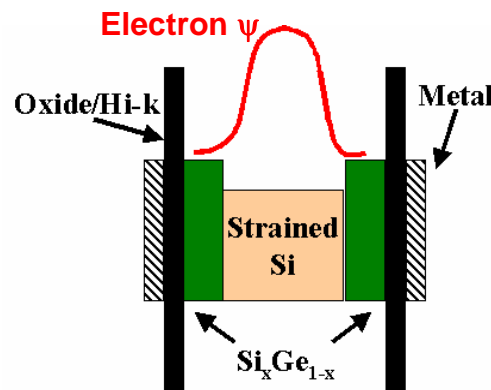
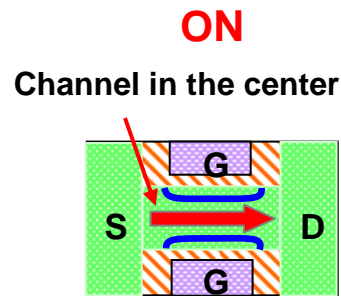
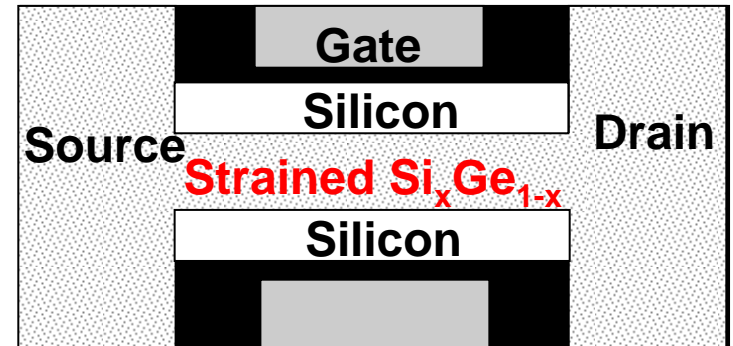
- 10-20 nm single crystal Ge wires
- CVD temperature: 275 °C
- Initial fabricated transistor shows great promise $\mu_p \sim 500$
- 3D integrable technology

(Wang, et al., Appl Phys. Lett, 22 Sept. 2003)

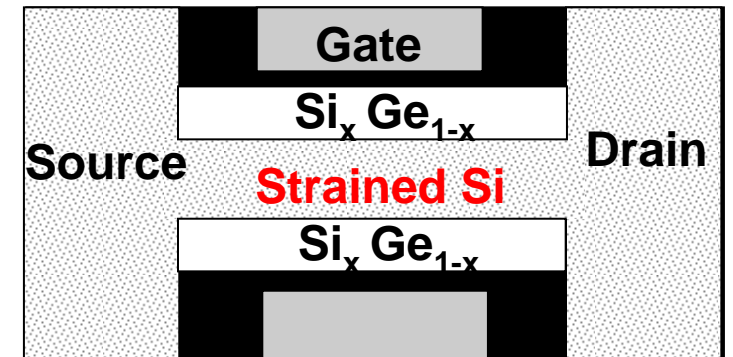
Center Channel Nanowire Heterostructure FET



PMOS



NMOS

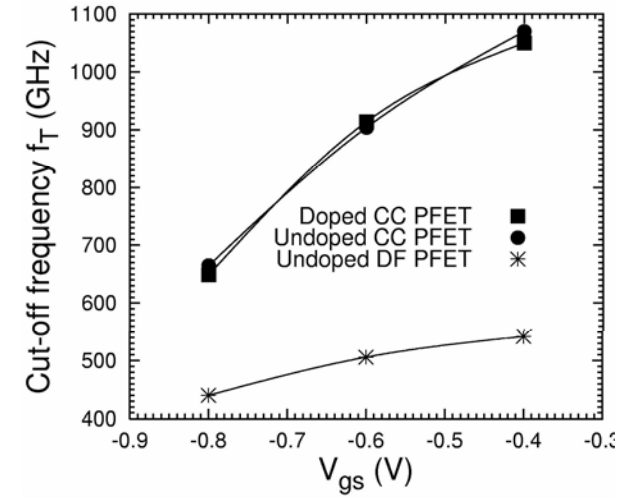
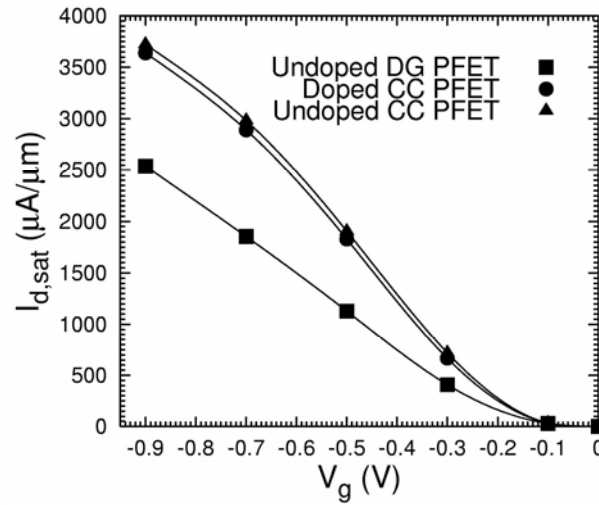
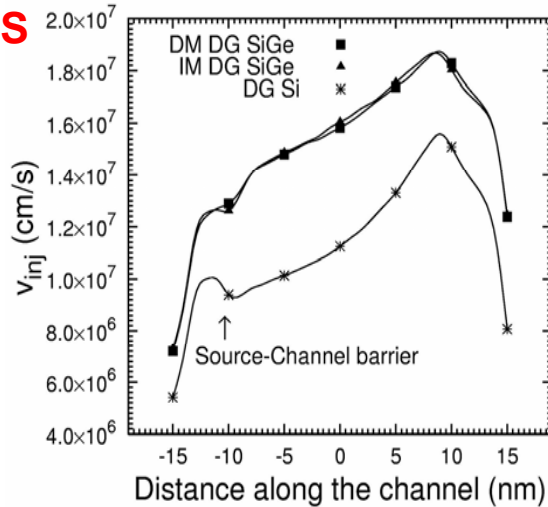


- Carriers in the center of an un-doped strained-Si or $\text{Si}_x\text{Ge}_{1-x}$ channel
- High mobility due to zero E field, strain, low surface scattering

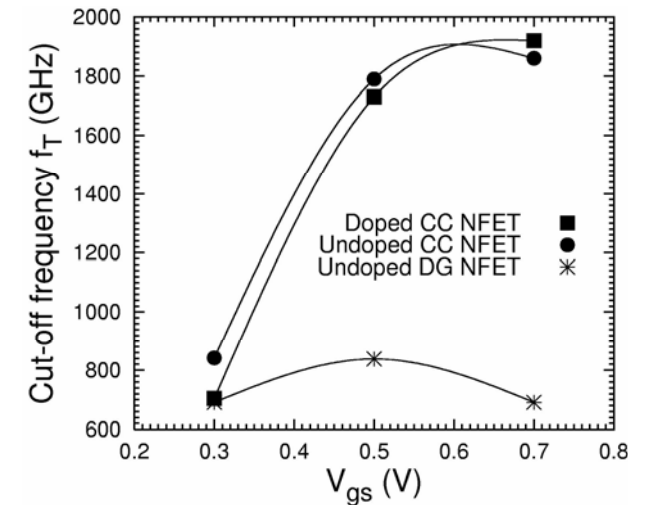
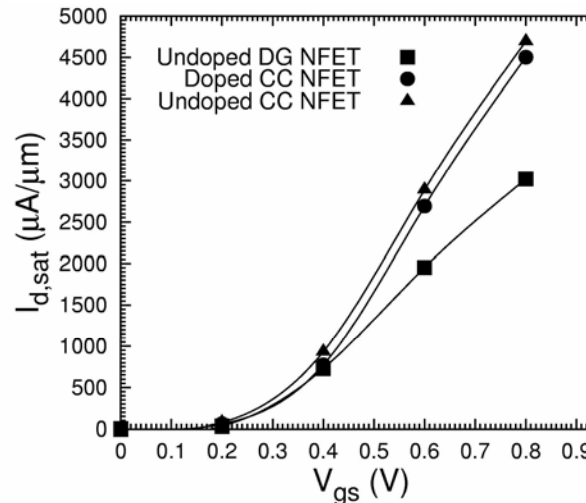
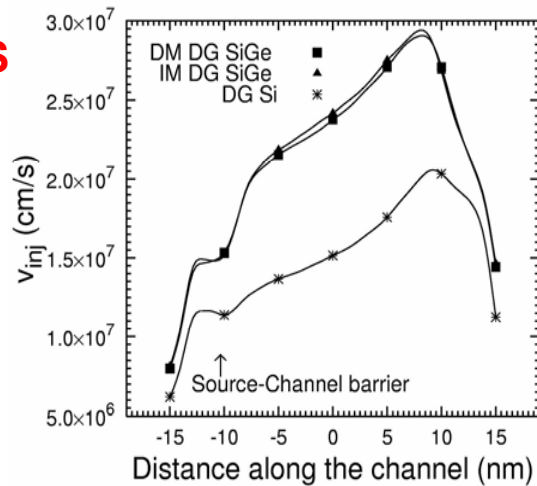
Center Channel Nanowire Heterostructure CMOS

Elwomis: Full-band Monte-Carlo simulations

NMOS



PMOS



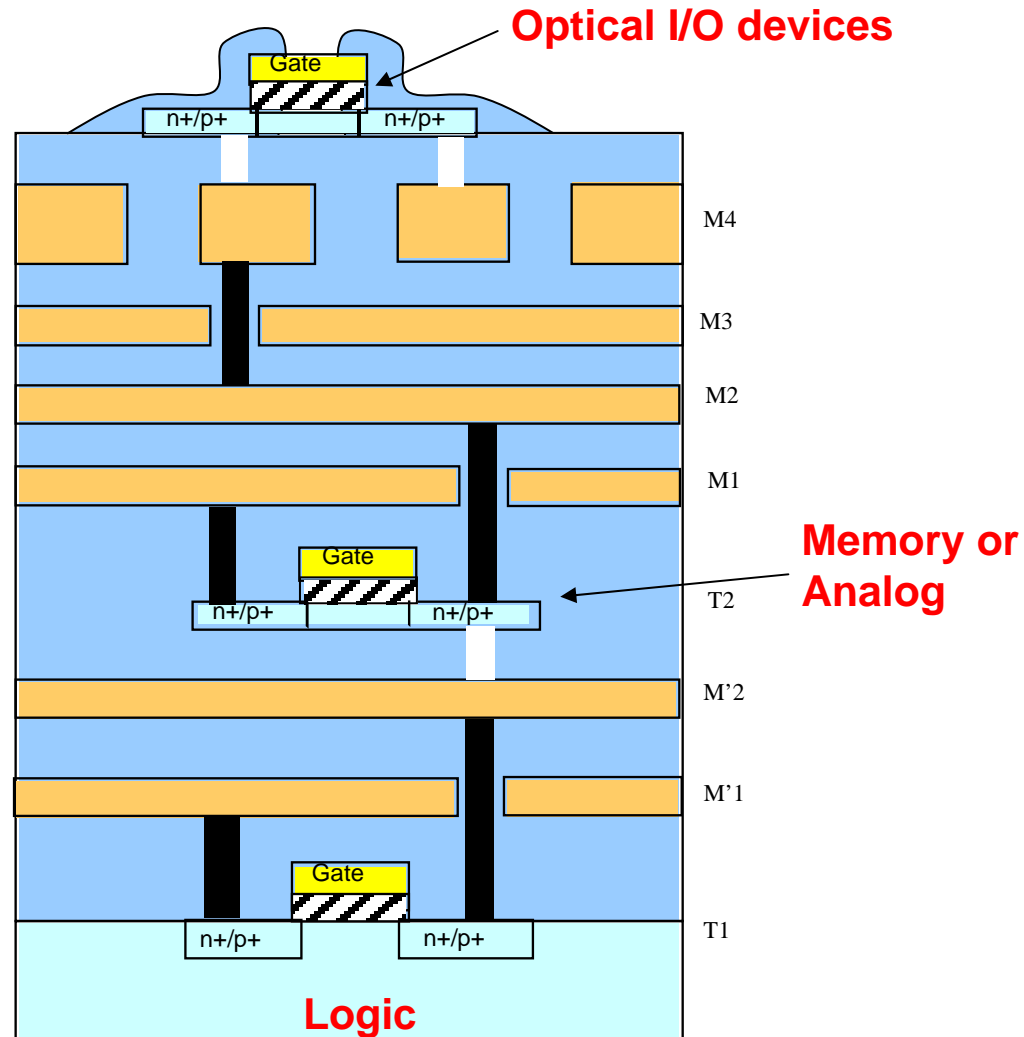
Carrier velocity

Drive current

cut-off frequency

Krishnamohan, Jungemann and Saraswat, IEEE SISPAD 2004

3D Integration

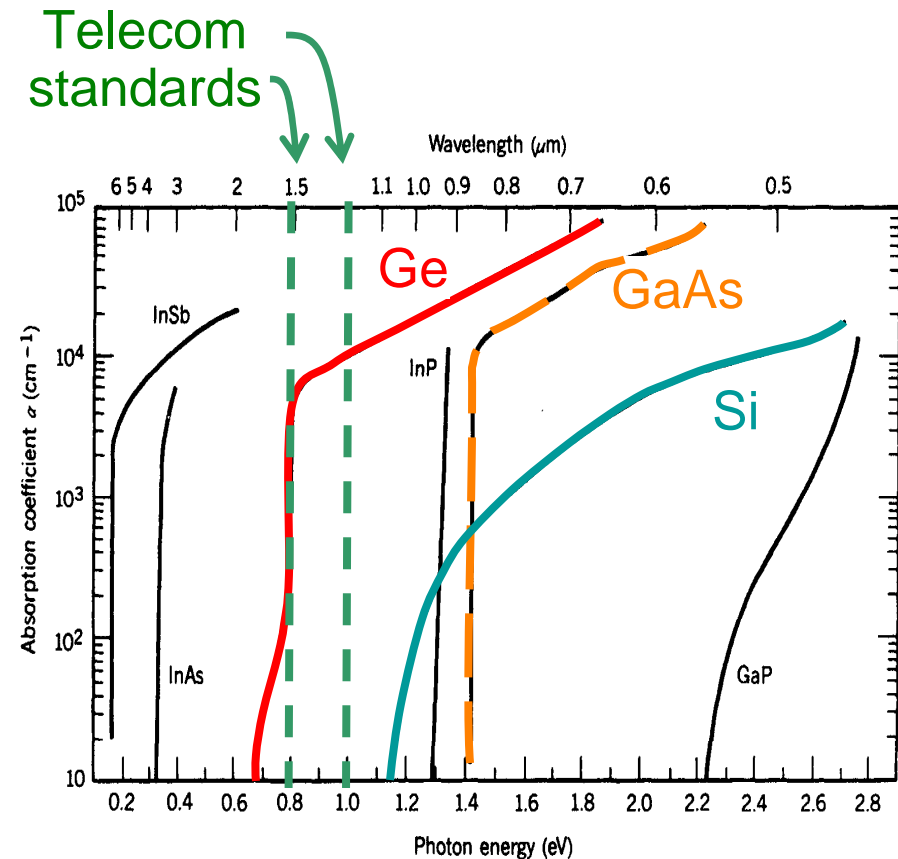


Fabricate devices at any metal level if thermal budget is low

Ge – A Prospective Optical Material

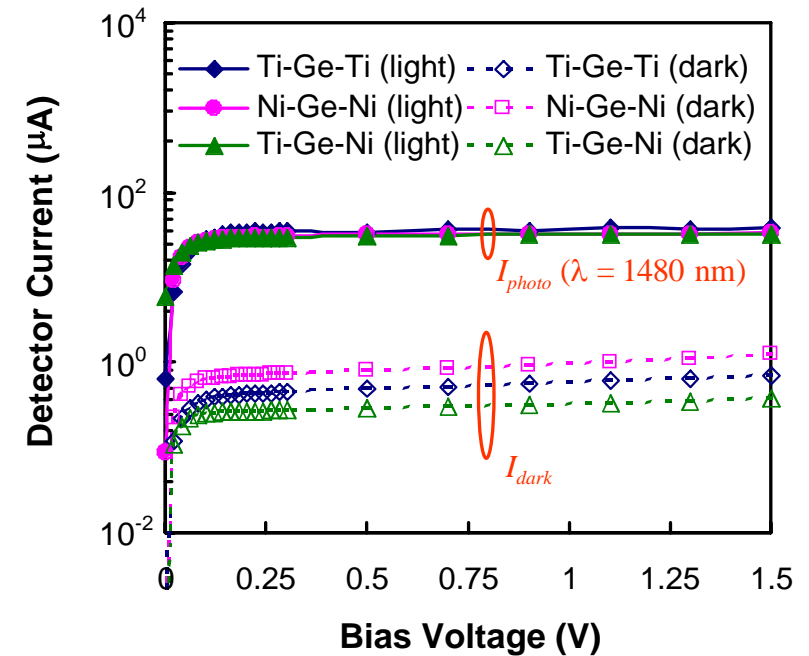
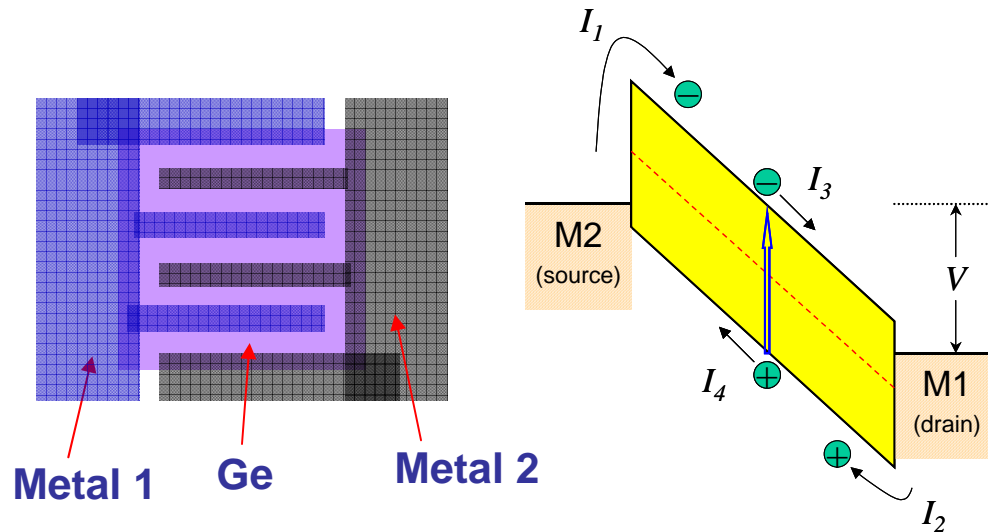
Optical Properties:

- Smaller optical bandgap
⇒ Broadens λ spectrum for opto-electronic integration to enhance CMOS functionality
- High carrier mobilities
⇒ Short detector transit time
- Lattice match with GaAs
⇒ III-V heterogeneous integration
- **Problem: Surface passivation**



(Stillman *et al.*, *IEEE TED*, 31, p.1643, 1984)

Ge Metal-Semiconductor-Metal Photodetector

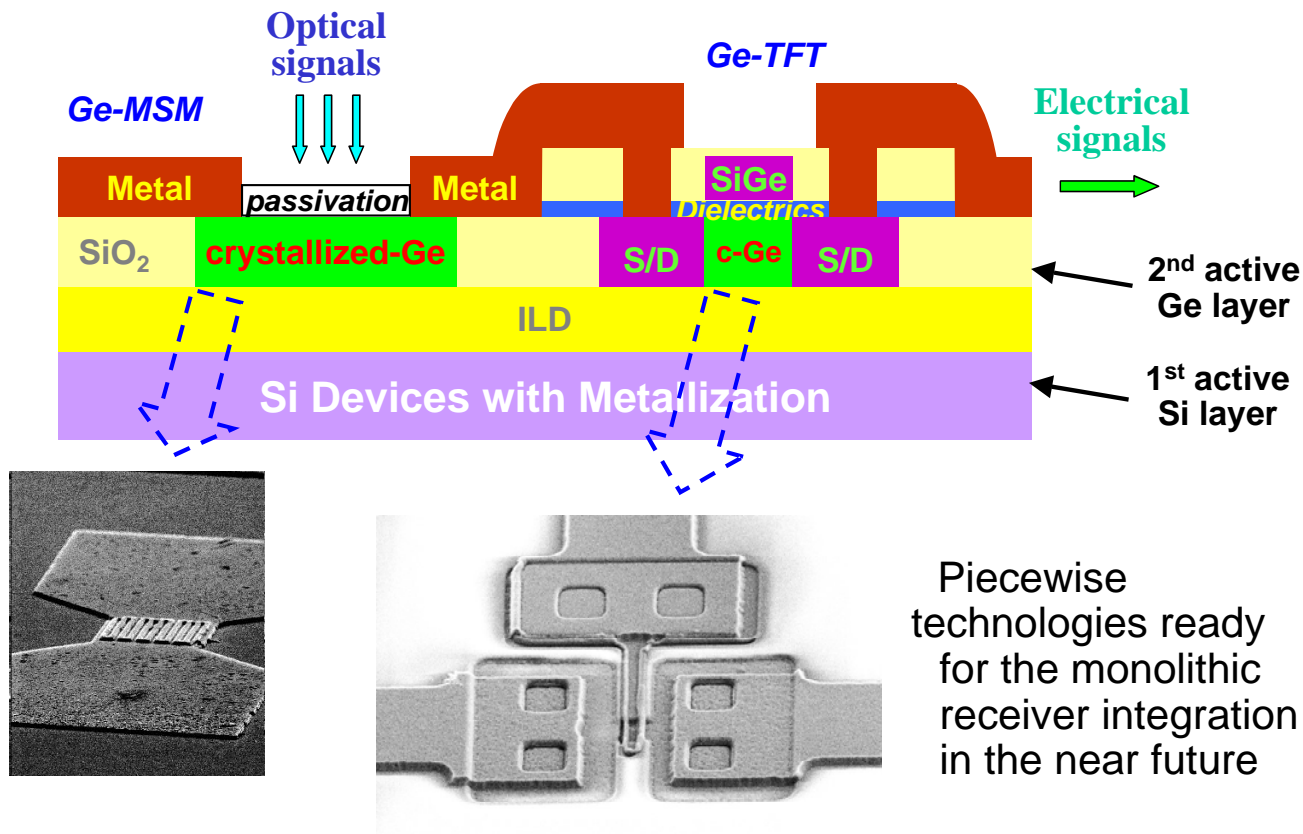


Problem: Large dark current, especially for small bandgap material like Ge

Solution: Asymmetric MSM structure to reduce dark current

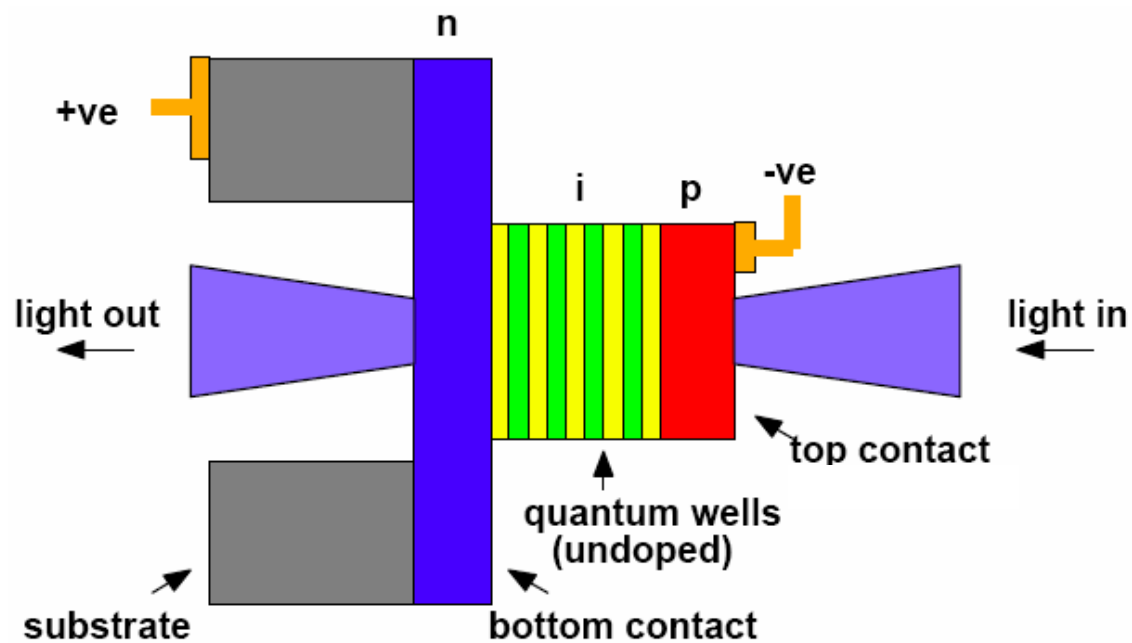
Chiu, Okyay and Saraswat, IEEE Photonics Tech. Lett., Vol. 15, Nov. 2003

3D Integration of Ge Optoelectronic Devices on Si



- Employ recrystallization or layer transfer technique for Ge on Si
- Integration of optical receiver in the upper active (Ge) layer
 ⇒ On-chip optical clock distribution in 3D-ICs

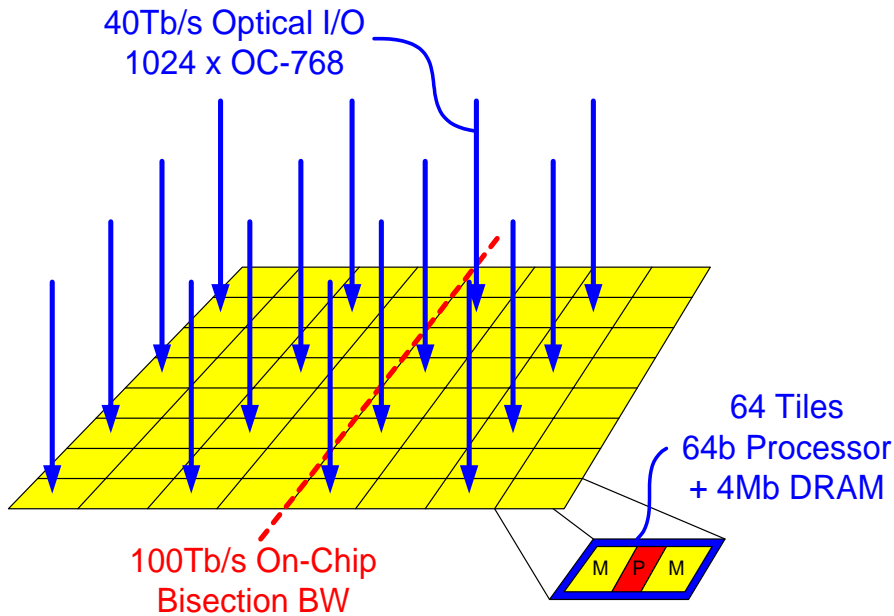
Technology for Optical Interconnects on Silicon: Quantum Well Modulator



Application of E-field changes optical transmission through quantum well modulators

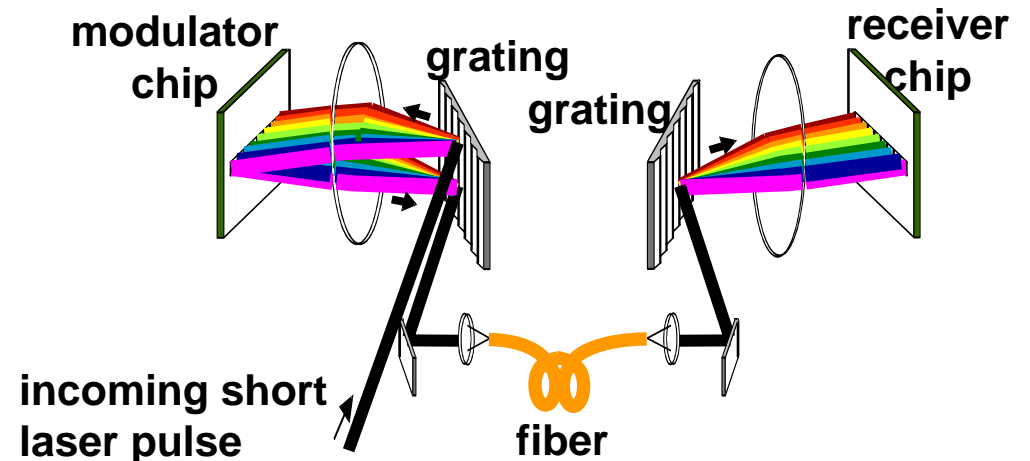
Where Can Optical Interconnects help?

On Chip Optical Interconnects

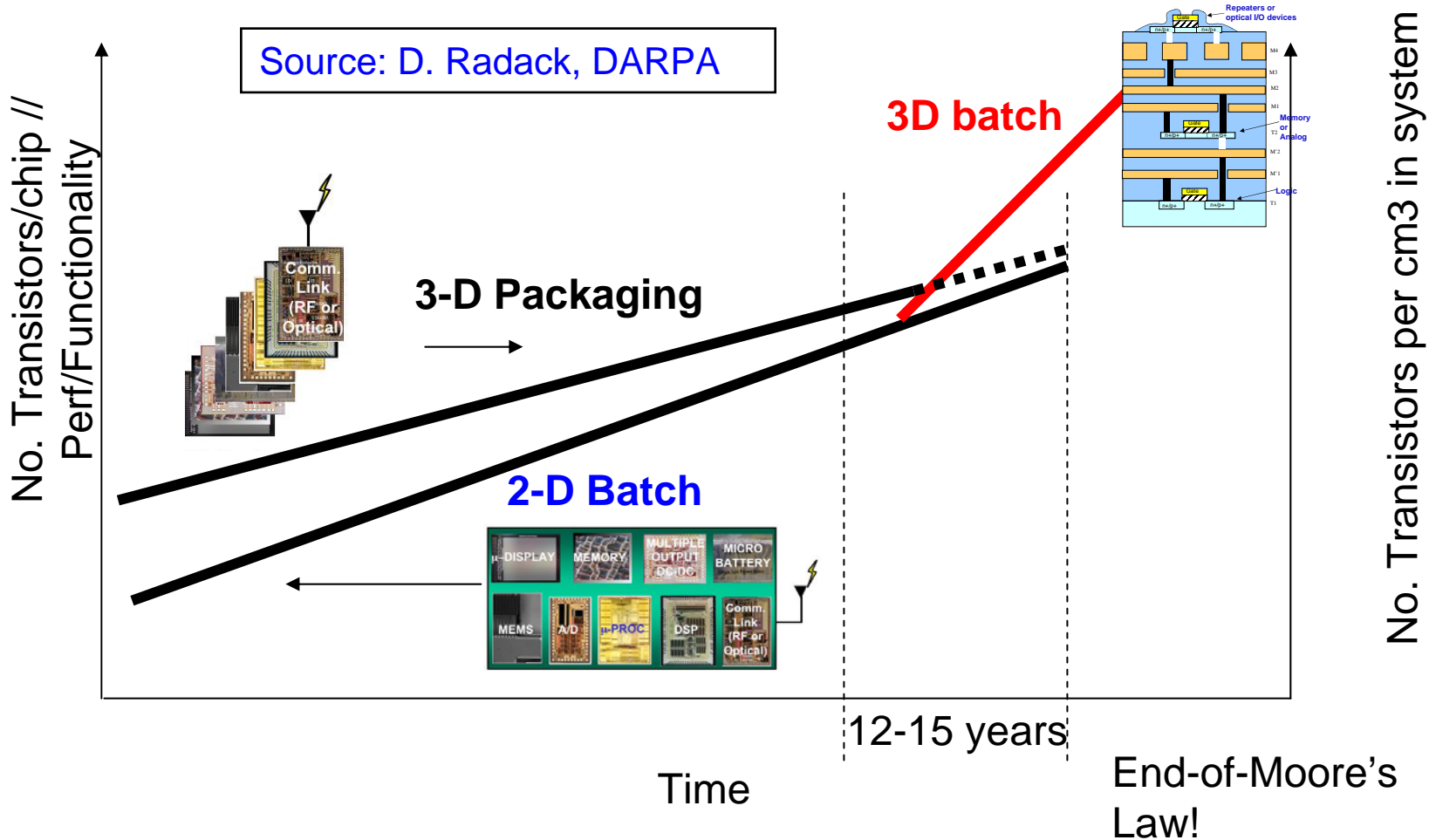


- Signal wires
 - Reduce delay
 - Increase bandwidth
- Clock distribution
 - Reduce jitter and skew
- I/O with very high bandwidth
- Reduce power
- **Need manufacturable technology**

Chip-to-chip Optical Interconnects



Motivation: Integration Density

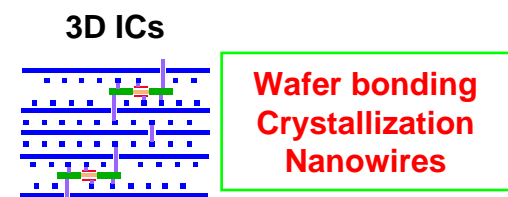
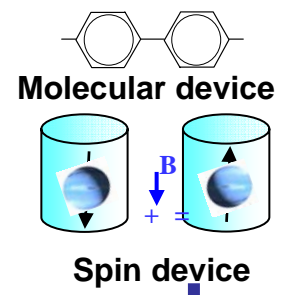


The Best Integrators of Electronic Devices Will Own the Heart of Every System – We have <15 Years to Figure it out

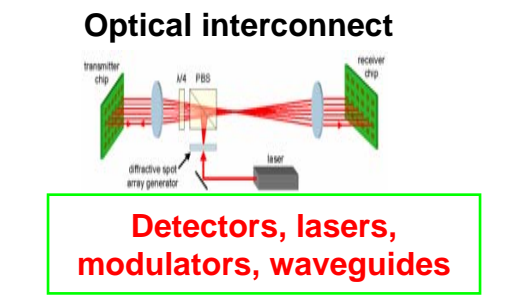
Conclusion: Technology Progression

Nanotechnology

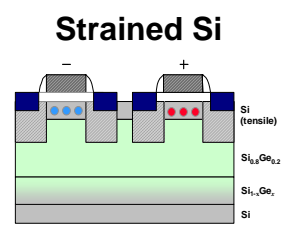
Single elec transistor



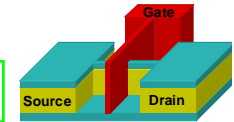
Wafer bonding
Crystallization
Nanowires



Detectors, lasers, modulators, waveguides

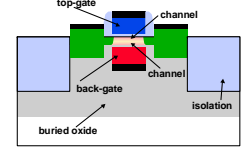


Double-Gate CMOS

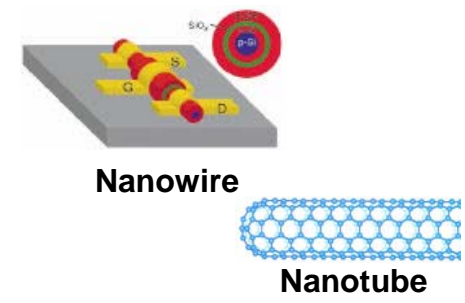


Metal gate
High k gate dielectric

Ge/Si Heterostructure

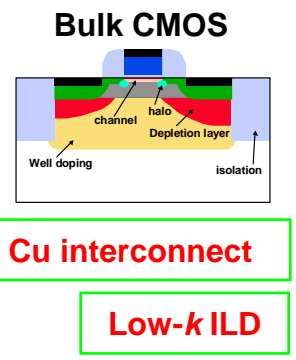


Ge on Si hetroepitaxy
Ge on Insulator

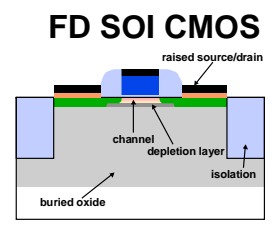


Nanowire

Nanotube



Cu interconnect
Low- k ILD



Feature Size (Time)

100 nm



1 nm

Implications for Academia

- Continued progress in silicon based CMOS IC technology requires aggressive introduction of new materials and devices
- Cost of doing industrial R&D is increasing prohibitively
- Not enough expertise in industry sector to deal with this massive challenge
- Accelerated rate of new materials, devices and structures will force us to broader, inter-disciplinary cooperation.
- Academia has wealth of research expertise in broad spectrum of disciplines, i.e. EE, PHYS, CHEM, CHEME, MS&E, APPLIED PHYS to create knowledge and understandings of such new materials as high K, Ge augmenting Si, and metal gate electrodes, optical interconnects, which can provide an integrated solution
- Industry-Academia partnership is the fundamental element of such cooperation, especially for pre-competitive research
- Infrastructure for microelectronics research in academia can be provided through multi university collaborative centers
- Networking and partnering in global scale will be the natural consequence