
Non-Volatile Silicon Memories at the Nano-Scale

An electronics example straddling semiconductor physics and technology, materials science, and large-scale integration & architecture

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Outline

- A discussion of central physical issues, characteristics of the approach, current state, and limits based on floating charge that is coupled to field effect
 - ◆ Storage based on confined medium
 - Confined but with large cross-section: nanocrystals
 - Small capture cross-section: Defects with high localization
 - ◆ Changing the locale of storage
 - Back-side storage in SOI-like structures
- Educational attributes

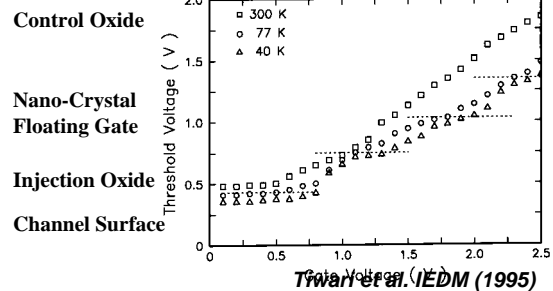
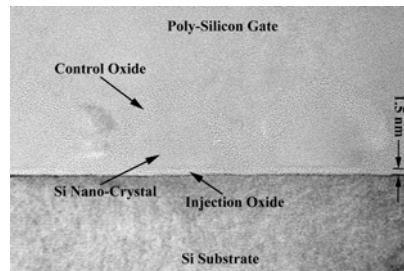
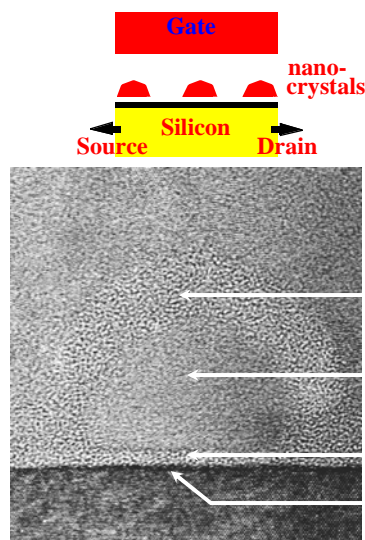
An Electron in a Semiconductor

- Unhindered movement of a single electron is μA 's of current
 - ◆ However, to observe it, requires constraints (barriers, e.g.) and the current drops – typically nA
- A 10 nm x 10 nm x 10 nm cube of silicon has ~ 50 available states in ~ 1 eV of energy range
- Variance of an ensemble of n that follows Poisson distribution is $1/\sqrt{n}$
- Mean free path of a hot electron is 5-40 nm

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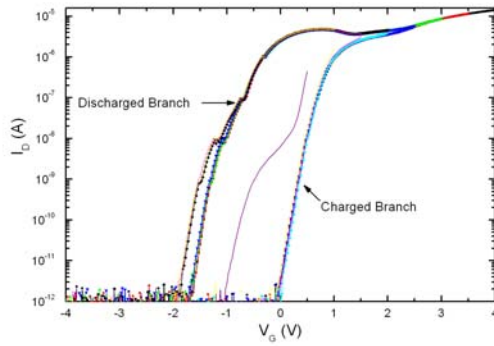
NanoCrystal Floating-Gate Memory



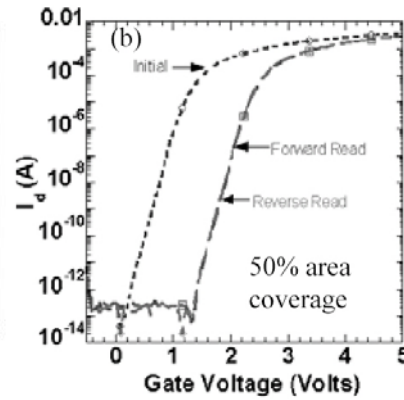
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Gain Cell

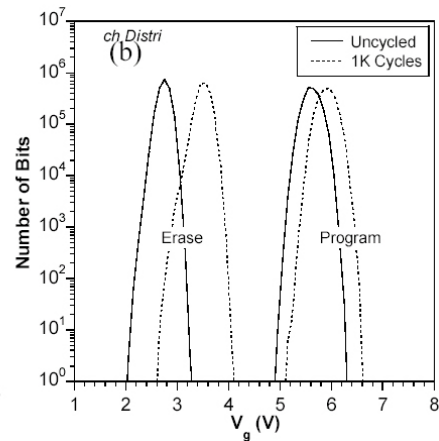
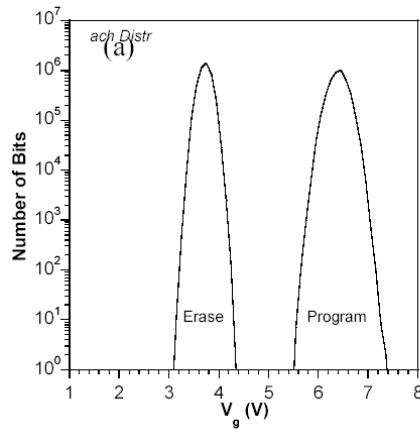


From IEDM'99



From IEDM'03

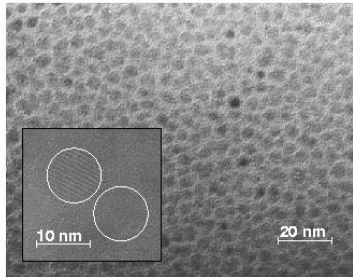
Nanocrystal Memories



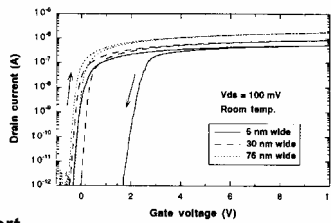
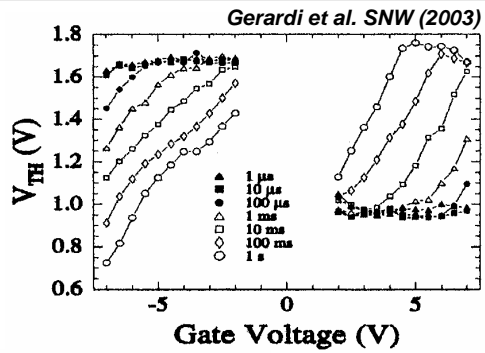
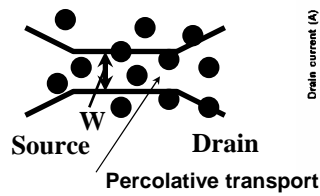
4Mb Array in a 6V 90 nm process
Muralidhar et al., 2003 IEDM

Nanocrystal Memory

Nano-crystals by aerogel dep.



De Blauwe et al. IEDM (2000)

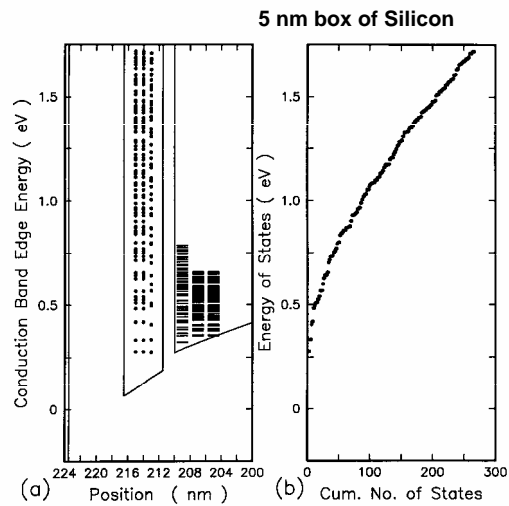
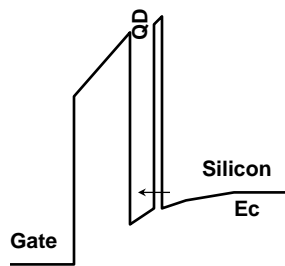


Hiramoto et al. (2000)

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Storage in Quantized Medium (Silicon)



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Charging and Erasure

Electrostatic energy change upon addition of an electron

$$\Delta E_s = \frac{Ne^2}{C} + \frac{e^2}{2C}$$

Hamiltonian for the system:

$$H = H_{2deg} + H_{qd} + H_T,$$

where

$$H_{2deg} = \sum_n (\epsilon_n + eV) a_n^\dagger a_n$$

with n identifying the indices of the ladder in the inversion layer

and

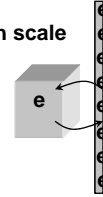
$$H_T = \sum_{n,m} T_{nm} a_n^\dagger b_m + c.c.$$

with m identifying the indices of the ladder in the quantum dot

Equation of motion for the density matrix:

$$i\hbar \frac{\partial \hat{P}_H(t)}{\partial t} = [H, \hat{P}_H(t)]$$

Quantum dot
5-10 nm length scale



Inversion layer
1-2 nm thick

Charging and Erasure

With $H_0 = H_{2deg} + H_{qd}$

the interaction density matrix is

$$\hat{P}_I(t) = \exp \left[\frac{i}{\hbar} \int_{t_0}^t H_0 dt' \right] \hat{P}_H(t) \exp \left[-\frac{i}{\hbar} \int_{t_0}^t H_0 dt' \right]$$

and the equation of motion is given by

$$i\hbar \frac{\partial \hat{P}_I(t)}{\partial t} = [H_T(t), \hat{P}_I(t)]$$

where

$$H_T(t) = \exp \left[\frac{i}{\hbar} \int_{t_0}^t H_0 dt' \right] H_T \exp \left[-\frac{i}{\hbar} \int_{t_0}^t H_0 dt' \right]$$

The solution is of the form:

$$\hat{P}_I(t) = \hat{P}_I(t_0) - \frac{i}{\hbar} \int_{t_0}^t [H_T(t'), \hat{P}_I(t')] dt'.$$

Charging and Erasure

The state of the system $|n_n, n_m\rangle$ is characterized by the probability $p_{n_m}(t)$ for occupation number n_m at time t in the quantum dot, and is given by

$$p_{n_m}(t) = \sum_{n_n} \langle n_m, n_m | \hat{P}_I(t) | n_n, n_m \rangle .$$

The probability $p_N(t)$ or N electrons in the dot can be found from this as a sum of all configurations for which $\sum_m n_m = N$

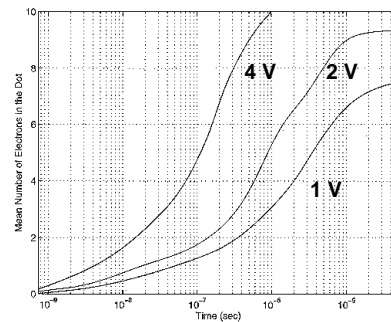
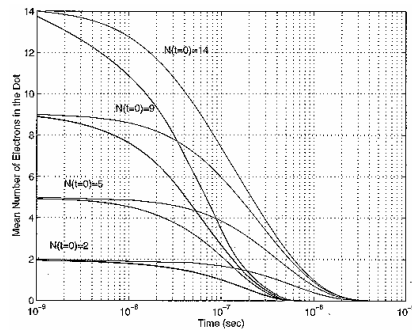
Transition equation for probability vector $\vec{P}(t) = [p_0(t), p_1(t), \dots]$ is

$$\frac{\partial \vec{P}(t)}{\partial t} = W \cdot \vec{P}(t)$$

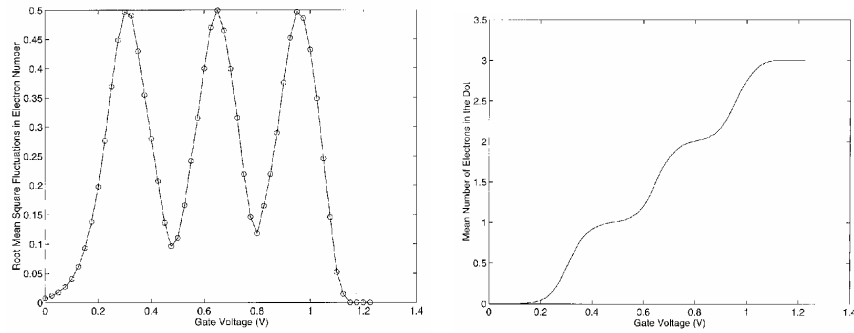
where W is the transition matrix

This now allows us to follow the evolution of the system from known initial conditions

Erasure and Injection



Occupation

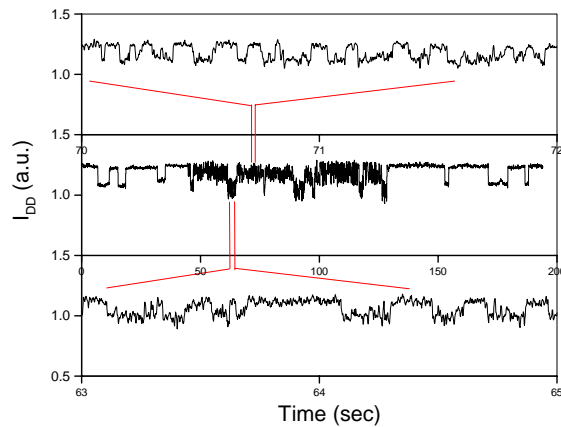


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RTS: Nano-Crystal Memory

- Fast and slow processes – surface states; and correlated processes

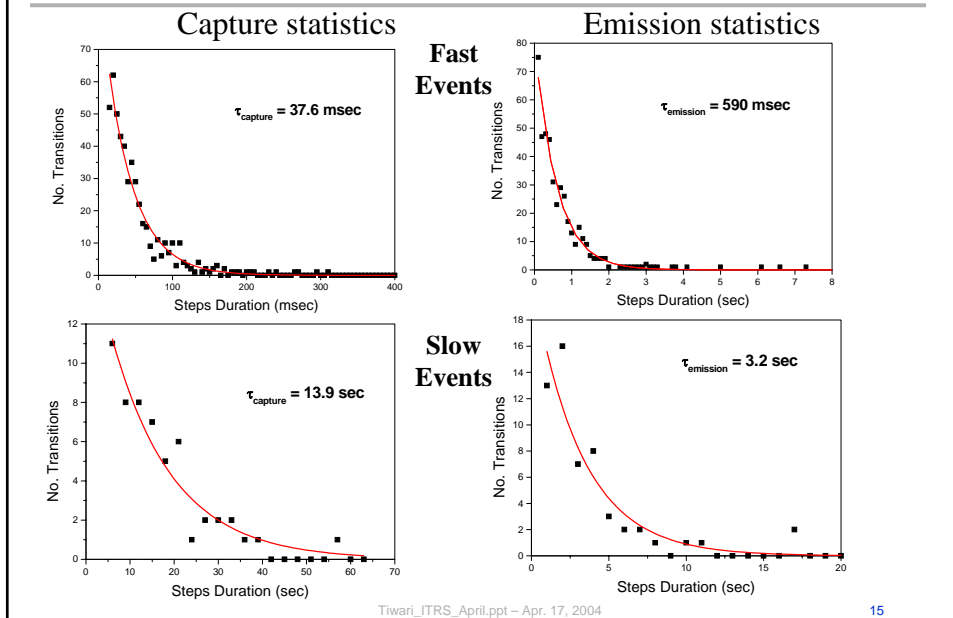


RTS Amplitude $\sim 14\%$ $\Delta t = 1$ msec

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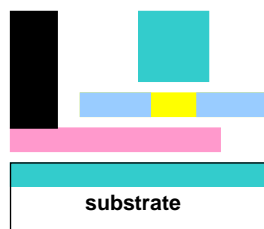
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Nano-Crystal Memory: Switching Events

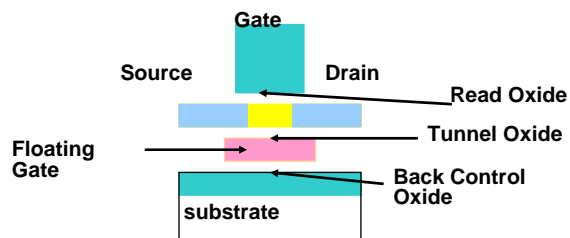


Flash Scaling: Electrostatics and Coupling

Back-Plane Transistor

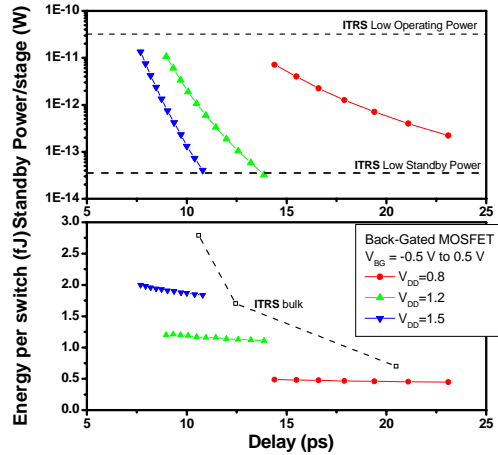


Back-Plane NVRAM



- Decoupling of read operation from writing and endurance constraints
- And makes compact SRAMs also possible

Power: Switching and Standby

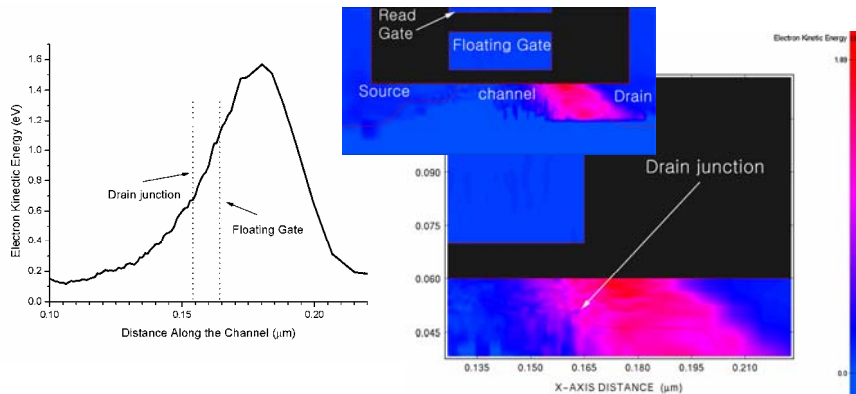


- $L = 90$ nm with 2 nm front oxide, 5 nm back oxide, 25 nm Si, and using 21 stage ring oscillator
- Devices provide tuning of standby power and switching performance with good noise margin

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Front Floating Gate Flash ($L_{eff} = 100$ nm)



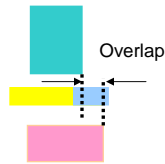
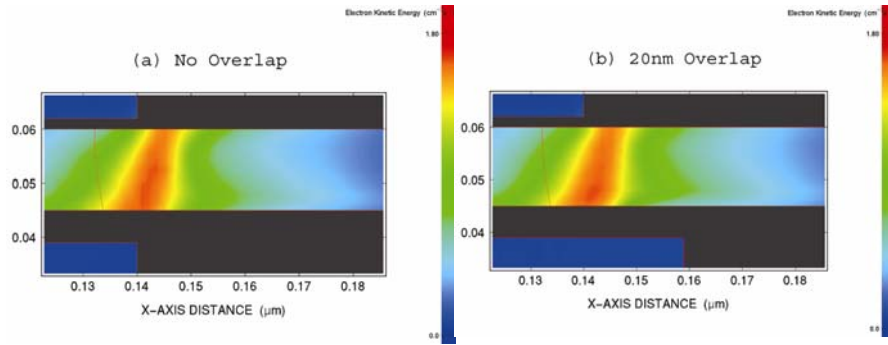
- KE loss occurs in the doped extensions together with velocity overshoot
- Smaller overlap leads to poorer coupling at smaller dimensions

Kumar et al., IEEE SNW (2002)

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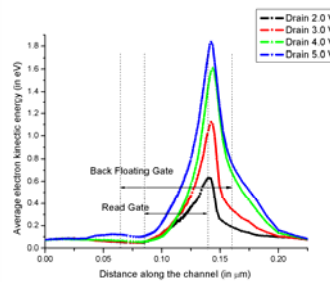
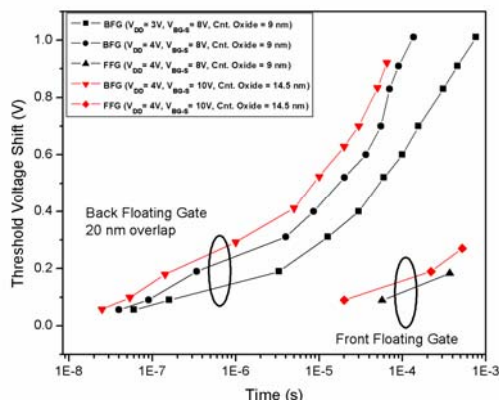
Floating Gate Overlap and Coupling



- $L_{\text{eff}}=45\text{nm}$, Si channel=15nm, Injection Oxide=6nm, Control Oxide=9nm, Back plane thickness=20nm
- Write Conditions: $V_D=-4\text{V}$, $V_S=-8\text{V}$, $V_{\text{sub}}=0\text{V}$
- Overlap is referenced to the front/read gate edge.

Kumar et al., IEEE Trans. Nanotechnology (2002)

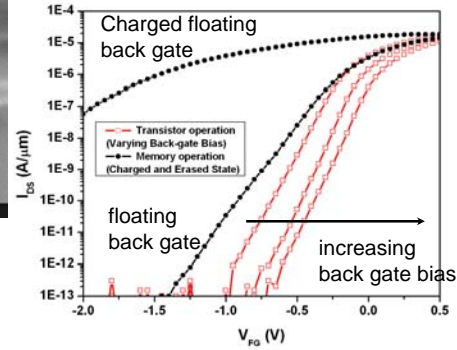
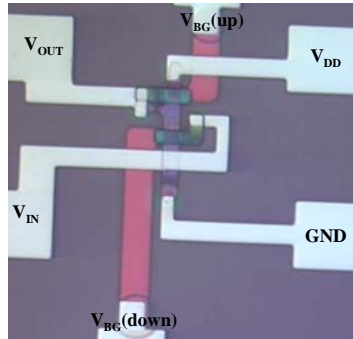
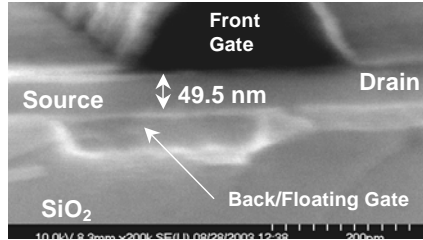
Charging Times ($L_{\text{eff}} \sim 45 \text{ nm}$)



Electron kinetic energy distribution for different drain biases along the channel

- Charging/Programming time in μs for a threshold change of $\sim 1 \text{ V}$
- Size scales limited by front-gate electrostatics and λ , i.e., 10's of nm

Tunable Back-Gated Transistors



- Threshold voltage tunable by approximately the bandgap
 - ◆ Basis for adaptive device, circuits and architecture

Avci and Tiwari, El. Letters (2004)

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Defect Charge Trapping

Electron Traps:

Two-fold coordinated N $\equiv \text{Si}_2\text{N}\cdot$
(in nitrides, oxy-nitrides)

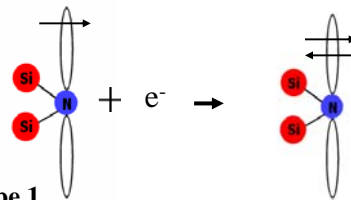
One-fold coordinated O $\equiv \text{Si}\cdot\text{O}$
(in oxides, oxy-nitrides)

...

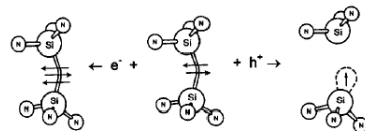
Hole Traps:

Si-Si bonds in nitrides and oxides

...



Type 1
Reduced by oxidation
 $\text{Si}_2\text{N} + \text{O} \rightarrow \text{Si}_2\text{O} + \text{N}$

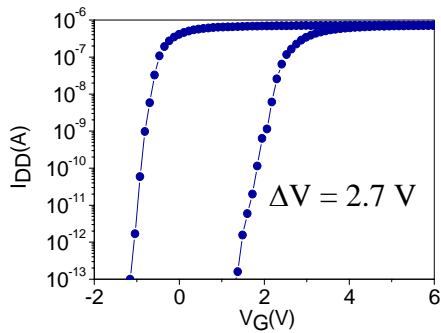


Type 3
Reduced by nitridation $\rightarrow \text{Si}_3\text{N}$
Gritsenko et al. (1999), ...

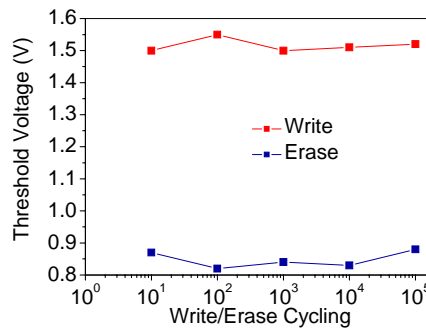
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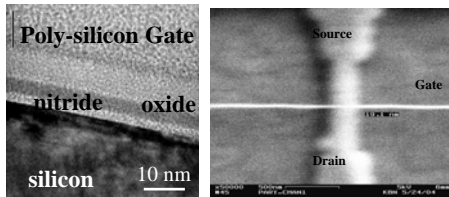
Scaled Front-Side SONOS Memories



L = 46 nm, W = 33 nm
 ONO stack = 2 / 6 / 12 nm



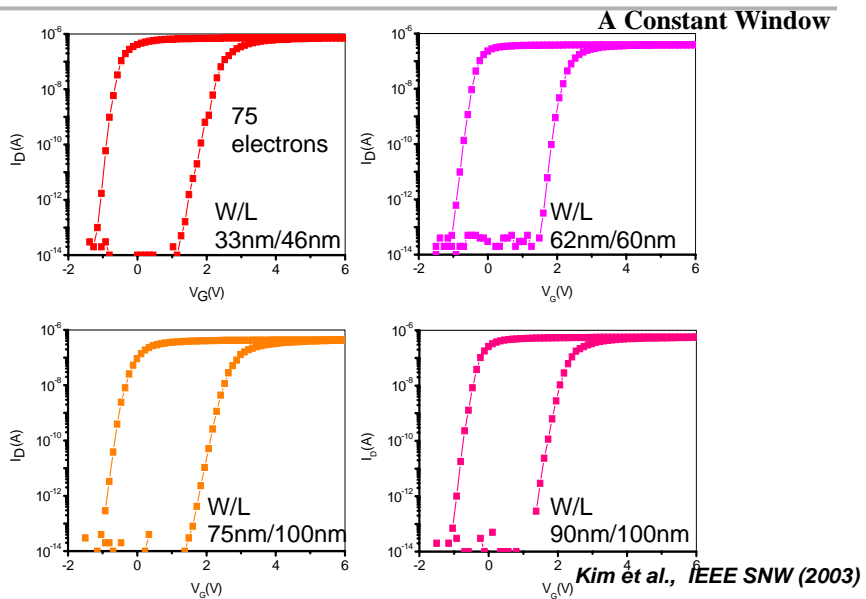
Kim et al., IEEE SNW (2003)



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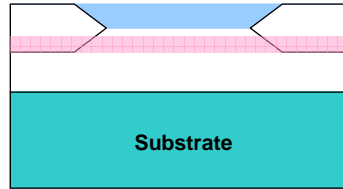
SONOS Memories



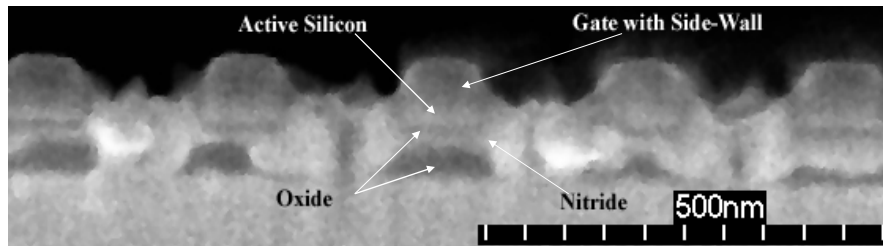
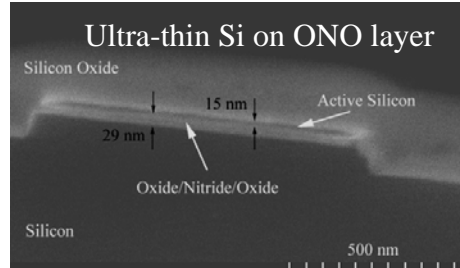
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Defects on the Back



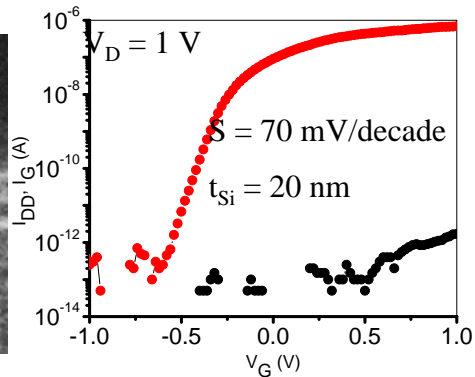
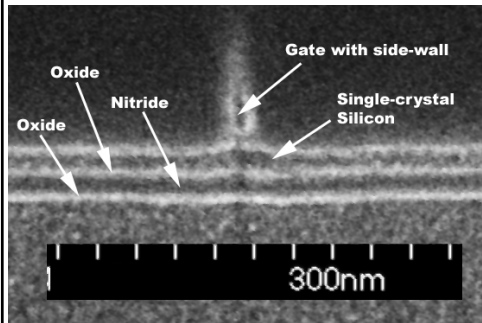
Similar to SOI ONO/n⁺ Si



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Defects on the Back



ONO stack = 2 / 6 / 13 nm;

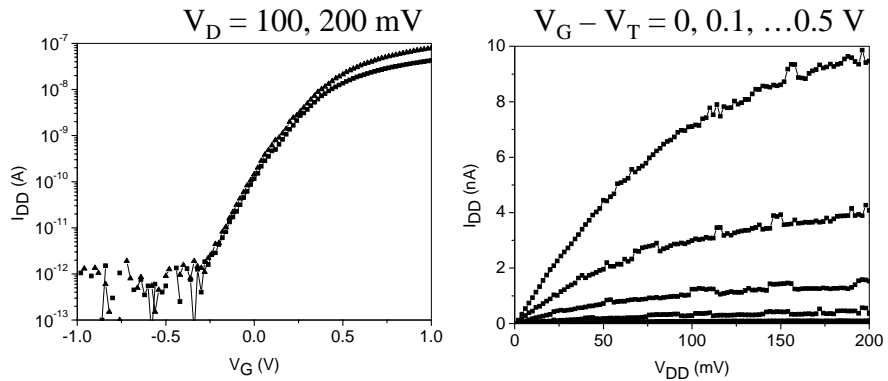
L = 50 nm, W = 100 nm

Silva et al., IEEE SOI Conf. (2003)

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Single Electrons in Output Characteristics



Oxide/Nitride/Oxide : 8 / 15 / 40 nm; $t_{Si} = 50 \text{ nm}$

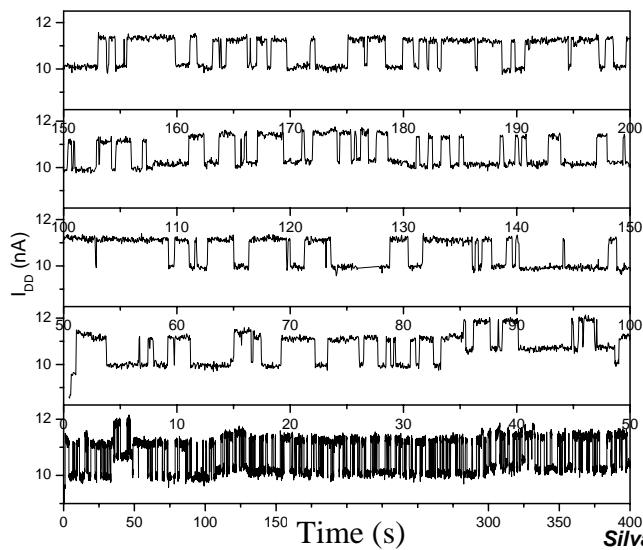
Silva et al., IEEE SOI Conf. (2003)

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Back-Interface (Si/SiO₂/SiN/SiO₂) RTS

$L = 50 \text{ nm}, V_{DD} = 10 \text{ mV}$

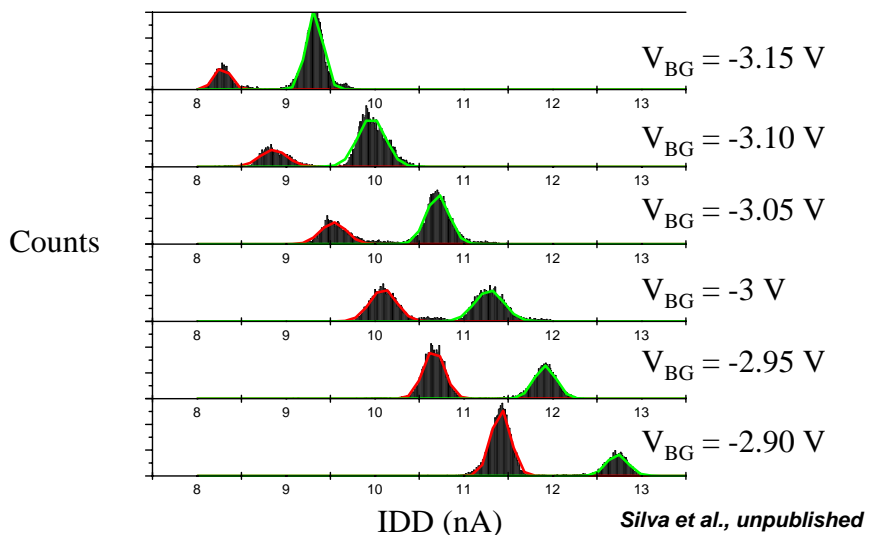


Silva et al., unpublished

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Back-Interface RTS: Histogram 2-level signal as V_{BG} swept



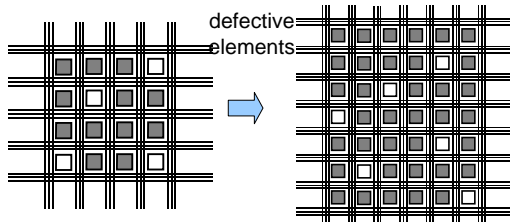
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Configurable Architectures

Configuring around defects:

What does it imply?



- Suppose, we work with 10^5 logic blocks, each employing 100 device elements
- What does it mean that one can work with chips that are 90% functional (or that 10% of logic blocks are faulty)
 - ◆ If the probability of failure is p for each element, probability of a logic block being functional is $(1-p)^{100}$
 - ◆ Probability of 90% yield in logic blocks implies $((1-p)^{100})^{10^5} = 0.9$, and device level faults of **1 in 10^8**
 - *We still need extremely high reproducibility and yield*

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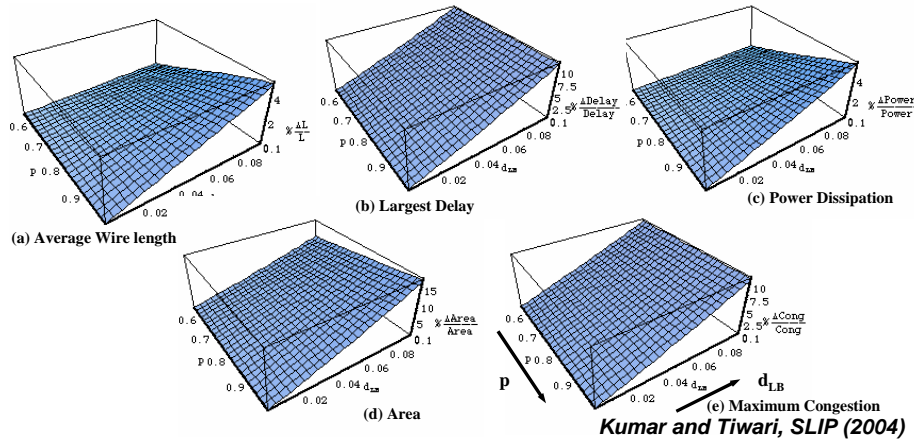
Defective Logic Blocks

- Uniform defect density d_{LB} ; Logic Block Scaling
- Increase in terminal count

$$C_{LB} = \frac{1}{1 - d_{LB}}$$

$$\Delta T_{EXT} = tN^p \left[\left(\frac{1}{1 - d_{LB}} \right)^p - 1 \right]$$

$$\Delta T_{INT} = tN \left[\left(\frac{d_{LB}}{1 - d_{LB}} \right) - \left(\left(\frac{1}{1 - d_{LB}} \right)^p - 1 \right) \right]$$



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Summary

- Using few/single electrons requires an effective compromise in storage statistics to provide sufficient tolerance while providing gains in density, power consumption and endurance
 - ◆ Example: nano-crystal memory
- Scaling to 10-30 nm length scale will require us to address electrostatics, statistics, endurance, leakage, ... significantly more carefully
 - ◆ Example: decoupling of reading from storage such as in various forms of back-storage structures

Acknowledgements

Students (H. Silva, A. Kumar, M.K. Kim, U. Avci) and collaborators from IBM and Samsung
NSF, DARPA, SRC, Center for Nanoscale Systems, Cornell Center for Materials Research and Cornell Nanoscale Facility

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Educational Issues

- Semiconductor Electronics
- Quantum Physics/Electronics
- Materials Science/Chemical Engineering
- VLSI/Algorithms/Computer Architecture
- Characterization

Advanced and increasing knowledge – not too far from traditional discipline of Electrical Engineering

- ◆ Core requirements of electrical engineering and physics, mathematics, computer sciences, and other engineering disciplines from which it draws

Ability to participate in course offerings across departments provides sufficient opportunity for broad education