

Submicron InP Bipolar Transistors: Scaling Laws, Technology Roadmaps, Fabrication Processes, High Frequency Circuits,

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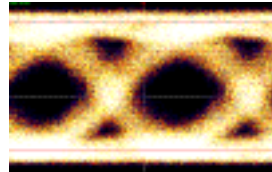
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100-1000 GHz Semiconductor Electronics: Integrated Circuits !

Optical Fiber Transceivers

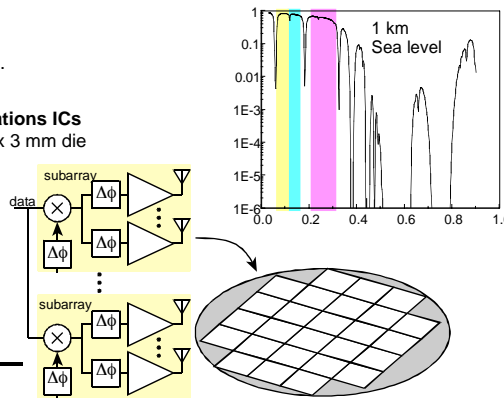
40 Gb/s now commercially available
160 Gb/s ICs now clearly feasible



mmWave Transmission

65-80 GHz, 120-160 GHz, 220-300 GHz Links
Low atmospheric attenuation (weather permitting).
High antenna gains (short wavelengths)

example: monolithic phased-array communications ICs
~6° beamwidth (30 dB aperture gain) from 3 mm x 3 mm die
array power combining _ low power per element
active beam steering_ tracks receiver motion
Gigabit rates over ~ 1 km range.

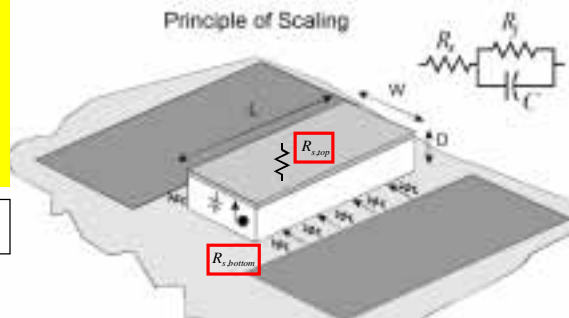


mm-wave, sub-mm-wave imaging

high resolution even with small aperture
less Rayleigh scattering than at optical, IR
aviation at night in rain and fog, weapons detection

Frequency Limits and Scaling Laws of (most) Semiconductor Electron Devices

diode as example



contributing parameters	time constant	to double bandwidth
transit time $C \propto WL/D$	$\tau \propto D/v_{electron}$	reduce D by 2:1
$R_{s,bottom} \propto 1/L$	$R_{s,bottom} C \propto W/D$	reduce W by 4:1
$C \propto WL/D$ $R_{s,top} \propto \rho_{contact}/WL$	$R_{s,top} C \propto \rho_{contact}/D$	reduce $\rho_{contact}$ by 4:1 use Schottky: $\rho_{contact} = 0$ use flared contact: $R_{s,top} L \sim \rho_c \ln(1/W)$
$C \propto WL/D$ $R_{junction} \propto kT/qI$	$R_{junction} C \propto WL/ID$ $\propto 1/JD$	increase J by 4:1
space - charge limited J		$J_{max} \propto (V + \phi)v_{electron}/D^2$, increases 4:1

R/C/ τ Limits the Bandwidth of (most) Electron Devices

resistance capacitance transit time

 device bandwidth

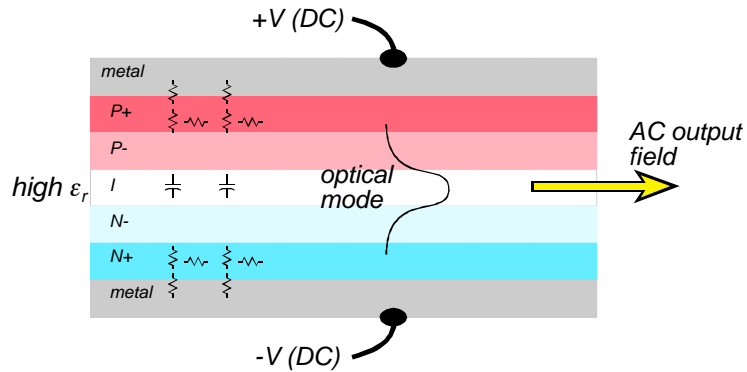
applies to:

bipolar transistors, field-effect transistors, Schottky diodes
 RTDs, photomixers, photodiodes

Applies whenever AC signals are removed through Ohmic contacts

Effective ultra high frequency devices
 must minimize, eliminate, or circumvent
 contact resistance, capacitance, & transit time

Why aren't semiconductor lasers $R/C/\tau$ limited ?



dielectric waveguide mode confines AC field away from resistive bulk and contact regions.

AC signal is not coupled through electrical contacts

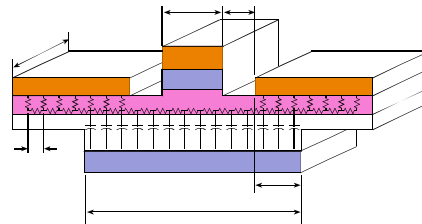
dielectric mode confinement is harder at lower frequencies

Bipolar Transistor Scaling Laws

Required transistor design changes required to double transistor bandwidth

key device parameter	required change
collector depletion layer thickness	decrease 2:1
base thickness	decrease 1.414:1
emitter junction width	decrease 4:1
collector junction width	decrease 4:1
emitter resistance per unit emitter area	decrease 4:1
current density	increase 4:1
base contact resistivity (if contacts lie above collector junction)	decrease 4:1
base contact resistivity (if contacts do not lie above collector junction)	unchanged

(C's, τ 's, C/I's all reduced 2:1)



...easily derived from geometry / resistivity / velocity relationships

We design HBTs for low gate delay, not for high f_τ & f_{max}

Gate Delay Determined by:

Depletion capacitance charging through the logic swing

$$\frac{\Delta V_{LOGIC}}{I_C} (C_{cb} + C_{be,depletion})$$

Depletion capacitance charging through the base resistance

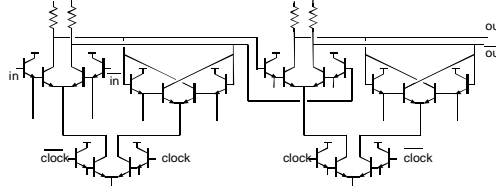
$$R_{bb} (C_{cbi} + C_{be,depletion})$$

Supplying base + collector stored charge through the base resistance

$$R_{bb} (\tau_b + \tau_c) \frac{I_C}{\Delta V_{LOGIC}}$$

The logic swing must be at least

$$\Delta V_{LOGIC} > 4 \frac{kT}{q} + R_{ex} I_C$$



$(\tau_b + \tau_c)$ typically 10 - 25% of total delay;

Delay not well correlated with f_τ

$(\Delta V_{LOGIC}/I_C)(C_{cb} + C_{be,depl})$ is 55% - 80% of total.

High (I_C/C_{cb}) is a key HBT design objective.

$$J_{max,Kirk} = 2\bar{v}_{electron} (V_{ce,operating} + V_{ce,full\ depletion}) / T_c^2$$

$$? \frac{C_{cb}\Delta V_{LOGIC}}{I_C} = \frac{\Delta V_{LOGIC}}{2V_{CE,min}} \frac{A_{collector}}{A_{emitter}} \frac{T_c}{2\bar{v}_{electron}}$$

R_{ex} must be very low for low ΔV_{logic} at high J

A Technology Roadmap for 40 / 80 / 160 Gb/s

Parameter	Gen. 1	Gen. 2	Gen. 3
MS-DF speed	60 GHz	121 GHz	260 GHz
emitter			
Emitter Width	1 μm	0.8 μm	0.5 μm
Parasitic Resistance	50 $\Omega\text{-}\mu\text{m}^2$	20 $\Omega\text{-}\mu\text{m}^2$	5 $\Omega\text{-}\mu\text{m}^2$
base			
Base Thickness	400Å	400Å	300Å
Doping	$5 \cdot 10^{19}/\text{cm}^2$	$7 \cdot 10^{19}/\text{cm}^2$	$7 \cdot 10^{19}/\text{cm}^2$
Sheet resistance	750 Ω	700 Ω	700 Ω
collector			
Contact resistance	150 $\Omega\text{-}\mu\text{m}^2$	20 $\Omega\text{-}\mu\text{m}^2$	20 $\Omega\text{-}\mu\text{m}^2$
Collector Width	3 μm	1.6 μm	0.7 μm
Collector Thickness	3000 Å	2000 Å	1000 Å
Current Density	1 mA/ μm^2	2.3 mA/ μm^2	12 mA/ μm^2
$A_{collector}/A_{emitter}$	4.55	2.6	2.9
f_τ	170 GHz	248 GHz	570 GHz
f_{max}	170 GHz	411 GHz	680 GHz
I_C/L_C	1 mA/ μm	1.9 mA/ μm	3.7 mA/ μm
τ_T	0.67 ps	0.50 ps	0.22 ps
C_{cb}/I_C	1.7 ps/V	0.62 ps/V	0.26 ps/V
$C_{cb}\Delta V_{logic}/I_C$	0.3 ps	0.19 ps	0.09 ps
$R_{bb}(\Delta V_{logic}/I_C)$	0.8	0.68	0.99
$C_{cb}(\Delta V_{logic}/I_C)$	1.7 ps	0.72 ps	0.15 ps
$R_{ex}(\Delta V_{logic}/I_C)$	0.1	0.15	0.17

Key Scaling Challenges:

Loss of yield at small dimensions
progressively harder to obtain

progressively harder to obtain;
alternative is to decouple
base & collector dimensions

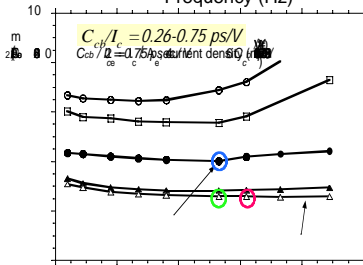
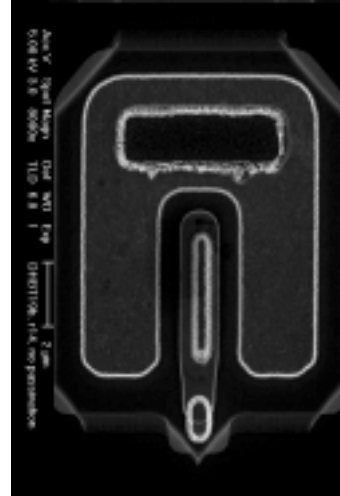
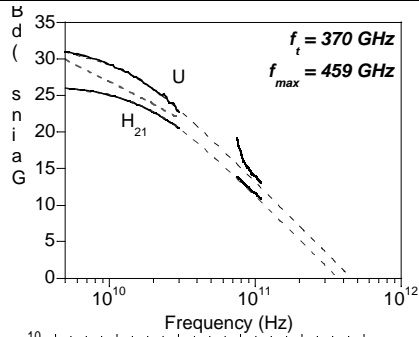
defining narrow contacts

heating _ thermal resistance

key figures of merit
for logic speed

Sub-mm-wave Indium Phosphide HBTs

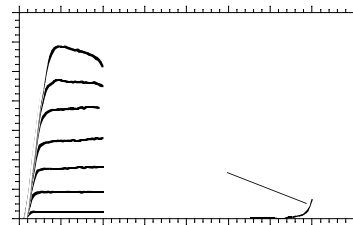
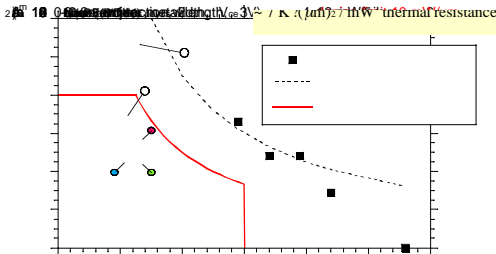
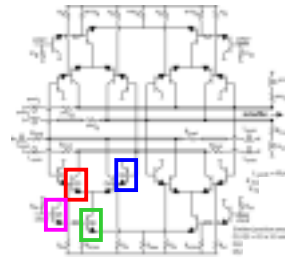
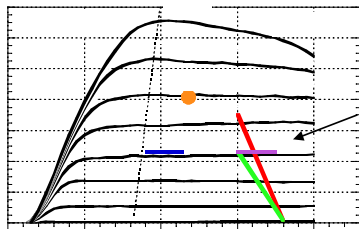
Dahlström, Griffith (UCSB/ONR); Fang, Lubyshev, Fastenau, Liu (IQE)



Late-2003 500-nm-generation mesa HBTs
 power amplifiers feasible to 250 GHz
 digital ICs (static divider benchmark) feasible to 180 GHz

Thermal failure is more significant than breakdown

Dahlström, Griffith (UCSB); Fang, Lubyshev, Fastenau, Liu (IQE)



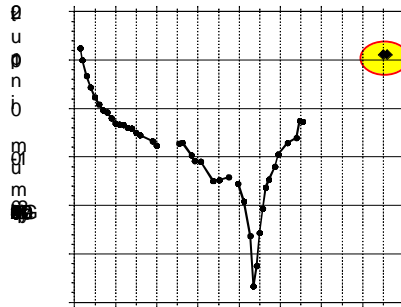
$$P/A_E = J_E V_{ce} \propto f_{clock}^2 V_{CE}$$

$$V_{br,ceo} = E_{max} T_{collector} (?), \text{ decreases more slowly than } f_{clock}^{-1}$$

UCSB / RSC / GCS 152 GHz Static Frequency Dividers



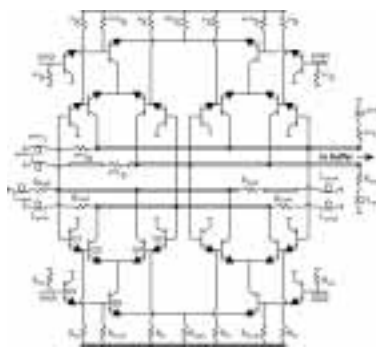
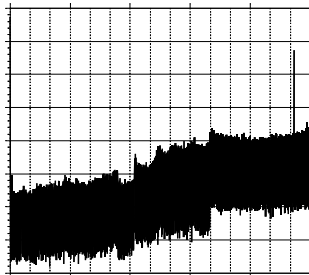
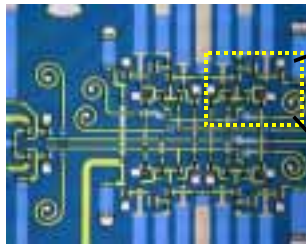
	units	data current steering	data emitter followers	clock current steering	clock emitter followers
size	μm^2	0.5 x 3.5	0.5 x 4.5	0.5 x 4.5	0.5 x 5.5
current density	$\text{mA}/\mu\text{m}^2$	6.9	4.4	4.4	4.4
C_{cb}/I_c	psec / V	0.59	0.99	0.74	0.86
V_{cb}	V	0.6	0	0.6	1.7
f_t	GHz	301	260	301	280
f_{max}	GHz	358	268	358	280



IC design: Zach Griffith, UCSB
 HBT design: RSC / UCSB / GCS
 IC Process / Fabrication: GCS
 Test: UCSB / RSC / Mayo

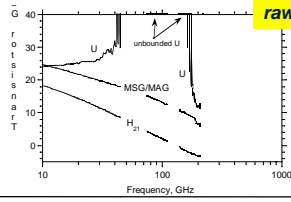
142 GHz Static Frequency Dividers: ICs built at UCSB

Z. Griffith, M. Urteaga, N. Harff, J. Prairie

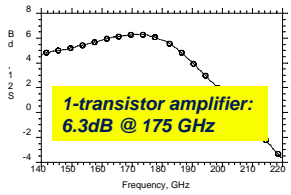
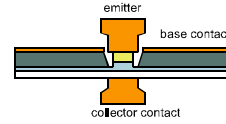
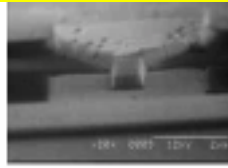


Deep Submicron Bipolar Transistors for 140-220 GHz Amplification

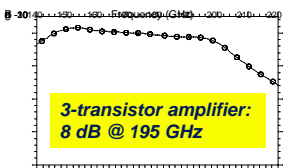
M. Urteaga



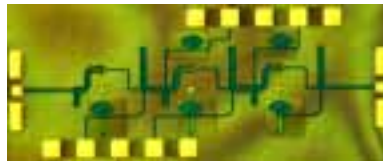
raw 0.3 μm transistor: high power gain @ 200 GHz



1-transistor amplifier:
6.3dB @ 175 GHz

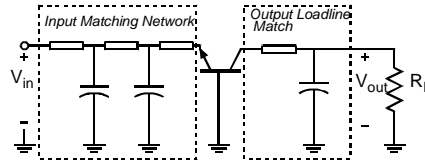
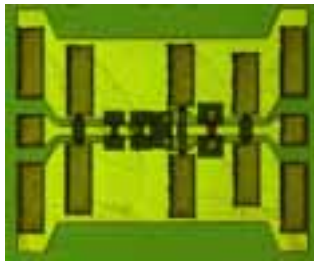


3-transistor amplifier:
8 dB @ 195 GHz

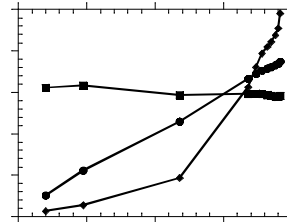
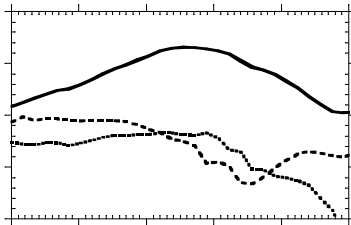


172 GHz Common-base Power Amplifier: InP Mesa DHBT

V. Paik, Z. Griffith, M. Dahlström

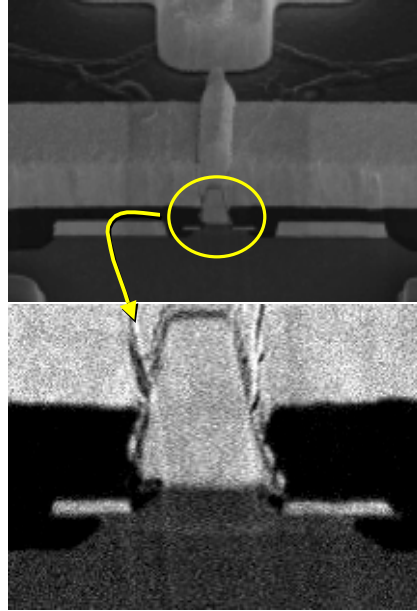
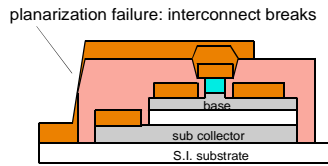
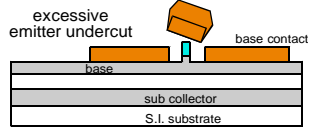
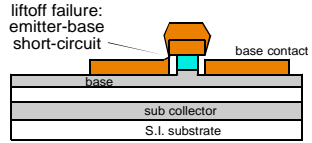


8.3 dBm saturated output power
4.5-dB associated power gain at 172 GHz
DC bias: $I_c=47$ mA, $V_{cb}=2.1$ V.



175 GHz Power Amplifier Demonstrated in a 300 GHz f_{max} process
460 GHz f_{max} DHBTs available now, 600 GHz should be feasible soon
- feasibility of power amplifiers to 350 GHz
- monolithic phased array communications ICs to 300 GHz

InP HBT limits to yield: non-planar process

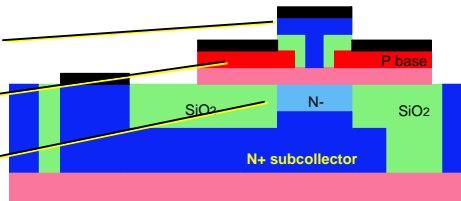


Yield quickly degrades as emitters are scaled to submicron dimensions

Parasitic Reduction

At a given scaling generation, intelligent choice of device geometry reduces extrinsic parasitics

- wide emitter contact: low resistance
- narrow emitter junction: scaling (low R_{bb}/A_e)
- thick extrinsic base: low resistance
- thin intrinsic base: low transit time
- wide base contacts: low resistance
- narrow collector junction: low capacitance

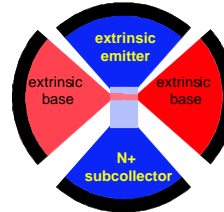


Much more fully developed in Si...

Relationship to Radial Contacts:

$$R_{bulk} = \frac{2\rho_{bulk}}{\pi L} \ln \left[\frac{L}{W} \sqrt{\frac{r}{W}} \right]$$

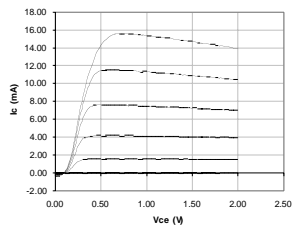
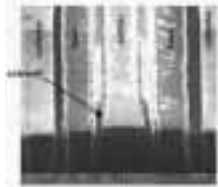
$$R_{contact} = \frac{\rho_s}{\pi L r}$$



— greatly reduced access resistance

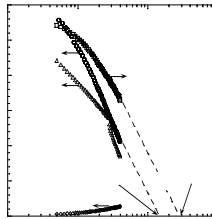
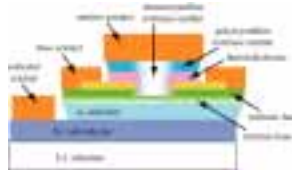
Low Parasitic, Scalable HBT processes

Emitter dielectric sidewall process



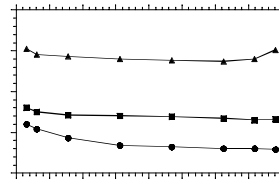
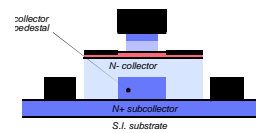
Urteaga, Rodwell, Pierson, Rowell, Brar, Nguyen, Nguyen: UCSB, RSC, GCS

Polycrystalline extrinsic emitter regrowth



Dennis Scott, Yun Wei

Collector pedestal implant



Yingda Dong

Monocrystalline Emitter Regrowth

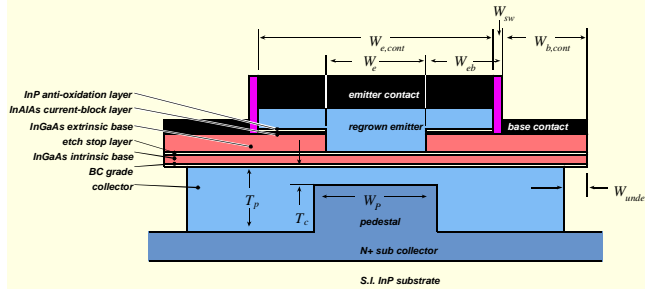
Christoph Kadow

Regrown base-emitter junction

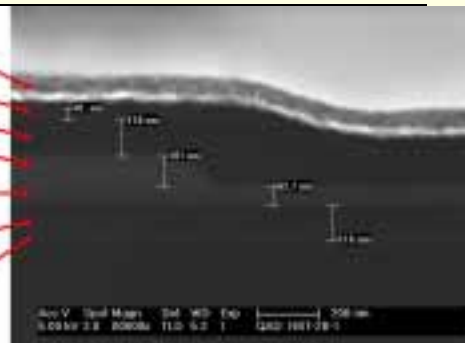
Emitter width defined by emitter window

Large-area, low-resistance emitter contact

Low-resistance extrinsic base



Contact metal
Emitter cap
InP emitter
I-base
I-base, setback and BC grade
InP collector
Etch stop



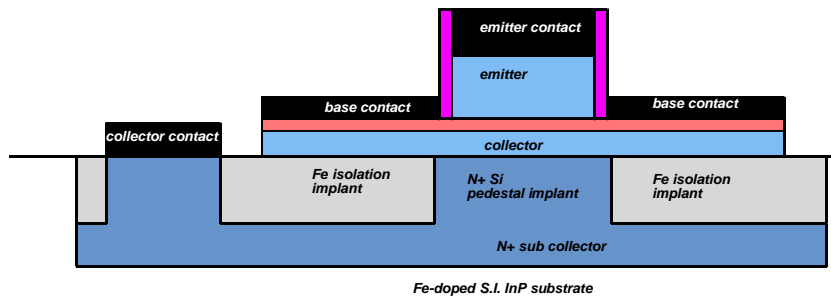
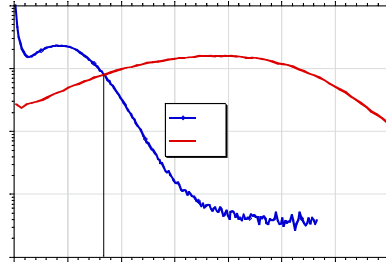
Double Collector Pedestal Implant

Navin Parthasarathy

Fe/Si dual Implantation
forms both subcollector and pedestal buried layers: does not require MBE regrowth

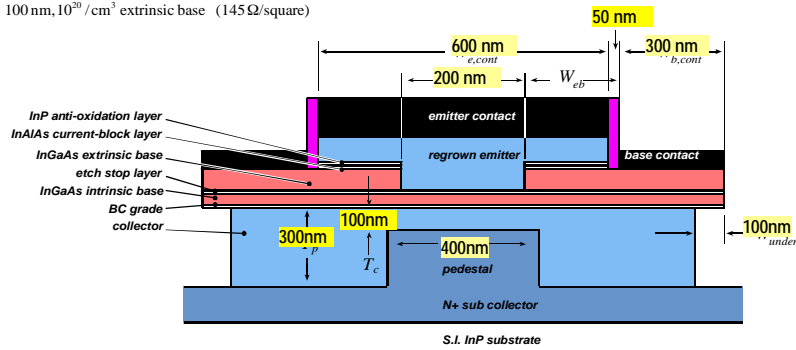
Collector pedestal
reduces C_{cb} at sides of emitter contact
increased transistor & logic speed

Patterned Implanted Subcollector
eliminates base pad capacitance
greatly increased power-delay product



200 nm Scaling Generation: Target 230 GHz clock rate

30 nm, $2 \cdot 10^{19} / \text{cm}^3$ intrinsic base
100 nm, $10^{20} / \text{cm}^3$ extrinsic base (145 Ω/square)



$$\rho_{c,emitter} = 15 \Omega \cdot \mu\text{m}^2$$

$$? R_{ex} A_E = 7.5 \Omega \cdot \mu\text{m}^2$$

$$\rho_{c,base} = 20 \Omega \cdot \mu\text{m}^2$$

$$J_e = 9.5 \text{ mA}/\mu\text{m}^2$$

$$0.3 \text{ ps wiring delay on collector bus}$$



$$f_{\text{clock (divider)}} \cong 232 \text{ GHz}$$

$$f_r = 495 \text{ GHz} \quad f_{\text{max}} = 606 \text{ GHz}$$

$$V_{br,ceo} \cong 4 \text{ V}$$

Doctoral Education

Graduates find jobs in research, advanced development
Future job \neq past research

Education in Fundamentals

E & M, Q.M., solid-state
need more thermodynamics, heat transfer, chemistry,
circuits & communication theory for device Ph.D.s

Learning how to do research

designing experiments & interpreting data
picking good research problems
independent critical thinking

Undergraduate Education

First 3 years

core subjects of discipline (electrical engineering)
broad training across math, science & engineering

Final year

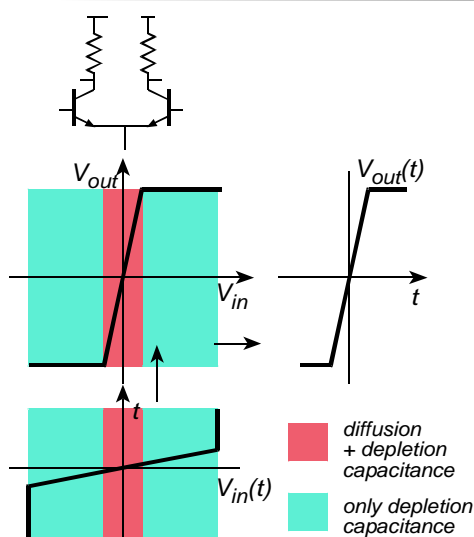
some industry-specific courses
independent design

Lower-division courses based on faculty research ?

usually too specialized for undergrad program,
potential to distract from core curriculum goals
appropriate budgeting of course content in curriculum

details of scaling laws

Why isn't base+collector transit time so important for logic?



Diffusion capacitance :

$$\begin{aligned} \delta Q_{\text{base}} &= (\tau_b + \tau_c) \delta I_C \\ &= (\tau_b + \tau_c) \frac{dI_C}{dV_{be}} \delta V_{be} \\ &= \frac{(\tau_b + \tau_c) I_C}{kT/q} \delta V_{be} \end{aligned}$$

...active only over kT/q voltage swing.

Under Large - Signal Operation :

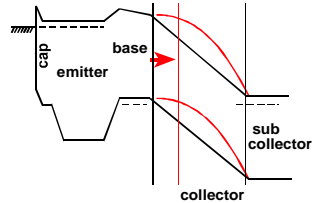
$$\begin{aligned} \Delta Q_{\text{base}} &= (\tau_b + \tau_c) I_C \\ &= \frac{(\tau_b + \tau_c) I_{dc}}{\Delta V_{LOGIC}} \Delta V_{LOGIC} \end{aligned}$$

Large - signal diffusion capacitance reduced by ratio of

$$\frac{\Delta V_{LOGIC}}{kT/q} \text{ which is } \sim 10:1$$

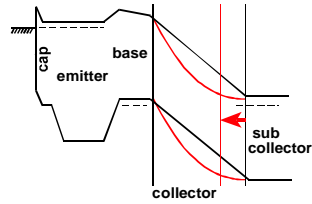
Depletion capacitances present over full voltage swing, no large-signal reduction

Scaling Laws, Collector Current Density, C_{cb} charging time



Collector Field Collapse (Kirk Effect)

$$V_{cb} + \phi > +(J/v_{sat} - qN_d)(T_c^2 / 2\epsilon)$$



Collector Depletion Layer Collapse

$$V_{cb, min} + \phi > +(qN_d)(T_c^2 / 2\epsilon)$$

$$? J_{max} = 2\epsilon v_{sat} (V_{cb} + V_{cb, min} + 2\phi) / T_c^2$$

Note that $V_{be} \cong \phi$, hence $(V_{cb} + \phi) \cong V_{ce}$

$$C_{cb} \Delta V_{LOGIC} / I_C = (\epsilon A_{collector} / T_c) (\Delta V_{LOGIC} / I_C) = \frac{\Delta V_{LOGIC}}{(V_{CE} + V_{CE, min})} \frac{A_{collector}}{A_{emitter}} \frac{T_c}{2v_{sat}}$$

Collector capacitance charging time is reduced by **thinning the collector** while increasing current

Emitter Resistance is a Key HBT Scaling Challenge

ECL Delay not well correlated with f_τ or f_{max} .

Largest delay is charging C_{cb}

$$C_{cb} \frac{\Delta V_{logic}}{I_C} = \frac{dA_{collector}}{T_c} \frac{\Delta V_{logic}}{J_e A_{emitter}} ; \text{ where } J_{e, max} \propto 1/T_c^2.$$

? $J_e \cong 10 \text{ mA}/\mu\text{m}^2$ needed for 200 GHz clock rate

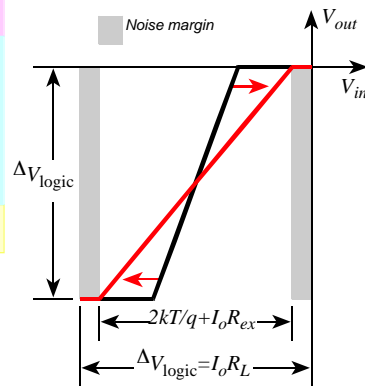
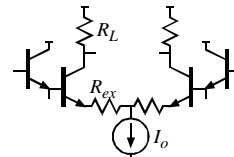
Voltage drop of emitter resistance becomes excessive

$$R_{ex} I_c = \rho_{ex} J_e = (15 \Omega \cdot \mu\text{m}^2) (10 \text{ mA}/\mu\text{m}^2) = 150 \text{ mV}$$

? large fraction of $\Delta V_{logic} \cong 300 \text{ mV}$.

Degrades logic noise margin

$\rho_{ex} \leq 7 \Omega \cdot \mu\text{m}^2$ needed for 200 GHz clock rate



other excess slides

Indium Phosphide HBTs

Superior Johnson Figure-of-Merit

electron velocity x breakdown field
increased breakdown at a given bandwidth
key technology for mm-wave power

Superior Electron Transport

increased bandwidth at a given scaling generation
150 GHz digital clock rate (static divider) at 500 nm scaling

Inferior Scaling & Parasitic Reduction

must be addressed !

Indium Phosphide vs. Silicon Germanium HBTs

Parameter	InP/InGaAs	Si/SiGe	benefit (simplified)
collector electron velocity	3E7 cm/s	1E7 cm/s	lower τ_c , <i>higher J</i>
base electron diffusivity	40 cm ² /s	~2-4 cm ² /s	lower τ_b
base sheet resistivity	500 Ohm	5000 Ohm	lower R_{bb}
comparable breakdown fields			

Consequences, if comparable scaling & parasitic reduction:

- ~3:1 higher bandwidth at a given scaling generation
- ~3:1 higher breakdown at a given bandwidth

Problem for InP: SiGe has much better scaling & parasitic reduction

Technology comparison today:

- Production SiGe and InP have comparable speed
- SiGe has much higher integration scales

Addressing scaling barriers: SiGe-like InP HBTs

Dennis Scott, Yun Wei, Yingda Dong

Objectives:

- SiGe-like high-yield planar process flow.
- Device structure without scaling limits.
- Capable of 250-300 GHz clock rates.

Scaling barriers for 250-300 GHz clock:

- Extremely low emitter resistance is needed.
- Need narrow 300 nm collector junction but also need ~300 nm wide base contacts;
- _ must decouple base & collector dimensions

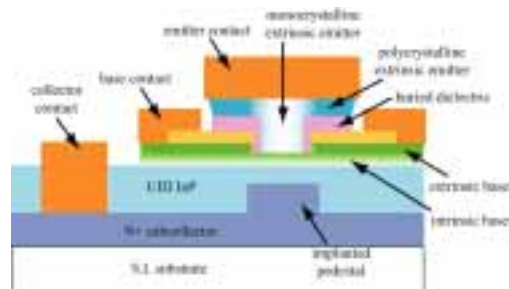
Approach:

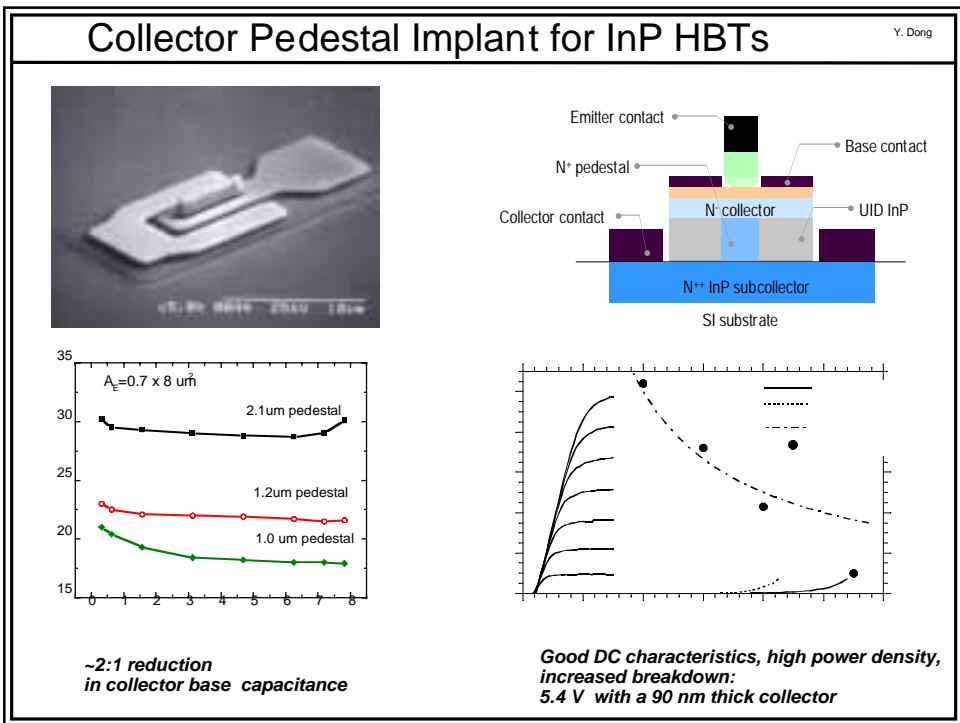
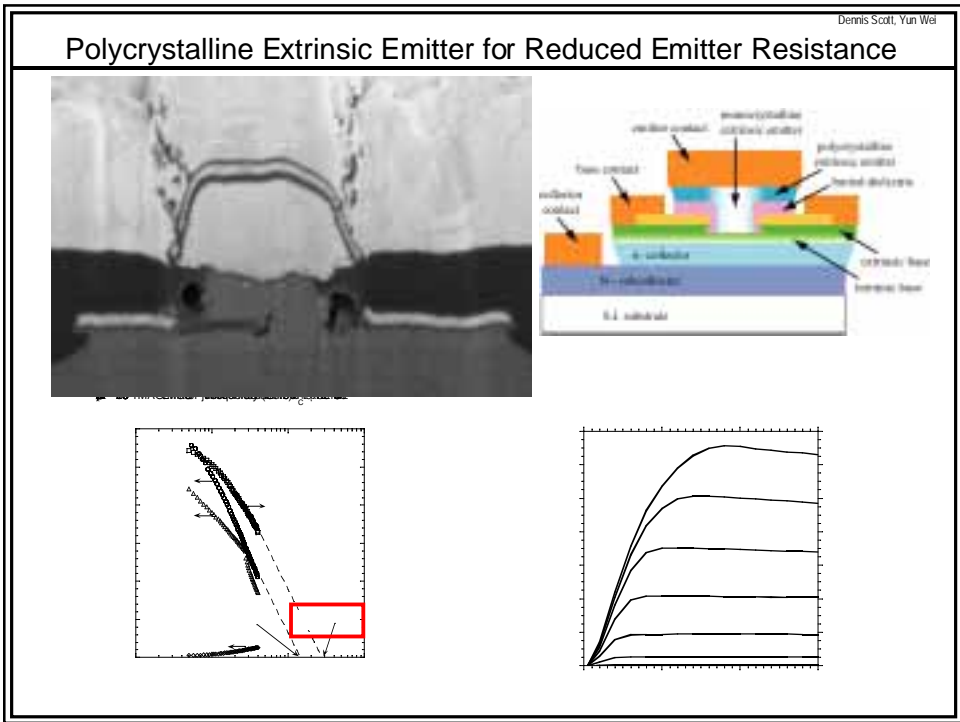
Pedestal collector

- decouples base and collector dimensions
- planar high yield process

Regrown submicron emitter

- SiGe-like process
- _ potentially high yield
- large emitter contact but small emitter junction
- _ low emitter resistance
- thick extrinsic base, thin intrinsic base
- _ reliability, current gain, base resistance





First Step: UCSB Dielectric Sidewall Emitter-base Process: Transferred to Rockwell June 2003

