Transparent and Stretchable Metal Electrodes

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Abstract:

Thin layers of lamellar-forming polystyrene-*block*-poly (methyl-methacrylate) (PS-*b*-PMMA) provide the templates for fabricating nanowires with a "fingerprint" morphology. The electrical characteristics of the nanowires were measured, and largely deviated from simulated devices due to high defect density. Their highly curved conformation makes the nanowires strong candidates for electrical testing on flexible substrates under compression and elongation. The wires' high transmittance on glass substrates reveals that they can function as transparent metal electrodes for use in electronic devices.

Introduction:

Diblock copolymers are macromolecules composed of two chemically distinct blocks, each a linear repetition of a particular monomer, that self-assemble to create periodic microdomains, each of which exclusively contains one of the polymers that make up the copolymer [1]. Varying volume fractions of the blocks generates different morphologies. When the volume fractions of the two blocks are similar, block copolymers self-assemble into the lamellar morphology [1], where the block with the higher volume fraction shows greater connectivity [2].

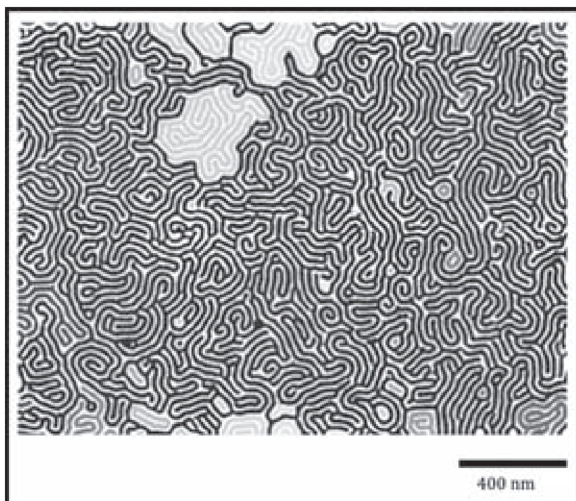

Figure 1: Color-coding for each PMMA backbone under a volume fraction f_{PMMA} of 0.55. (See cover for full color version.)

Figure 1 illustrates different continuous networks, each a different color, of PMMA, when the volume fraction of PMMA, f_{PMMA}, is 0.55 (see the cover of this publication for the full color rendition of this image). A single dominant network exists (blue) among small isolated networks. The high-connectivity, which offers redundant pathways from one point in the network to another, and the tortuous network conformation make block copolymers attractive for the fabrication of nanowires (NWs) [2-4]. Removing one block while preserving and using the other for patterning by thin-layer metal deposition allow for the formation of NWs. On transparent and stretchable substrates, these NWs should possess useful electrical properties, have high transmittance [5], and continue to perform well under mechanical strain.

Experimental Procedure:

Neutral brush solution was spin-coated and annealed onto cleaned glass slides or silicon wafers, allowing the block copolymer to orient perpendicular to the substrate [3]. Block copolymer blends were spun onto the neutral substrates and annealed to produce self-assembled thin films. The samples were exposed to ultraviolet light to break down the PMMA and developed using acetic acid, creating a polystyrene template. After five seconds of oxygen plasma to remove the brush, 1 nm of chromium (Cr) and 5 nm of gold (Au) were evaporated into the vacancies left by PMMA. Sonication in toluene removed the polystyrene, leaving the NWs on the substrate.

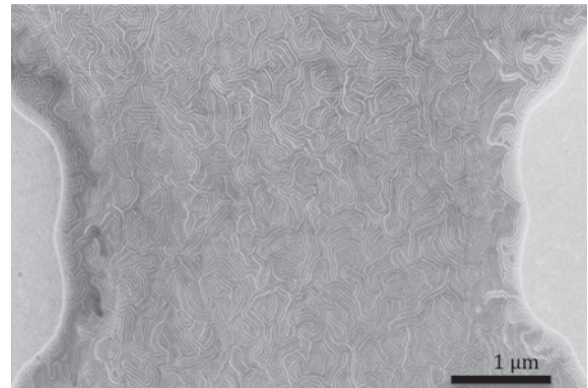

Figure 2: Nanowire network between micro-extensions from contact pads. Ideally, current must pass through these NWs.

Negative photoresist NR71 was spin-coated onto the nanowire samples for 40 seconds at 4000 RPM and exposed for 55 seconds using a mask-aligner and prepared mask containing contact pads with varying microwire features. The exposed samples were heated before development in RD6 for eight seconds, creating the pattern for the contact pads. After plasma treatment of 30 seconds, 10 nm of Cr followed by 100 nm of Au were evaporated, creating contact pads upon removing the remaining photoresist by sonication in acetone. Figure 2 illustrates the result of applying contact pads onto the nanowire samples, with a small gap between the microwire connectors to force current to pass through the NWs.

Current was measured using two probes from the probe station pressed onto the contact pads with potentials ranging from -10 millivolts to 10 millivolts applied across the samples.

Extinction coefficients for the NWs across the visible spectrum were measured on glass substrates using an Ocean Optics spectrometer and used to calculate transmittance.

Results and Discussion:

Figure 3 demonstrates the electrical characteristics of the NWs with $f_{PMMA} = 0.55$. A linear relationship between current and voltage exists for systems with continuous nanowire pathways between contacts, indicating a constant resistance. Increasing contact width increases sheet resistance because out-of-plane transport constitutes a larger fraction of the current for thin contacts. Simulations predicted that increased contact width would cause decreased sheet resistance, but defects in the fabricated NWs led to comparatively large resistances.

Figure 4 is a graph of the transmittance of two NW samples with $f_{PMMA} = 0.55$. The similar spectra indicate consistency in the transparency of these devices. Approximately 90-95% of light across the visible spectrum passes through the glass samples, demonstrating high transparency in these thin films.

Block copolymers are a useful template for fabricating NWs. The electrical characteristics of these NWs show potential for electronic devices while the transmittance through these samples displays the possibility for these NWs to become incorporated into devices requiring high transparency. These block-copolymer templated NWs are competitive with state-of-the-art materials in many solid-state devices. The high curvature of these NWs predicts that they will continue to function under strain and compression.

Future Work:

Improvements include producing defect-free samples for consistent device performance. A transfer process must be developed to test device performance under compression and strain. If the nanowires perform well under strain and compression, they can be incorporated into flexible solid-state devices.

Acknowledgments:

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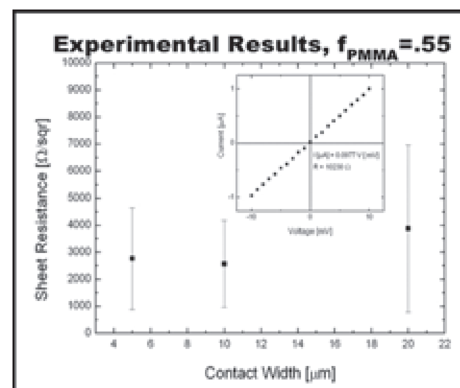

Figure 3: Sheet resistance and sample current-voltage curve with a nanowire network for $f_{PMMA} = 0.55$.

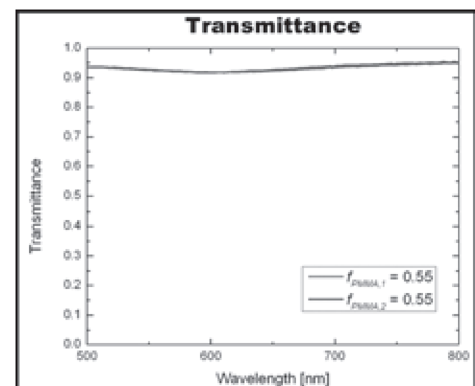

Figure 4: Transmittance across visible spectrum through two NW samples with $f_{PMMA} = 0.55$.

Silicon Carbide Device Simulation and Measurement

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Abstract:

Fabricating semiconductor devices is very expensive and time consuming, but most importantly, can be wasted if there is no clear understanding of what to look for. Computer simulations can accurately predict the fabrication process and device behavior, and can show how a device can be improved for better performance. Metal-oxide-semiconductor (MOS) capacitors are the basic components of MOS transistors, which can store or amplify charges and are the building blocks of integrated circuits. Using the simulation of an MOS capacitor, we wanted to develop silicon carbide (SiC) as a profitable semiconductor so that production of higher quality SiC can become a common process. With the simulation software Silvaco, we simulated an MOS capacitor using molybdenum (Mo) for the metal or gate, silicon carbide (4H-SiC) for the semiconductor and silicon dioxide (SiO_2) for the oxide. Then we measured different device parameters, including interface charge, oxide charge, and compared our results to a measured capacitance-voltage (C-V) curve of an MOS capacitor. Our purpose was to introduce SiC for more use in devices by; (a) simulating SiC MOS capacitors, (b) measure the C-V curve of the MOS capacitor with different characteristics, and (c) compare simulated with experimental data.

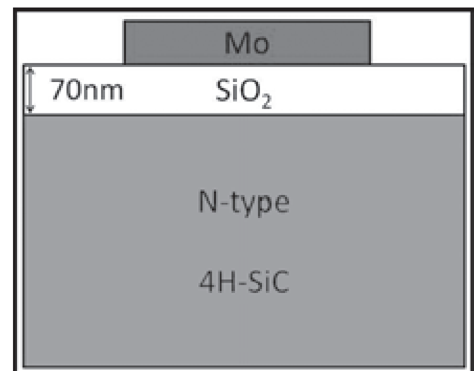

Figure 1: N-SiC MOS capacitor.

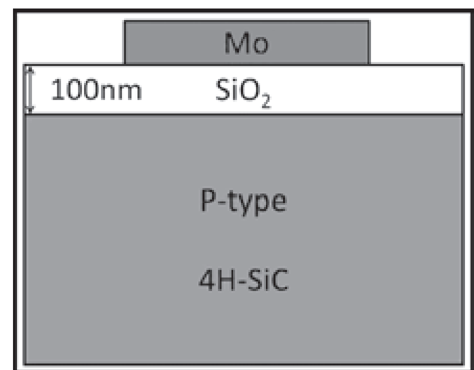

Figure 2: P-SiC MOS capacitor.

Experimental Procedure:

We first set up two MOS capacitors for Silvaco. Each had different oxide thicknesses and were named n-SiC (Figure 1) and p-SiC (Figure 2). We ran different simulations on each capacitor to gather information on their C-V curves. Each simulation was developed using five groups. Structure specification contained the mesh, region, electrode, and doping sections. Material models specification contained material, models, contact, and interface sections. Numerical method selection contained the method section. Solution specification contained log, solve, load, and save sections. Results analysis contained extract and tonyplot sections.

We exported the data from Silvaco (see Table 1, at right) and then; imported the data into Excel, normalized the data, refitted plots using Origin, and finally, compared the shifts and degradation between cases and ideal curve.

Silvaco
i. Run Time Environment
ii. Command File
iii. Structure Files
iv. ATLAS Device Simulator
v. Log Files and/or Solution Files
vi. Tonyplot

Results:

Our simulations of n-SiC and p-SiC devices showed a slight voltage shift and some degradation. In Figure 3, the ideal curve reaches depletion around 2 V. The interface state curve reaches depletion at 0 V, while oxide charges shift the depletion region to -2 V. In Figure 4, the ideal curve reaches depletion around 3.2 V. The interface state curve reaches depletion around 5 V and oxide charges shift the depletion region to 0 V.

Our results show how the SiC MOS capacitor is stable and efficient even with oxide charges and interface states.

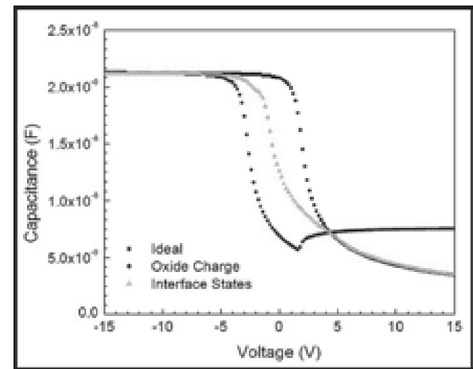

Figure 3: P-SiC results.

Conclusions:

SiC is a potentially important high-temperature semiconductor for power device applications and it can operate at temperatures much higher than Si. Using Silvaco, we simulated the effect of SiC oxide charges and interface traps on the behavior of MOS capacitors. The simulation software uses Poisson's, Carrier Continuity, and many other equations in Atlas to solve and gather data to generate the C-V curves. P-type MOS capacitors were able to retain the shape of the ideal C-V curve with only slight inversion due to the oxide charge. N-type MOS capacitors were also able to retain the CV curve shape, but with degradation due to interface states and lateral curve shift due to the oxide charge.

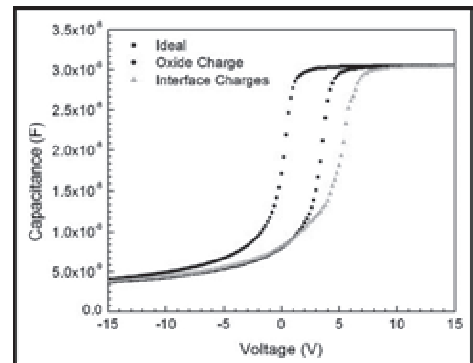

Figure 4: N-SiC results.

Future Work:

In the future, we hope to replace Si with SiC or take the technology to another level by building high-power devices using SiC. Even with defects, we have proven that SiC can still provide power and efficiency in devices. We will continue to research and simulate SiC and further prepare it for high-power use.

Acknowledgments:

I would like to thank Dr. Dieter Schroder and Xuan (Charlie) Yang for helping and guiding me throughout my research period. Thank you, Wei-Chieh Kao, for helping me organize the information we gathered concerning our studies. I would also like to thank Dr. Trevor Thornton and the staff of the Center for Solid State Electronics Research for use of lab equipment and assistance throughout the program. I would also like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and the National Science Foundation for their help in funding my research.

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Monolithic Integration of HEMT-Based Common Gate Oscillator with Active Integrated Antenna in the GaN Material System

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Abstract and Introduction:

This project focused on the preparation of high electron mobility transistors (HEMTs) and the design of a HEMT-based, single-lithography-layer oscillator with active integrated antenna circuit with target oscillation frequencies up to 100 GHz. HEMT devices are well known for their suitability in high frequency microwave circuits, possibly for two reasons. Firstly, HEMTs offer high electron densities, high breakdown voltages and superior drain currents as well as transconductance, making the devices suitable for high power, high frequency application. Secondly, because of reduction in columbic scattering and collisions, HEMT devices are known to display low-noise characteristics. These two factors combine make HEMTs amenable to nano-scale microwave oscillator design. Focus on reduction in device size is a growing demand and the prevalence of cellular phones, WiFi and other radio devices is increasing. Thus, the design of a low-cost, nano-scale microwave oscillating circuit is desirable. In this project, AlGaN/GaN HEMTs were fabricated with recessed gates in order to enhance aspect ratio, transconductance, cutoff frequency and maximum frequency of oscillation [1].

Methods:

This project can be divided into two main categories: HEMT fabrication and single-lithography-layer oscillator circuit design. In the former, AlGaN/GaN HEMTS, consisting of undoped GaN buffer layer, AlN spacer layer and AlGaN barrier layer, were grown on sapphire substrate. The device then underwent mesa isolation via argon sputtering techniques. Source/drain ohmic contacts were then patterned through a multilayered evaporation process in a Ti/Al/Ni/Au sequence [2]. After rapid thermal annealing, Schottky barrier Ni/Au gate contacts were placed using electron-beam lithography. Several series of HEMTs were fabricated with different gate lengths (100 nm, 300 nm, 500 nm) and source to drain spacings (3 μm, 3.5 μm, 4 μm, 4.5 μm, 5 μm). Argon dry etching was then used to create the recessed gate under the gate contact with recess depth of approximately 10 nm. For the oscillator design, the HEMT was the central device of interest. Thus, focus was given to HEMT fabrication and optimization regarding high frequency performance.

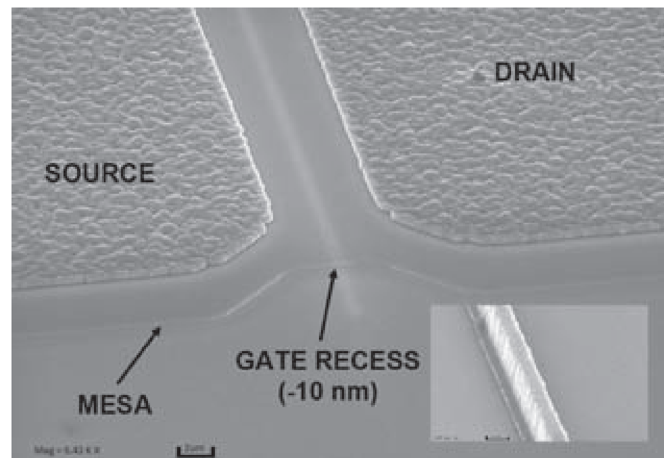

Figure 1: SEM micrograph of HEMT structure with gate recess. Insert shows SEM micrograph of gate recess.

Figure 1 shows a scanning electron microscope (SEM) image depicting an example of the HEMT structure without gate metallization: the mesa, patterned source/drain ohmic contacts, and the recessed gate structure. The inserted image shows an up-close SEM micrograph of the gate recess with gate metallization.

The second part of the project focused on the design of an oscillator and active integrated antenna with an oscillation frequency up to 100 GHz. A single-lithography-layer design is attractive because it can reduce manufacturing costs. To that end, a common gate oscillator circuit was selected for its simplicity and use of a voltage controlled transistor.

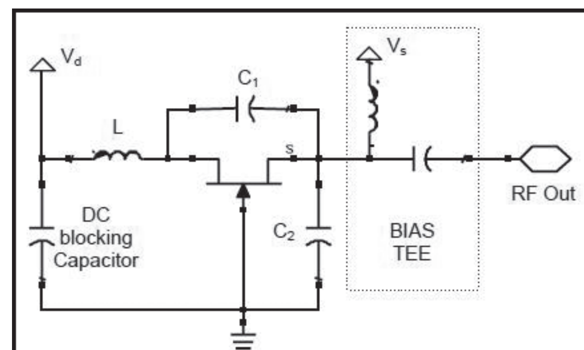

Figure 2: Common-gate oscillator circuit schematic.

Figure 2 shows the oscillator circuit schematic [3]. A circuit following this schematic was fabricated and tested successfully by Xu, et al., with gate-source bias of -5.3 V and drain bias of 20 V [3]. The remaining discrete circuit elements in the oscillator schematic include inductors and capacitors that comprise the LC tank subcircuit, DC blocking and a bias tee. Meanderline and interdigital geometries were selected to achieve single-lithography-layer realization of inductors and capacitors respectively. First, the capacitors were designed based on previously obtained empirical results. C1 and C2 in Figure 2 were designed as interdigital capacitors with eight structural fingers, finger spacing of 1 μm, finger width of 200 nm and overlap length of 8 μm. This design yielded a capacitance of roughly 2.7 fF.

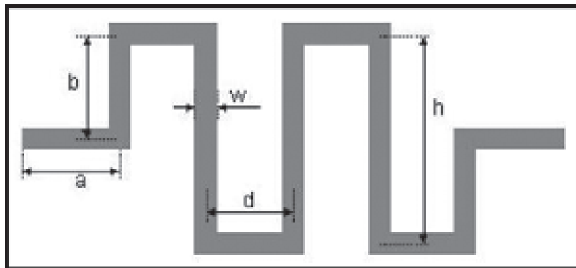

Figure 3: Meanderline inductor with characteristic dimensions.

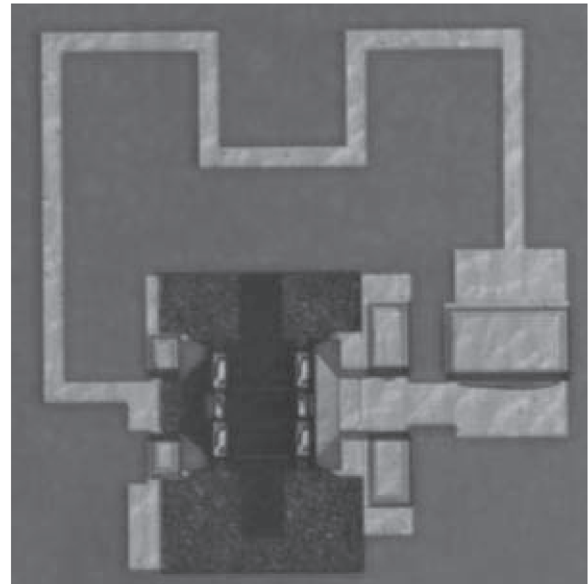

Figure 4: Example oscillator layout.

Figure 3 shows a meanderline inductor with characteristic dimensions [4]. A five-turn meanderline inductor with a = 140 μm, b = 160 μm, d = 80 μm, and h = 320 μm and thickness of 8 μm would yield an inductance of approximately 1.5 nH [5]. With these inductor and capacitor values, the tank circuit was calculated to oscillate at around 111 GHz.

The DC blocking capacitor was designed to achieve a capacitance approximately ten times that of C1, C2. To that end, the number of finger structures was increased to 24, and the overlap length was approximately 24 μm, while maintaining the same finger spacing and finger width as C1 and C2, or 1 μm and 200 nm respectively. The source bias tee structure was realized using a planar radial stub. More specifically, an oscillation frequency of 111GHz of an electromagnetic wave yielded a wavelength, λ, of approximately 2.68 mm. A transmission stripline, orthogonal to the RF signal stripline, of length $\lambda/4$ led to the radial stub. The stub angle was 90° with radius of $\lambda/4$.

Finally, for its wide-band characteristics, a simple bowtie antenna will be used as the integrated antenna element.

Future Work:

Future work includes arranging the described circuit elements for single-lithography-layer fabrication.

Furthermore, integration of coplanar waveguides for signal transmission is needed to improve signal quality and provide a better means to probe and inject signals. Figure 4 shows an example oscillator layout [3].

Acknowledgements:

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Characterization of Phase Change Materials for Radio Frequency Applications

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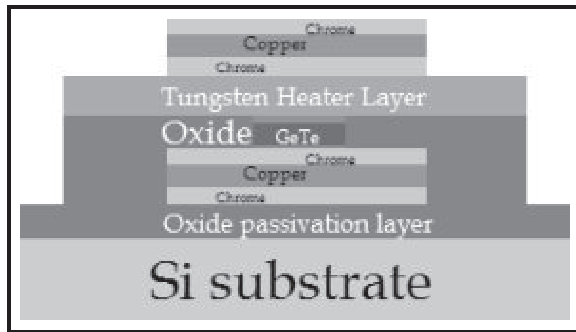

Figure 1: Cross-sectional schematic of device structure.

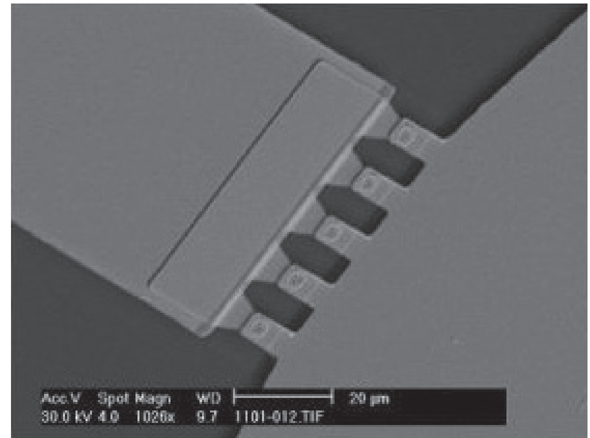

Figure 2: SEM image of a device with five 2 × 2 µm² vias.

Abstract:

Phase change materials are a class of compounds that can alter states between crystalline and amorphous when specific heating conditions are applied to them. Due to fast switching speed, long life cycles, and potential for high-density integration, these materials are currently being investigated for use in non-volatile memory applications [1, 2]. The focus of this project was to characterize a specific phase change material, $Ge_{50}Te_{50}$, to determine its possible capabilities for radio frequency (RF) applications. This material was chosen for use in RF switches due to its low crystalline state resistance and a high OFF/ON resistance ratio. The method of characterization was to fabricate simple ohmic switches and then apply voltages or currents with different pulse shapes and durations in order to obtain the phase transitions. The goals of this project were to optimize the switch design and fabrication method to achieve a low ON resistance and high OFF/ON resistance ratio, and to optimize the biasing conditions to obtain repeatable and reliable phase transitions. An extension of the project was investigating the effects of direct heating versus indirect heating. If the switches are successful, this material can be incorporated to design more advanced passive elements such as filters, phase shifters, and antennas.

Introduction:

Previous work has been reported on the use of phase change materials from GeSbTe (GST) compounds in non-volatile memory applications. There has been a recent report on the application of $Ge_{50}Te_{50}$ in switchable inductors [3].

The larger scope of this project included characterizing the $Ge_{50}Te_{50}$ material using simple ohmic switches, then moving on to the characterization of more complicated designs, such as filters, to determine the overall use of the material in radio frequency applications.

The goals of this internship were to develop fabrication processes for implementing phase change switches (aka phase change vias). Materials in the stack were deliberately chosen, the specific thickness for the different layers was determined, and the etch times and recipes were optimized through fabrication of several test wafers and characterization steps. Once the optimal design was determined, the devices were fabricated and direct heating measurement techniques were employed to transition the vias.

Experimental Procedure:

The switches were fabricated on silicon wafers. All liftoff molds and etch guides were created using photolithography. In order to isolate the devices from the silicon, wafers were passivated with a 2 μm thick silicon dioxide layer deposited by plasma-enhanced chemical vapor deposition (PECVD). Then the bottom electrode was deposited in an evaporator. The bottom electrode consisted of three layers, 300 Å NiCr, 5000 Å Cu, and 300 Å NiCr. After liftoff, 3000 Å of oxide was deposited using PECVD, and then etched to form an insulation layer on top of the tips of the electrodes, with a via directly over the electrode. The 100 nm $Ge_{50}Te_{50}$ layer, with 50 Å Ti adhesion layer and 100 Å Ti overcoat layer, was deposited on this via by sputtering. $Ge_{50}Te_{50}$ liftoff was completed, and then a heater layer of 2500 Å of W was deposited using sputtering. Liftoff of the heater layer was completed, and then the top electrode was deposited. The top electrode also consisted of three layers, 200 Å NiCr, 3000 Å Cu, and 200 Å NiCr. After liftoff of the top electrode, the devices were complete.

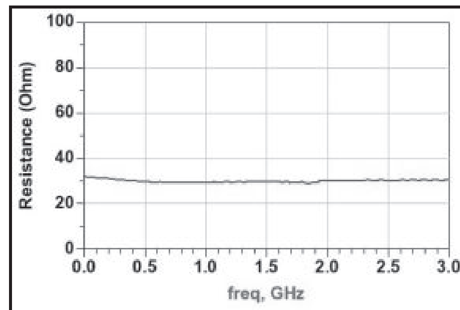

Figure 3: Crystalline resistance of the device shown in Figure 2.

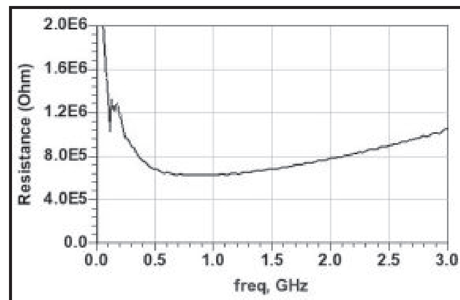

Figure 4: Amorphous resistance of the device shown in Figure 2.

Characterization results reported here were obtained using phase change vias with a tungsten layer in the stack, as discussed earlier. Repeatable phase transitions were obtained. The crystallization pulse was 200 μs with a rise and fall time of 200 μs, and amplitude of 1 V. The crystalline resistance was 100-300 Ω; however, the resistance of the electrodes alone was measured to be around 75 Ω, yielding an ON resistance of ~30 Ω for the phase change layer (see Figure 3). The pulse to amorphize was 2 μs with a rise and fall time of 5 ns and amplitude of 2.5 V. However, the amorphization was easily obtained with several different pulses of different durations with amplitudes of 1.5 V or higher. The amorphous resistance was 800 kΩ -1 MΩ (see Figure 4).

While this OFF resistance is higher than previous work [1], and the OFF/ON resistance ratio is between 10^4 and 10^5, the ON resistance could still be improved upon.

Given these results, $Ge_{50}Te_{50}$ has good potential for use in RF applications.

Future Work:

While basic characterization of the material was completed during this internship, there remain many variations to be explored.

Further investigation could be conducted into the effect of various sputter pressures and powers on the $Ge_{50}Te_{50}$ material. Different thicknesses of $Ge_{50}Te_{50}$ for the via could have effects on the phase change conditions and should be further characterized. Also, the variations between direct and indirect heating should be examined.

This summer research has shown that $Ge_{50}Te_{50}$ is a promising candidate for RF switching applications and can be used in tunable inductors, capacitors, and advanced devices such as antennas, phase shifters, and filters.

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Fabrication and Characterization of Vertical Silicon Nanopillar Schottky Diodes

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Introduction:

Schottky (rectifying metal-semiconductor) contacts have widespread use, particularly in high frequency [1] and high power electronic devices [2]. It is important that Schottky diodes be miniaturized to preserve their functionality as devices shrink to the nanoscale [3], for applications such as voltage clamping, rectification in switched-mode power supplies, and reverse current protection in photovoltaic systems [4]. Standing upright, nanopillars can access vertical dimension in device fabrication, which is recognized as an important step in maintaining and/or surpassing Moore's law [5]. Here, we present a low temperature (no thermal oxide required), top-down process for fabricating arrays of vertical n-type silicon nanopillar Schottky diodes that can be incorporated into planar complementary metal oxide semiconductor (CMOS)-integrated circuits. We also characterize our metal-semiconductor (nickel-silicon) contacts and note that they differ from planar diodes.

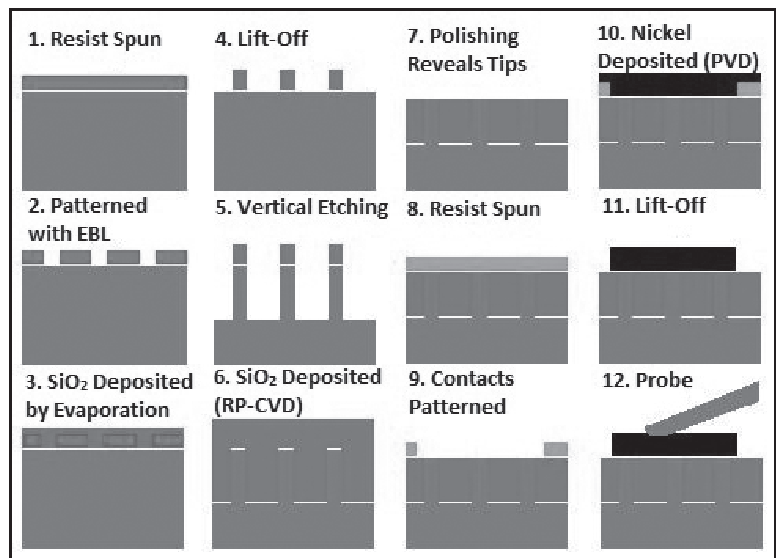

Figure 1: Schematic representation of fabrication process (not to scale).

Experimental Procedure:

A schematic representation of the fabrication process is shown in Figure 1. First, a hard mask of square-shaped SiO_2 islands (side lengths of 40 to 100 nm) was formed in arrays with a 4 μm pitch on an n-type (~ 2×10^{15} cm^{-3}) silicon (Si) substrate. This was done using electron beam lithography to expose arrays on a spin-coated 200 nm thick layer of 950K poly(methyl methacrylate) (PMMA). After developing the pattern at room temperature, roughly 50 nm of SiO_2 was deposited with electron-beam evaporation. The excess resist was dissolved in acetone, lifting off the oxide layer except for the SiO_2 islands.

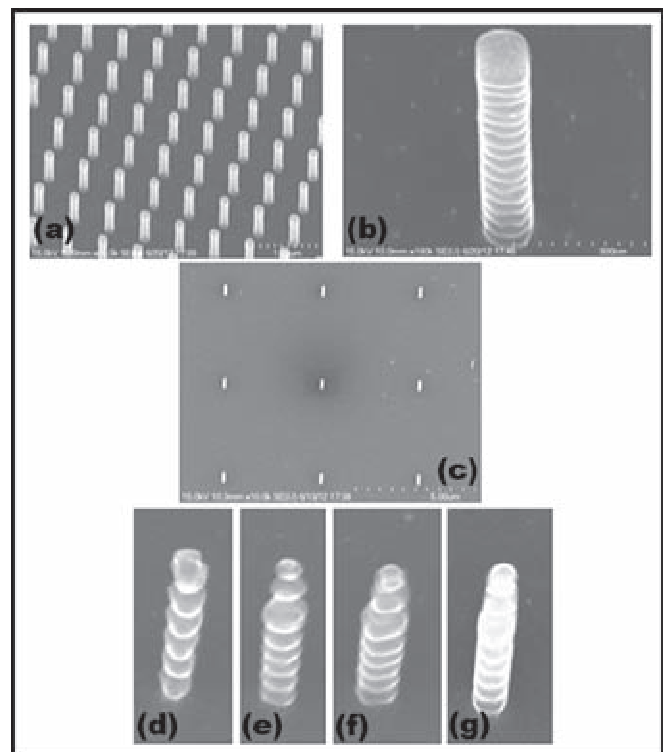

Figure 2: (a) SEM image of a 500 nm pitch array of 100 nm nanopillars after Bosch process using 4 sec etch, 2.5 sec deposition cycle. (b) Close-up of a 100 nm nanopillar in (a). (c) 4-micron pitch array of 100 nm diameter nanopillars obtained from using 8 sec etch, 5 sec deposition cycle. (d)-(g) Single nanopillars sized 40 nm, 60 nm, 80 nm, and 100 nm processed as in (c).

With this hard mask, nanopillars were formed with deep reactive-ion etching (RIE) making use of a Surface Technology Systems inductively coupled plasma (STS ICP) system. Employing what is known as the Bosch process, alternating modes of nearly anisotropic etching (using sulfur hexafluoride) and polymer deposition (using octafluorocyclobutane) produced vertical nanopillars approximately 1 μm tall.

Due to a small, unavoidable isotropic component in the etching mode, the nanopillar sidewalls were considerably scalloped. We were able to reduce the extent of scalloping by modifying the etching and deposition times during RIE. The resulting nanopillars are shown in Figure 2.

Finally, for support and electrical insulation, a conformal layer of SiO_2 was deposited using remote plasma chemical vapor deposition (RP-CVD). Chemical-mechanical polishing (CMP) then partially removed this layer, revealing the Si tips. 100 nm of nickel was sputtered after another electron beam lithography step patterned the contact windows. Excess nickel was lifted-off by ultrasonic agitation in an acetone bath, and rapid thermal annealing (RTA) formed a nickel silicide-silicon contact, creating the Schottky effect.

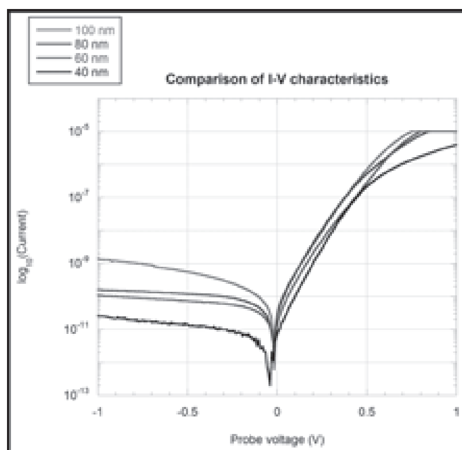

Figure 3: I-V characteristics of an array of 400 nanopillars of different diameters.

Results and Conclusions:

The resulting diodes' current-voltage characteristics (Figure 3) were analyzed to extract the barrier height, Φ_B; the ideality factor, n; and the series resistance, r_s in the thermionic current-voltage expressions (1) and (2):

$$I = I_s(\exp[q(V - Ir_s)/nkT] - 1) \quad (1)$$

$$I_s = AA^*T^2\exp[-qV/kT] \quad (2)$$

Where $q = 1.6 \times 10^{-19}$C, $k = 1.381 \times 10^{-23}$J/K, $T = 294$K, A is the diode contact area (assumed circular), and A^* is Richardson's constant, 112A/cm^{2}K^2 [6]. Typical values were 0.6 to 0.7eV for Φ_B, 1.5 to 2.5 for n, and 10 to 100 kΩ for r_s. These results confirm Schottky behavior.

An unexpected outcome that differentiates these diodes from planar diodes was non-ideal current scaling with respect to both number of diodes and radius. For the former, a linear relation was expected since the diodes are probed in parallel, but not observed: current ratios between the 40, 160, 240 to the 400 pillar array were roughly 1%, 10%, and 15%, respectively, compared to the expected 10%, 40%, and 60%. For the latter, dependence on area (radius squared) was expected because the heights of the nanopillars are consistent, but the power was found to be about 1.2 instead of 2. This indicates a dependence on perimeter size, and hence the increased importance of surface states due to a higher surface area to volume ratio.

Future Work:

Further research is needed to minimize scalloping to optimize nanopillar quality. The main parameter to be altered in this work should be the etch rate, in order to minimize the isotropy of the etching mode. Additionally, the non-ideal current scaling must be researched to be fully understood. One theory to account for this with respect to number of diodes is that a combination of inconsistent numbers of unintended "stray" nanopillars and faulty nanopillars are contacted with nickel, varying the actual amount probed from the assumed. Electron beam induced current (EBIC) is a method that could test this theory by illuminating the functioning diodes.

Acknowledgements:

Thank you to my mentor, Nishant Chandra, and my PIs, Drs. Stephen Goodnick and Clarence Tracy, for their time and effort. Additionally, to the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and the National Science Foundation for funding.

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Electrochemical Deposition of Polythiophene onto Carbon Nanotube Arrays

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Introduction:

Each new generation of electronic products uses high-speed microchips that squeeze more transistors/power and performance into even smaller packages. This leads to excess heat generation within the semiconductor components, which causes the chip to fail over time. Heat sinks were added to help cool these chips. Heat sinks allow for the heat to dissipate from the chip to the heat sink to a cooler ambient, like air. When the heat sink and microchip were first put together, it was found that the two surfaces formed contact points and air gaps. Contact points are areas where the chip and the sink are connected together and heat can travel successfully from the chip to the sink. Air gaps are all the areas between the contact points where heat has trouble crossing from chip to sink. Since air is an insulator, the heat builds up on the chip at these air gaps and become hot spots, which lead to device failure.

Thermal interface materials (TIMs) were used to eliminate the air gaps within the component and consequently provide a path of heat removal from the component package surface through the heat sink and heat spreader. Therefore, TIMs are integral part of overall electronic product design. An ideal TIM will have both high thermal conductivity and the ability to conform to the surfaces well. These are two major characteristics that determine the total thermal interface resistance of different surfaces. In order to improve the life and performance of electronic devices, TIMs with improved thermal resistance are in urgent need.

Carbon nanotubes (CNTs) are being researched as a favorable TIM because of their high thermal conductivity. CNTs allow for vertically aligned columns to transfer the heat from the chip to the sink [1-4]. However, the poor adhesion of CNTs to the substrate limits their use as TIMs for high power devices. In order to improve the performance of CNT based TIMs, the problem of adhesion has to be addressed.

The goal of this current research was to develop a hybrid material that combined the high thermal conductivity of carbon nanotubes (CNTs) and exceptional mechanical compliance of polythiophene (Pth). We selected Pth as the polymer of choice as it is an electroactive polymer and can be deposited electrochemically. Additionally, Pth is thermally stable up to the device operating temperature.

Experimental Procedure:

In a typical fabrication process, diced 2 × 3 cm silicon wafers were cleaned extensively. Two different catalyst seed layers — 100 nm titanium (Ti) / 10 nm aluminum (Al) / 3 nm iron (Fe), and 40 nm silicon oxide (SiO_2) / 10 nm nickel (Ni) — were deposited using a Denton Explorer e-beam evaporator. We used three minutes of low pressure chemical vapor deposition on the Ti/Al/Fe samples and 15 minutes of plasma-enhanced chemical vapor deposition on the SiO_2/Ni samples to induce CNT growth on the wafers using acetylene as precursor gas in a Black Magic PECVD reactor.

Finally, the CNT arrays were coated with Pth using three electrodes electrochemical deposition. The current was sent from the working electrode, the silicon wafer, to the

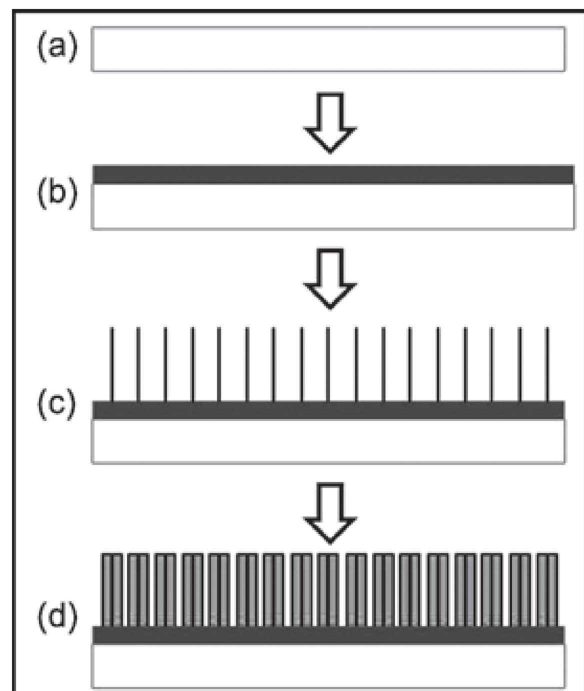

Figure 1: Fabrication process. (a) Silicon wafers. (b) Deposition of catalyst layer. (c) CVD for CNT growth. (d) Pth electrodeposition.

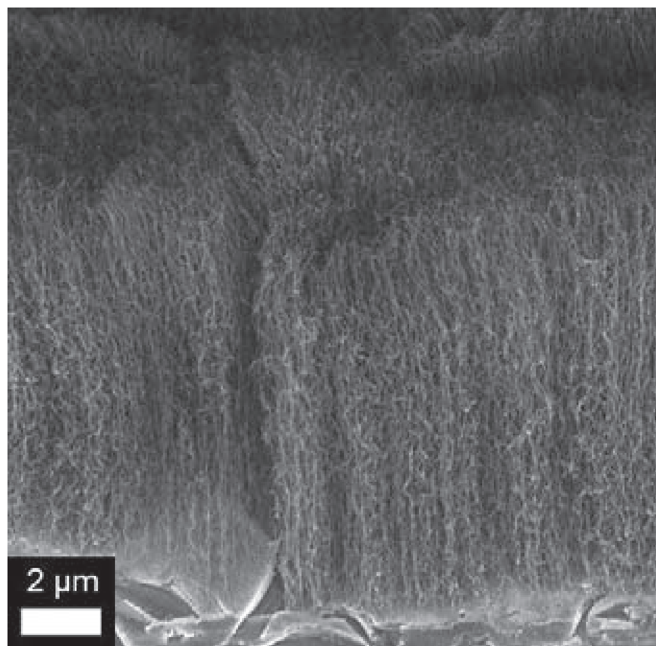

Figure 2: SEM image of Ti/Al/Fe CNT growth.

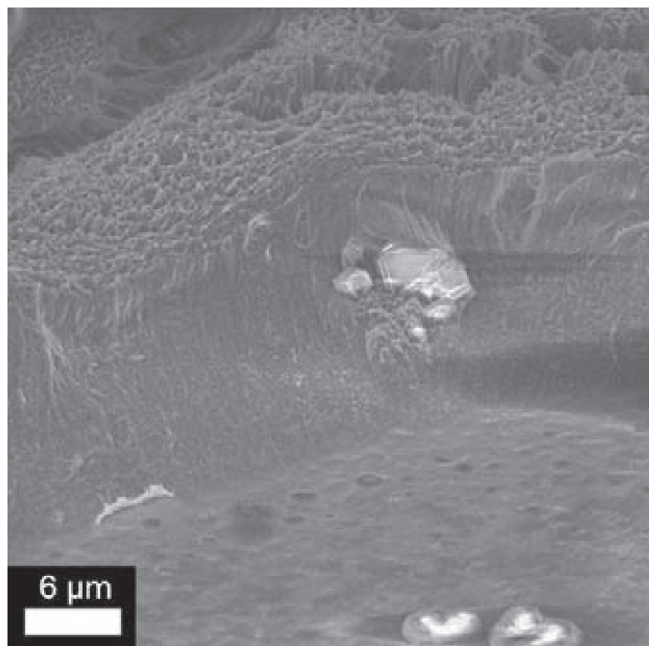

Figure 3: SEM image of Pth coating CNT arrays.

counter electrode, which was immersed in Pth solution, with the reference electrode measuring current. We used cyclic voltammetry to be able to control the amount of Pth coated on the CNTs and ran samples using 5, 10, and 15 cycles.

To evaluate the orientation, thickness, height, and density of the CNTs and Pth coating on CNTs, we used a scanning electron microscope (SEM). A typical fabrication procedure is outlined in Figure 1.

Results and Conclusions:

After CVD, we found that the Ti/Al/Fe catalyst layer produced the desired CNT arrays, and we used this catalyst layer for further experiments. As shown in Figure 2, the vertically aligned arrays measuring about 10-12 μm tall and a density of about $2 \times 10^{-7} cm^2$ was obtained in a typical LPCVD recipe with a three minute growth time.

The CNT arrays were successfully coated with Pth through electrochemical deposition using cyclic voltammetery (Figure 3). However, we were only able to coat a thick layer of Pth on top of the CNTs and further modification of electrochemical process is required to achieve a conformable coating.

Future Work:

Future research will involve quantifying how much Pth is deposited per cycle during deposition. This will allow us to control coating with the amount of cycles. In addition, we need to determine how to coat the individual CNTs and not just the whole array. Using a photoacoustic technique, we plan to measure the thermal resistance for our hybrid structures to compare to other TIMs. Additionally, we will run adhesion and electrical/thermal conductivity tests in order to ensure our TIM will adhere to the surfaces as predicted, without affecting the thermal performance. The long-term plan is to develop this material into an effective Thermal Interface Material that can be used in electronics to improve current technology and increase the life-span of electronics.

Acknowledgements:

I'd like to thank my Principal Investigator, Dr. Baratunde Cola, and my mentor, Dr. Virendra Singh, for their help with my research, and the opportunity to conduct it at Georgia Tech. I'd also like to thank the Georgia Tech IEN coordinators Leslie O'Neill and Nancy Healy. Thank you to the NEST group for their lab facilities and help. Finally, I'd like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program and the National Science Foundation (NSF) for their help and funding.

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Understanding Performance Limitations in Organic Transistors

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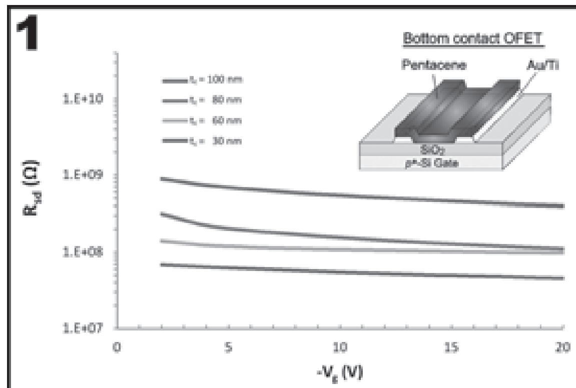

Figure 1: Contact resistance for varying pentacene thickness in TC OFETs (inset).

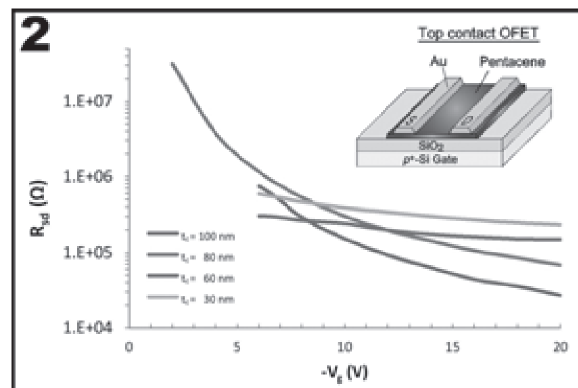

Figure 2: Contact resistance for varying contact thicknesses in BC OFETs (inset).

Introduction:

Organic field-effect transistors (OFET) are critical components of many prospective organic electronic products [1], but their performance is limited by poor charge injection and weak charge transport, manifesting as high contact resistance and low mobility. The goal of this work was to understand performance limitations in pentacene-based OFETs by varying device architecture and processing to empirically demonstrate optimal design parameters.

Experimental Methods:

Pentacene OFETs of top/bottom-contact (TC/BC) and bottom-gate (BG) configuration were fabricated (Figures 1 and 2). BC devices suffer from contact effects because molecular self-organization is disrupted, resulting in poor film morphology near the contacts. Small charge injection area (~ contact thickness) is also believed to limit performance in BC OFETs. In this study, BC devices with various contact thicknesses were fabricated to explore both issues. Compared to BC OFETs, TC OFETs perform better, demonstrating lower contact resistance and higher mobility. The OSC film is not disturbed by contact deposition and, furthermore, TC OFETs have larger charge injection area as the entire contact surface contributes to injection. However, in TC OFETs, charge carriers must cross the entire OSC film to reach the channel, causing high access resistance. Meanwhile, large numbers of traps limit charge transport. So, TC devices with different pentacene film thicknesses and diverse dielectric treatments were fabricated to understand contact resistance and trap origins.

Current-voltage (I-V) characterization and low-frequency noise (LFN) measurements were performed in ambient conditions. The contact resistance (R_{sd}) was evaluated by the modified transfer length method [3] with devices having different channel lengths. Intrinsic low-field mobility (μ_0) was extracted via the Y-Function method [4]. Normalized power spectral density of drain current fluctuations at $f = 20$ Hz were plotted against drain current to identify noise mechanisms. The normalized noise spectra were accurately modeled by carrier number fluctuations induced by charge trapping/detrapping and, thus, a surface equivalent trap density (N_{ST}) was extracted.

Results and Discussions:

The R_{sd} of BC OFETs is depicted in Figure 1 as a function of gate voltage (V_G). Surprisingly, R_{sd} increased with contact thickness, contrary to the expectation that charge injection should be enhanced by greater charge injection area. Our results indicated this enhancement was negligible and the small grain contact region played a dominant role. Thicker contacts produced a steeper edge profile, causing poorer molecular packing. Charge injection was limited by this

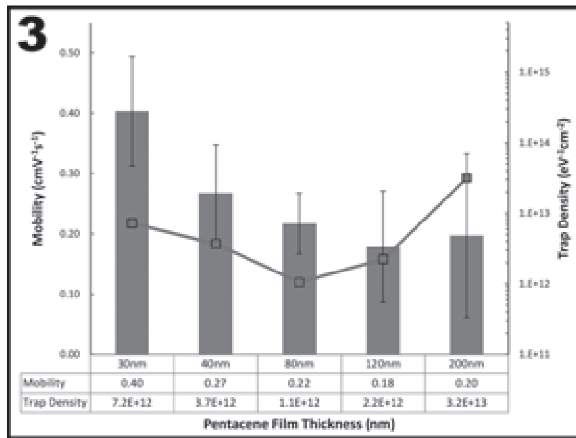

Figure 3: Intrinsic mobility (left axis) and trap density (right axis) for several pentacene thicknesses.

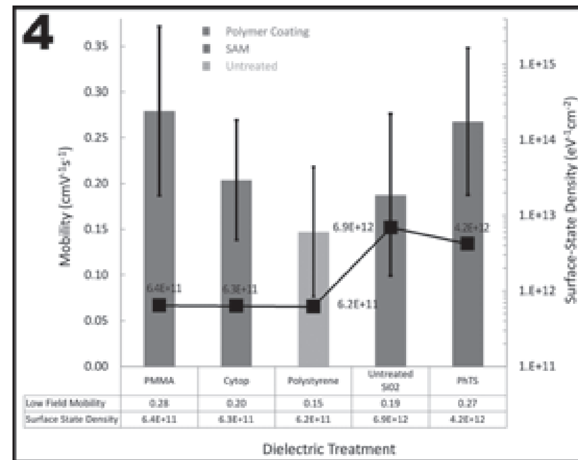

Figure 4: Intrinsic mobility and surface-state density for several dielectric treatments.

highly resistive zone, yielding high contact resistance and reduced mobility.

Figure 2 illustrates the R_{sd} in TC OFETS with various pentacene film thicknesses (t_{SC}). Simulations showed that R_{sd} increased drastically with t_{SC} as VG dependence weakened [2]. The former was due to longer vertical transport required in thicker films, and the latter was from weaker charge concentration modulation by V_G.

The present results qualitatively match simulations, but the range of magnitudes spanned is much smaller. This non-ideality is likely because of contact metal (Au) diffusion into the pentacene film, which may make the actual t_{SC} smaller than the nominal thickness. Future experiments will address this by alternative fabrication techniques such as contact lamination.

Besides determining charge injection, t_{SC} affects charge transport in the channel. In Figure 3, mobility μ_0 decreased with t_{SC}. To understand this, the trap density (N_{ST}) by LFN was plotted against t_{SC} in Figure 3, showing an inverse trend to that of mobility. High N_{ST} in the film might be due to poor film quality and interfacial traps. This agreed with the understanding that thicker grain boundaries will produce more deep traps. Indeed, the nearly proportional dependence of N_{ST} on t_{SC} implied uniformly distributed traps within the OSC bulk.

It appears mobility variation was not strictly due to charge trapping. One possible interpretation is limited charge injection in thicker films, as charge must traverse the contact region mainly by hopping. Since the contact provided insufficient charge to the channel, the apparent mobility was limited.

The OSC/dielectric interface is crucial to transport. Figure 4 illustrates the mobility and the surface state density (N_{SS}, deduced by sub-threshold swing) in TC devices with different treatments of the SiO_2 dielectric. PMMA and PhTS-SAM gave the comparably highest mobility and untreated SiO_2 had lower mobility, as expected. The small N_{SS} for polymer treatments (Cytop, PMMA, and polystyrene) showed high interface quality, probably due to the similar material properties between pentacene and polymeric dielectric treatments. Strikingly, a high N_{SS} was obtained for PhTS-SAM treatment though SAM layers typically improved mobility. Untreated SiO_2 showed the largest N_{SS}, presumably from charge trapping hydroxyl groups.

The N_{ST} by LFN indicates pentacene film quality also strongly depends on dielectric, providing additional explanation for the mobility variation. The N_{ST} in untreated SiO_2 was the largest, followed by PhTS-SAM. Approximately an order of magnitude lower N_{ST} obtained in PMMA treated devices indicated a higher quality pentacene film.

Conclusions:

Fabrication and measurement of pentacene-based OFETs with varying device architectures and processing methods enabled deeper understanding of OFET performance limitations. Choosing a proper contact thickness that preserves the film morphology is critical to optimizing charge injection in BC OFETs. For TC OFETs, a thin but a high quality OSC film is key to strong charge injection in the contact and efficient charge transport in the channel. In addition, polymeric dielectrics improved OSC film quality and reduced the interface traps. Future efforts will examine a larger parametric range of device parameters to better understand trends in trap density and contact resistance as well as define changes in the film morphology.

Acknowledgements:

Dr. Yong Xu, Tsukagoshi-sensei, NNIN iREU, NSF, NIMS.

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Spin Torque Ferromagnetic Resonance with the Spin Hall Effect

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Abstract:

The goal of this REU project was to measure the film thickness dependence of spin-torque ferromagnetic resonance (ST-FMR) induced by the spin Hall effect. The spin Hall effect occurs when a current is sent through a conducting, nonmagnetic material, and spin-up and spin-down electrons are separated on either side of the material. This creates what is called a spin current, transverse to the electron current. In this research, the spin Hall effect was used as a source for spin injection in a nonmagnetic, conducting metal to create magnetic precession in an adjacent ferromagnetic film. The purpose of these experiments was to help achieve a better understanding of the spin Hall effect in various materials and the dynamics of spin Hall induced ST-FMR. Photolithography, ion milling and sputter deposition were used to define bilayer structures with contact pads. With these devices, we measured the ferromagnetic resonance signal to quantitatively determine the spin current injection and spin Hall angle.

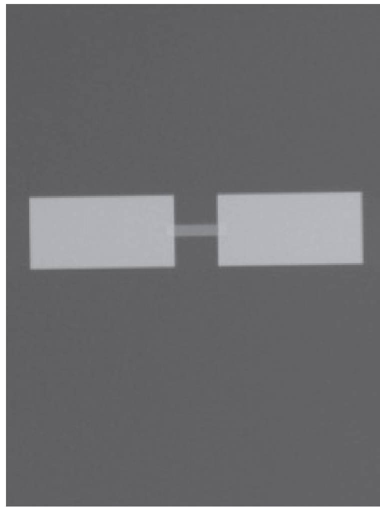

Figure 1: An image of the bilayer device between to copper contacts.

Introduction:

Spin transfer by the spin Hall effect has already been demonstrated in research performed by both the Ralph and Buhrman groups at Cornell. Past experiments in the area of spin manipulation have used magnetic materials in order to create spin current and to inject spin angular momentum into ferromagnetic materials. What is unique about this project is that we used the spin Hall effect in a nonmagnetic material to create this spin current, which is more energy efficient and a novel way of doing spin manipulation.

Experimental Procedure:

There were several steps to the fabrication process for the spin torque device. The first step involved sputtering different thicknesses of permalloy (Py) for each device made (varying from about 4 nm to 7 nm for four different devices) and then 3 nm of platinum (Pt). We did our first lithography step to define the basic device structure with ion milling. After this, a second lithography step is done to deposit the contact metals of Ti, Cu and Au onto the surface using e-beam evaporation.

Figure 1 shows an actual device upon which we did our measurements. Figure 2 demonstrates what was happening in the device during the measurement process. The incoming radio frequency current is indicated by I_{RF}. The colored arrows indicate two different torque vectors that were acting on the magnetic moment of the Py; the blue vector represents the torque associated with the Oersted field of the I_{RF}, and the red represents the torque associated with the spin transfer from the SHE. The result of these two torques was an oscillation of the magnetic moment of the Py.

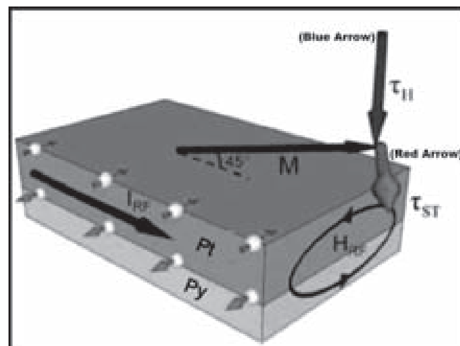

Figure 2: An illustration of what is happening in the device during the measurement process [1].

For the ferromagnetic resonance (FMR) measurement set up of our device, a signal generator created a radio frequency voltage across the spin Hall metal. The output was a DC voltage that gave the resonance signal.

We exposed the sample to a scanning magnetic field. A resonance peak was then induced at a certain magnetic field, which was read via the DC voltage signal out, as shown in Figure 3. This process was performed for only three out of four of the different device thicknesses, as the 7 nm sample returned high resistivity readings and very noisy resonance data. This could have been due to any number of errors in the fabrication process, including particulates or resist residue being on the sample before depositing contacts.

The curve was fit to an equation (3) from Liu, et al. [2].

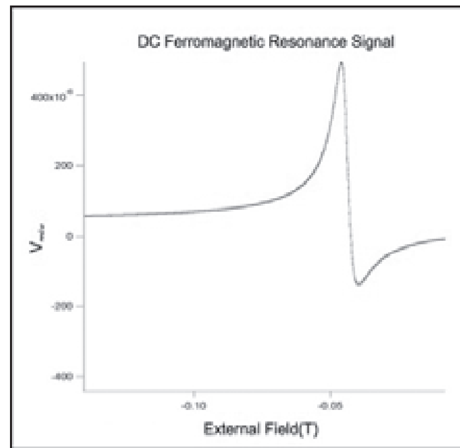

Figure 3: Represents the resonance curve, fit to an equation from Liu, et al. [2].

Results and Conclusions:

We calculated the spin Hall angle for each device fabricated by decomposing the resonance signal we found from ferromagnetic resonance measurements. Using non-linear graph fitting with the aforementioned equation, we split the resonance signal into its asymmetric component, which represented Spin Transfer, and its anti-symmetric component, which represented the Oersted field from the current. We then took the ratio of these two separate signals to find the spin Hall angle of each device for different thicknesses. Figure 4 represents the correlated data that we found.

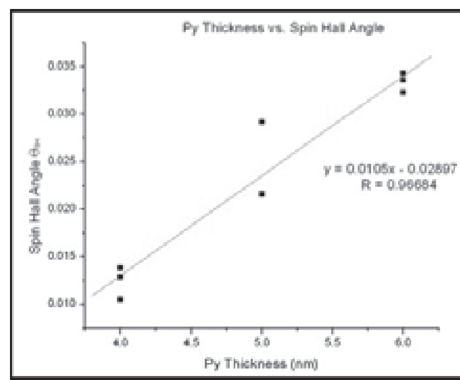

Figure 4: The correlated data after fitting and spin Hall angle calculations.

Ultimately a positive correlation between spin Hall angle and ferromagnetic layer thickness was found, as shown in Figure 4. There were a couple of issues with the data collected however. The first problem was that the spin Hall angle found for every device was much lower than expected, with the highest value recorded at 0.034, whereas previous spin Hall measurements have shown a spin Hall angle for platinum as large as 0.07 [2]. This was likely due to the fact the demagnetization constant Meff was not measured for each device.

It is believed that this correction could eliminate the positive correlation in the data and return no change in the spin Hall angle for varying thickness. Further measurements are necessary to determine these values.

Future Work:

If this positive correlation between ferromagnetic thickness and the spin Hall angle remains correct after parameter corrections, it will likely motivate further investigation into thickness dependence of the spin Hall angle.

Acknowledgments:

My thanks goes to the National Science Foundation, the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, the Cornell NanoScale Science and Technology Facility, my PI Dan Ralph, my mentors Wan Li and Eugenia Wan, and my CNF REU Program Coordinator Melanie-Claire Mallison for making this research possible.

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Self Assembled Monolayers on Inkjet-Printed ITO

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Abstract and Introduction:

Ink-jet printing allows for cost efficient roll-to-roll manufacture of thin-film transistors (TFTs) over large areas, enabling next-generation transparent displays, touch panels, opto-electronics, and radio frequency identification [1-4].

TFT conductance and cutoff frequency scale inversely with gate length. However sub-micron gate lengths are incompatible with traditional printing techniques, which have ~ 20 μm resolution [5]. New methods have been investigated to make sub-micron gate length organic TFTs without advanced photolithography [4].

Here, we expanded that approach to treat inkjet-printed indium tin oxide (ITO) electrodes with hydrophobic octadecyltrichlorosilane (OTS) self-assembled monolayers (SAMs) to repel away a second printed ITO electrode, yielding sub-micron electrode gaps. By combining this process with a solution-processed semiconductor, a cost-effective short channel TFT can be made. In this project, we refined inkjet printing of ITO nanoparticle ink to obtain uniform printed ITO patterns, which erre annealed to minimize sheet resistance. We used OTS to selectively manipulate the wettability of printed ITO versus various substrates. The effect of SAMs was quantified by contact angle measurements.

Preliminary experiments show that it may be possible to use this process to fabricate narrow gaps between ITO electrodes.

Experimental Procedure:

A carbon-water ink was used to optimize printing parameters on a DMP-2800 Series Dimatix Inkjet printer (Fujifilm, Santa Clara, CA). An aqueous ITO nanoparticle (NP) dispersion with 18% wt ITO (In_2O_3 and SnO_2) and an average particle size of 18 nm (US Research Nanomaterials, Houston, TX) was printed on sodalime glass, SiO_2, Si_3N_4, and Parylene-C substrates. To optimize printed ITO resistance, 2 mm × 0.1 mm one-layer printed ITO patterns on glass were rapid thermal annealed (RTA) on a JetFirst 150 RTP for four minutes at temperatures of 400-600°C in O_2, N_2, or N_2:O_2 4:1. Resistance measurements were performed using applied voltages from -5V to 5V.

Selected samples were treated with a 0.2% OTS/toluene solution for 20-25 minutes followed by sequential rinsing in toluene, acetone and isopropanol. Measurements of advancing contact angle were made with a VCA Optima series contact angle instrument (AST Products, Inc., Billerica, MA).

Results and Discussion:

The printing waveform was optimized to obtain uniform ITO lines with 150 nm thickness per printed layer by tuning

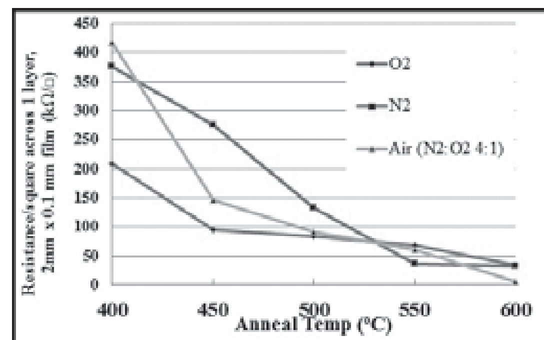

Figure 1: Printed ITO sheet resistance vs. temperature of 4-min RTA in various ambient environments.

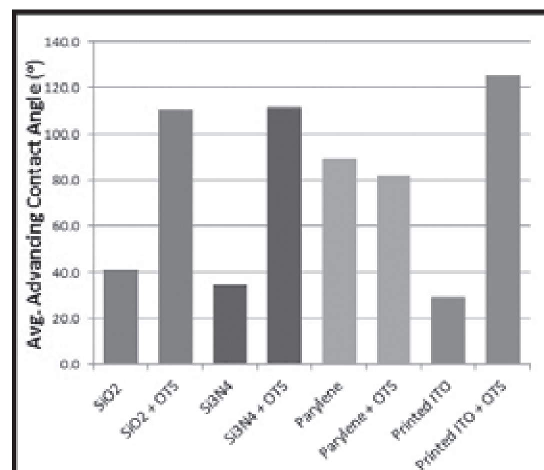

Figure 2: Contact angle of water on ITO and other substrates before and after OTS-SAM treatment.

the following parameters: firing voltages of 16-25V, firing frequency of 1-2 kHz, drop spacing of 18-20 μm and printing height of 0.5-0.75 mm. Post-printing RTA was optimized to minimize ITO resistance: four minutes at 600°C in 4:1 N_2:O_2 (air) yielded the lowest average sheet resistance of 6.1 kΩ/☐ for one-layer printed patterns (Figure 1).

Advancing contact angles of water on various substrates with and without OTS treatment were measured (Figure 2). For SiO_2 and ITO samples, contact angle increased upon OTS treatment due to OTS reaction with surface hydroxyl groups. ITO's change from relatively hydrophilic (52.77°) to notably hydrophobic (106.26°), indicates that OTS forms a SAM on ITO. The contact angle changed least for Parylene-C (88.9° before and 81.73° after OTS treatment), due its lack of a hydroxyl-terminated surface.

Selective wetting was observed between dropcast ITO and parylene after OTS treatment: the parylene could still be wetted, while the ITO film was so hydrophobic that water droplets would not leave a dispensing syringe when in contact with the ITO (Figure 3). In contrast to parylene, OTS-treatment of nitride increased its hydrophobicity, but it still remained more hydrophilic than OTS-treated ITO. Therefore, selective wetting similar to that on parylene was observed on OTS-coated ITO on nitride.

To explore the ability of OTS to define small gaps between ITO electrodes, we printed ITO patterns onto nitride substrates, annealed at 600°C for 4 min in 4:1 N_2:O_2, treated with OTS, and dropcast ITO ink. In some areas, dropcast ITO preferred nitride surfaces, however other ITO drops overlapped with OTS-treated printed ITO (Figure 4).

It is likely that the ITO drops were too large in volume to allow for very small-scale hydrophobic interactions to dominate. More investigation is needed to refine the selective wetting process.

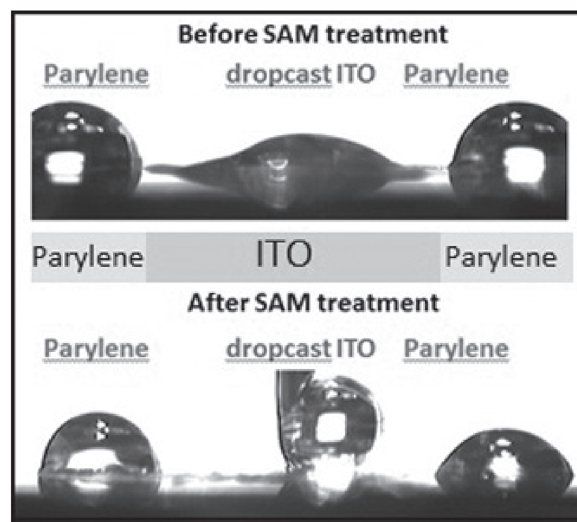

Figure 3: Water wetting on dropcast ITO and parylene before and after OTS-SAM treatment.

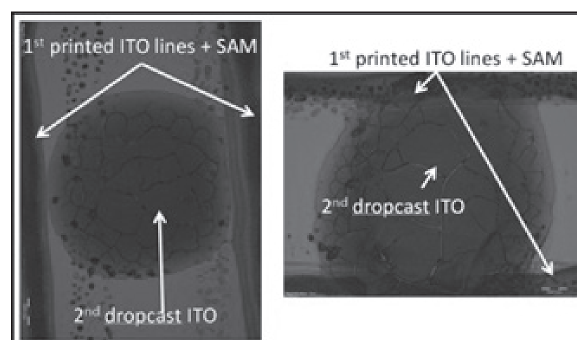

Figure 4: Different samples showing repelling (left) and overlap (right) of ITO dropcast on printed, annealed and OTS-treated ITO patterns.

Conclusions:

Inkjet printing and annealing of aqueous ITO NP inks was refined to obtain neatly patterned ITO films of thickness ~ 150 nm/layer, with minimum sheet resistance of 6.1 kΩ/☐. Contact angle measurements before and after OTS-SAM treatment show greater increase in hydrophobicity of printed ITO lines compared to substrates such as parylene and silicon nitride. We use this effect to achieve selective de-wetting of secondary ITO ink drops off previously printed ITO lines onto parylene or nitride surfaces. Preliminary results indicate that it may be possible to use such selective wetting processes to achieve sub-micron scale ITO electrode gaps, for high-performance thin film transistors fabricated by inkjet printing.

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Fabication of GaAs-Based Integrated Circuits by Advanced Nanofabrication Techniques

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Abstract:

Gallium arsenide (GaAs), a III-V semiconductor, has recently gained attention due to promising applications in wireless technologies that include power amplifiers and integration of switches for use of different frequency bands. The relatively high electron mobility, lower high frequency noise, and lower parasitic capacitances of GaAs in comparison to silicon make GaAs a suitable choice for high frequency integrated circuits.

This project focused on the creation of three GaAs integrated circuit (GaAs-IC) devices — specifically the: 1) Metal-semiconductor field effect transistor (MESFET), 2) Logic Inverter, and 3) Ring Oscillator — with each subsequent device employing the previous device as a base component. The Schottky barrier intrinsic to the MESFET made it difficult to achieve the necessary positive threshold voltage for creating a functional ring oscillator. Using industrial level design, fabrication, characterization, and analysis techniques, all three devices were ultimately created and the functional ring oscillator achieved an operating frequency of 19.9 MHz — a value comparable to predicted values.

Approach:

One cycle of the project involved the computer automated design of a new sample (including several devices), followed by fabrication in a cleanroom environment. The devices were then characterized using the manual prober system. Data was analyzed using MATLAB.

Methods:

Preparation of GaAs Substrate. The GaAs substrate used; 1) an n-type GaAs active layer ($N_D = 3 \times 10^{16}$) with an initial thickness of 500 nm on, 2) a semi-insulating GaAs. The GaAs wafer was first cut to the appropriate size. Thinner active layers correspond to higher threshold voltages, so the sample was then etched with $H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 50$ to achieve a depth ranging from 100 nm to 500 nm.

Mesa Fabrication. The sample was coated with primer (HMDS), then photoresist (AZP4620 : PGMEA = 3 : 1). Samples were exposed to the Mesa pattern using the DL-1000 laser lithography system and hand developed in 2.38% tetramethylammonium hydroxide (TMAH). A postbake at 140°C prepared the sample for a second etching process that electrically isolated the samples. The photoresist was removed with N-methyl-2-pyrrolidone (NMP).

Source and Drain Electrode Fabrication. The sample was coated with primer (HMDS), then two photoresists (PGMI and TSMR8800). Samples were then exposed and developed. Au-Ge/Ni/Au = 1500A/100A/1500A was deposited by the R-DEC e-gun evaporation system. The resist and excess metal was lifted off with NMP. The sample was then annealed at 400°C to prepare the sample for a second etching process that electrically isolated the samples. The photoresist was removed with N-methyl-2-pyrrolidone (NMP).

Gate Electrode Fabrication. The sample was coated with primer (HMDS), then two photoresists (LOR5A and AZ5214E). Samples were then exposed and developed. Ti/Au = 2000A/2000A was deposited by the ULVAC jsputter sputtering system. The resist and excess metal was lifted off with NMP.

A completed ring oscillator device is shown in Figure 1.

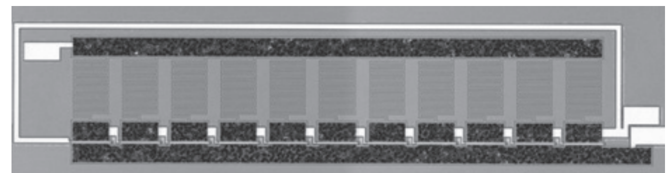

Figure 1: Completed ring oscillator device.

Results:

Positive Gate Threshold Voltage Achieved Through T-Gate Design. An active layer thickness of below 174 nm is needed to achieve a positive threshold voltage. However, functional devices with this thickness are difficult to create due to increased defects at the interface of the active layer and semi-insulating GaAs; effective mobility is determined to drop significantly as active layer thickness is decreased. Initial MESFET fabrication resulted in a maximum threshold

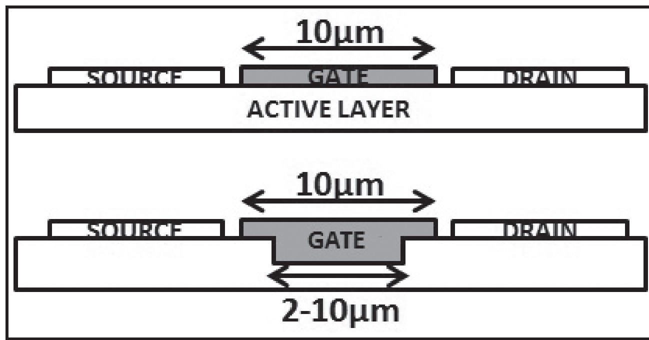

Figure 2: Schematic of T-gate (bottom) with original gate for reference (top).

voltage of -0.22V determined from drain current as a function of gate voltage data measured using a manual prober system for each device.

The T-gate design (Figure 2) involved using the gate width of 10 µm employed in earlier designs while etching a portion of the active layer ranging in width from 2 µm to 10 µm centered below the gate metal. By etching the active layer at only this area to 141.3 nm and 172.4 nm, positive threshold voltages of 0.15V and 0.3V were achieved, respectively (Figure 3). The most successful T-gate variation had a 2 µm base width.

MESFET and Inverter Performance. Devices across MESFET and inverter samples were found to be consistent. Strong gate dependences were observed and inverter devices exhibited sensitive input and full-scale output.

Ring Oscillator Performance. Functional ring oscillators were fabricated using the T-gate design on the 174.2 nm active layer sample. Oscillation frequencies of 19.9 MHz were observed for load resistances of 3.2 kΩ and 1.7 kΩ corresponding to applied voltages of 1.3V and 0.9V, respectively.

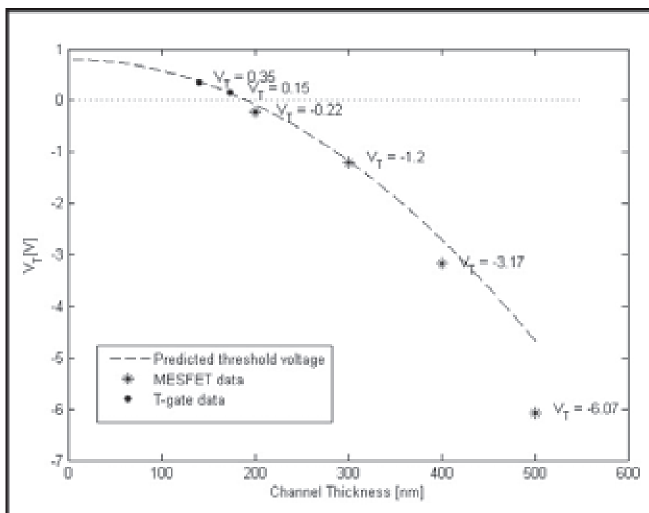

Figure 3: Average threshold voltage as a function of active layer thickness. Values for thicknesses over 200 nm correspond to MESFET data while values for thicknesses below 200 nm correspond to T-gate data.

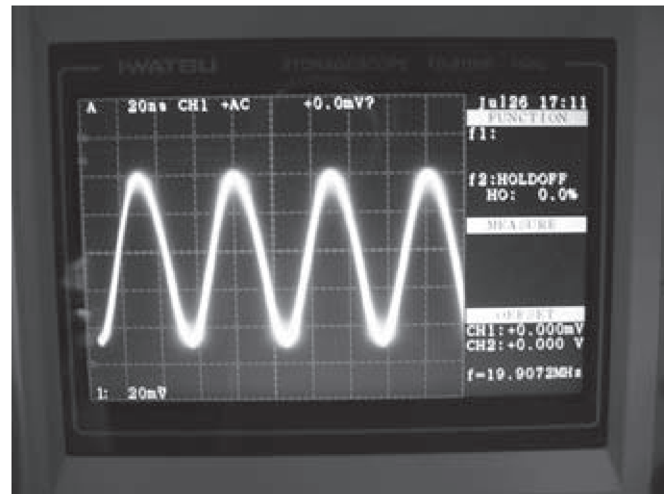

Figure 4: Functional ring oscillator output for R = 3.2 kΩ and V_{DD} = 1.3V.

Conclusions and Future Work:

The importance of achieving a positive threshold voltage was realized during early iterations. The resulting design and fabrication of the T-gate overcame the decrease in effective mobility for thinner active layers and contributed to the successful fabrication of all three target devices. The ring oscillator output oscillation frequencies of 19.9 MHz were comparable to calculated values.

However, the ring oscillator design can be improved in future iterations. A T-gate base width below 2 µm may increase effective mobility and produce stronger inverting characteristics at lower load resistances, producing higher oscillation frequencies. In addition, it has been observed that full sized 200 µm by 200 µm source/drain electrodes have a higher effective mobility and corresponding drain current than the compacted 100 µm by 200 µm electrodes used for later samples. Use of full sized versions in future designs may yield similar performance improvements.

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