The Effects of Surface Passivation on Trap Levels in Silicon Nanocrystals

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Introduction:

Silicon nanocrystals (Si-NC) systems have a wide variety of applications due to their optical properties, and their growth can be easily incorporated into Si fabrication methods already established in industry, making Si-NCs an attractive alternative to bulk Si. Recent developments have allowed for the synthesis of Si-NCs that are resistant to oxidation through surface passivation [1]. However, the effects of surface passivation on the electronic properties of Si-NCs remain unknown. With this in mind, our research focused on the investigation of trap levels in Si-NCs and the effects of passivation on these traps.

Experimental Details:

The Si-NCs were created using non-thermal plasma synthesis with both SiH_4 and SF_6 gas in order to produce H and F terminated Si-NCs. Details on Si-NCs and passivated Si-NCs growth are described by Pi, et al. [2], and Liptak, et al. [1], respectively. Metal-oxide-semiconductor (MOS) capacitors were fabricated by annealing RTA cleaned n-type Si <100> in a O_2 ambient in order to create a thin SiO_2 interface, followed by the deposition of Si-NCs on the SiO_2 layer.

In order to optimize our measurements, we then utilized atomic layer depostion (ALD) to deposit a high-κ dielectric (HfO_2) layer on top of the Si-NCs, and finished by evaporating aluminum back and gate contacts. We fabricated devices with no Si-NCs (for control), a 30-second deposition Si-NCs layer, and a one-minute deposition Si-NCs layer for both bare Si-NCs and surface passivated Si-NCs samples. A topological overview of the device structure can be seen in Figure 1.

The trap centers of our fabricated MOS structures were then investigated using capacitance-voltage (C-V) profiling and deep level transient spectroscopy (DLTS) in order to confirm the presence of traps as well as to characterize the energy level and trap cross-section of these trap centers. The C-V profiles were acquired at different frequencies of 200, 50, and 10 kHz and the DLTS data was acquired using a temperature range of 35K-420K and a rate window of approximately 16 s^{-1}.

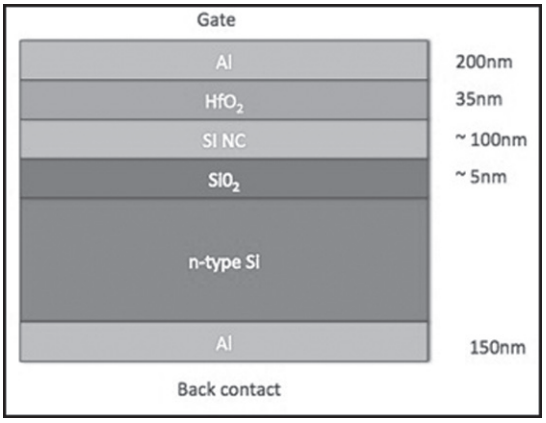

Figure 1: Cross-sectional side view of the fabricated MOS-capacitors with embedded Si-NCs. The approximate thickness of each layer is shown at the right of the corresponding layer.

Results:

The C-V profiles of the samples (not shown), suggest the presence of trap levels in a number of ways: (1) The decrease in accumulation in both the bare and passivated Si-NCs samples indicated the presence of majority traps; (2) Stretchout indicated a greater number of trap levels in the bare and passivated Si-NCs samples; (3) The decrease in depletion in both the bare and passivated Si-NCs samples suggested a higher concentration of interface and majority trap levels; and (4) A greater change in the depletion capacitance was observed for the bare and passivated Si-NCs samples than for the control sample, indicating an increase in interface state density. It is also worth noting that the change in depletion capacitance was greater in the passivated samples.

The C-V measurements also demonstrated hysteresis in all samples for all profiling frequencies, as can be seen in Figure 2. The negative shift of approximately 0.5 V in the down trace of all the measurements is consistent with previously observed values by Kwon, et al., and this memory effect confirms the presence of Si-NCs in the samples [3].

The DLTS measurements are shown in Figure 3 and the trap levels found are summarized in Table 1. These results show that the trap levels found in

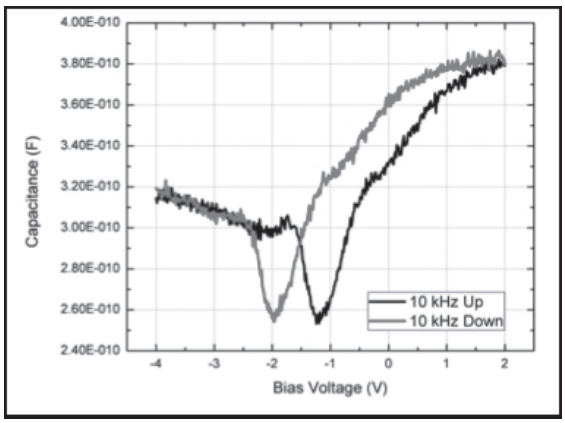

Figure 2, above left: C-V profile shows the hysteresis profile for a 10 kHz scan of the passivated sample.

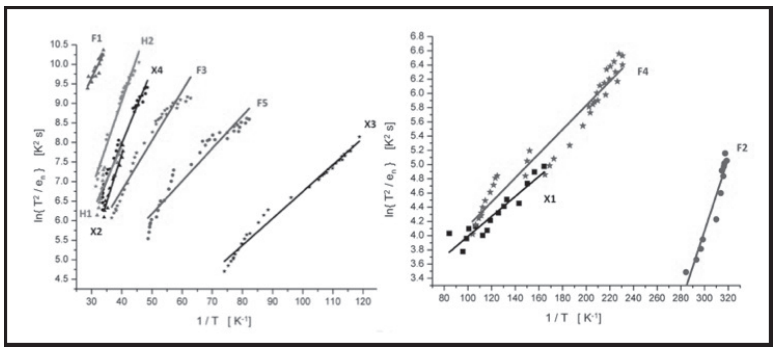

Figure 3, above right: Arrhenius plots of our DLTS measurements show the presence of multiple traps levels. Each trap is labeled and more information can be found in Table 1.

Table 1, at right: List of the corresponding activation energy, capture cross-sections and temperature peaks for the trap levels found.

Control			
Trap	E (ev)	σ (cm²)	Peak (K)
X1	0.01	$4.1x10^{-21}$	60
X2	0.39	$7.4x10^{-18}$	270
X3	0.07	$3.5x10^{-22}$	100
X4	0.19	$4.5x10^{-22}$	270

Bare Si-NCs			
Trap	E (ev)	σ (cm²)	Peak (K)
H1	-0.53	$1.7x10^{-17}$	270
H2	0.22	$4.4x10^{-22}$	290

Passivated Si-NCs			
Trap	E (ev)	σ (cm²)	Peak (K)
F1	-0.16	$4.0x10^{-20}$	350
F2	0.05	$2.1x10^{-17}$	40
F3	0.13	$1.6x10^{-21}$	230
F4	0.02	$3.5x10^{-22}$	60
F5	-0.08	$2.3x10^{-21}$	170

our bare Si-NCs samples are not consistent with previously reported values by Souifi, et al. [4] and Kwon, et al. [3], which can be attributed to different Si-NCs growing methods. The traps found also have capture cross-section orders of magnitude smaller than expected, which has been previously observed and attributed to charge tunneling into the Si-NCs and a lower density of states at the Si-NCs by Antonova, et al. [5].

Overall, surface passivation appears to remove deep level traps in Si-NCs while creating shallow level traps for both majority and minority carriers. Considering than an F-terminated Si surface oxidizes much faster than an H-terminated Si surface [6], the removal of deep level traps in Si-NCs by surface passivation supports proposed theories that deep level traps in Si-NCs are caused by hydrogen dangling bonds [7]. However, not enough data has been collected to make any serious assessment and further research is needed to; (1) confirm the validity of the observed trap levels, and (2) correlate growth parameters with observed trap levels.

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