Integration of Embedded CMOS Chips for On-Chip Optical Communication

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Abstract and Introduction:

The rapid development of telecommunications infrastructure in developing nations, the advent of high-speed cellular data networks and the recent popularization of cloud computing continue to drive demand for more robust and energy efficient data networks. The dominant source of power utilization in these networks is the electrical interconnect due to the high energy cost of moving data between the computing and communication blocks. Losses inherent in electrical interconnections between computing and telecommunications infrastructure may be mitigated by utilizing optical interconnects instead.

In recent decades, many electronic-photonic integration techniques have been explored, however, a process that is truly compatible with complementary metal-oxide-semiconductor (CMOS) technology has yet to be developed.

In this work, a novel integration technique that circumvents most of the difficulties faced by existing methods is presented. It allows for the integration of CMOS dies into silicon photonic substrates. The process is based on the creation of a chip-specific imprinted hard mask utilizing localized polymerization of a heat-curable poly(dimethylsiloxane) (PDMS) elastomer, which allows for the embedment of multiple dies into a single mask. Localized polymerization around individual dies is performed by the independent temperature control of the arm and stage of a flip-chip bonder. The masked substrate is then subjected to a series of reactive ion etching steps in order to create chip-specific cavities with length and width dimensional tolerances of less than 10 μm, enabling close integration of the CMOS die and photonics substrate.

Experimental Procedure:

In order to examine potential changes in the electrical characteristics of integrated dies, dies patterned with series and parallel RLC oscillator circuit designs were created via traditional contact photolithography, metallization, lift-off, and dicing techniques. Each die measured 1.5 mm long by 1.5 mm wide.

The procedure for the integration technique executed was as follows:

A passive silicon photonics substrate (optical substrate) containing silicon waveguides cladded by layers of silicon dioxide (SiO_2) was bonded to a Si carrier substrate using photoresist as an adhesive. Dow Corning Sylgard® 184 PDMS elastomer was mixed in a 6:1 base-to-curing agent weight ratio and spin-coated onto the optical substrate. The optical substrate was then placed onto the stage of a flip-chip bonder, which was kept cool to prevent polymerization of the entire surface coating. A die was picked up by the arm and tip of the flip-chip bonder, properly positioned over the optical substrate, and pressed into the prepolymer. Heating of the die by the arm initiated polymerization in the area immediately surrounding the die. Following the heating period, the arm was allowed to cool. Prior to liftoff of the arm, air was discharged through the tip for 800 μs to aid in the release of the die. Detailed flip-chip bonder temperature and applied force parameters are shown in Figure 1.

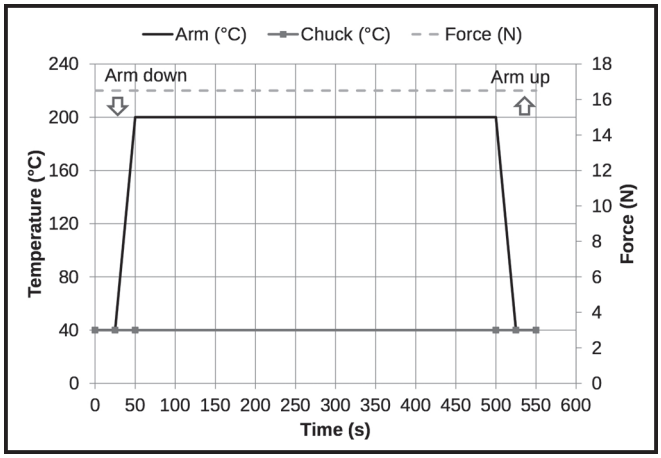

Figure 1: Flip-chip bonder temperature and applied force profile.

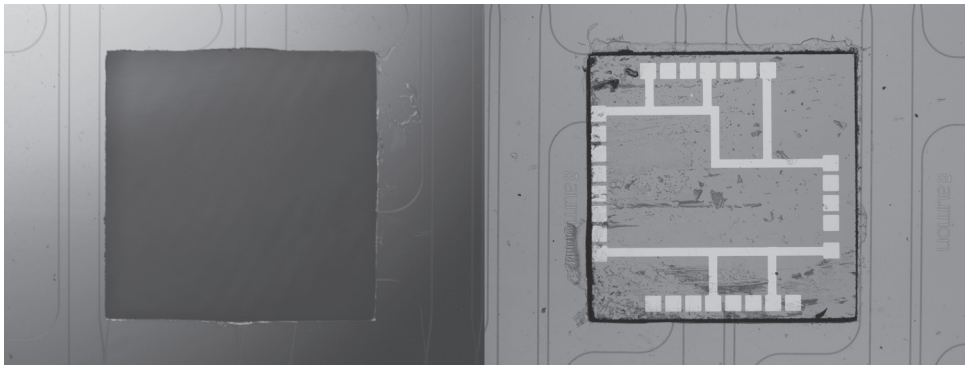

Figure 2: Vacant through-substrate cavity (left) and integrated RLC circuit die (right).

Following die embedment, the optical substrate was baked at 110°C for 10 minutes to cure the entirety of the elastomer mix atop the substrate. Afterwards, the die was removed from the mask, and residual PDMS that remained underneath it was removed via reactive ion etching (RIE). Inductively coupled plasma (ICP) RIE was used to remove the waveguide cladding layers. Bosch process deep RIE was employed to etch through the silicon waveguide core and the optical substrate base. The bulk of the remaining PDMS hard mask was removed manually, and the optical substrate was freed from the carrier. Residual PDMS was removed via reaction with tetra-n-butylammonium fluoride in a solution prepared as described by Balakrisnan, et al. [1].

The optical substrate was bonded upside down to a carrier substrate, and the die was fitted into the etched cavity. Backside planarization and filling of the gaps between the integrated die and the cavity walls was accomplished by spin-coating Filmtronics Incorporated 500F spin-on glass (SOG) onto the backside of the optical substrate. The SOG was soft-baked sequentially at 95°C, 175°C, and 200°C for two minutes per temperature. A total of three layers of SOG were applied in this manner.

Results and Conclusions:

Two optical substrates are shown in Figure 2. For a sense of scale, the die measures approximately 1550 μm by 1550 μm. The largest die-to-wall gap is approximately 15 μm wide, significantly larger than the smallest gap achieved in other samples created via the employed integration technique and similar methods [2]. This discrepancy is likely the result of distortion of the mask upon removal of the die prior to the etching procedure, and can be easily minimized with increased caution during die removal.

Future Work:

Planarization of the upper surface of the optical substrate could not to be carried out due to time constraints. However, this can be achieved by plasma-enhanced chemical vapor deposition of a layer of SiO_2, which can then be polished flat via chemical mechanical polishing. Traditional photolithographic and ICP RIE processes can then be employed to pattern and etch through the upper SiO_2 layer to uncover metal contacts atop integrated dies and the optical substrate. Standard metallization and lift-off techniques can then be used to deposit a top metallization layer to establish electrical connections between integrated CMOS dies and optoelectronic devices, thus enabling the creation of electronic-photonic integrated circuits.

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References:

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[2] Uddin, A., et al. IEEE Transactions on Components, Packaging, and Manufacturing Technology; Vol. 1, No. 12; 1996-2004 (2011).