Fabricating Parylene-C Shadow Masks for Applications in Short-Channel Top-Contact Carbon Nanotube Flexible Transistors

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Abstract:

Flexible transistors with semiconducting carbon nanotubes offer better mobility and stability than current organic material transistors for applications in flexible display and sensor devices. With carbon nanotubes as the semiconducting material, the transistors offer a higher performance due to the extraordinary electrical properties of single-walled carbon nanotubes (SWNTs). However, conventional metal shadow masks can only create flexible device transistors with a channel length of 50 μm or greater. Parylene-C shadow masks can be used instead of metal masks because of their flexibility, adaptability for patterning, and their ability to fabricate transistors with much smaller channel lengths. Previously it has been shown that Parylene-C masks allow for a fine resolution with a smallest feature size of 4 μm. We fabricated masks with features as small as 2 μm wide, and additionally used our masks to create short-channel transistors. We successfully constructed short-channel top-contact SWNT network inflexible and flexible transistors on silicon (Si) and polyamide substrates with a mobility of 0.1 to 2 cm^2/V-s and on/off ratios on the magnitude of 10^2 to 10^3.

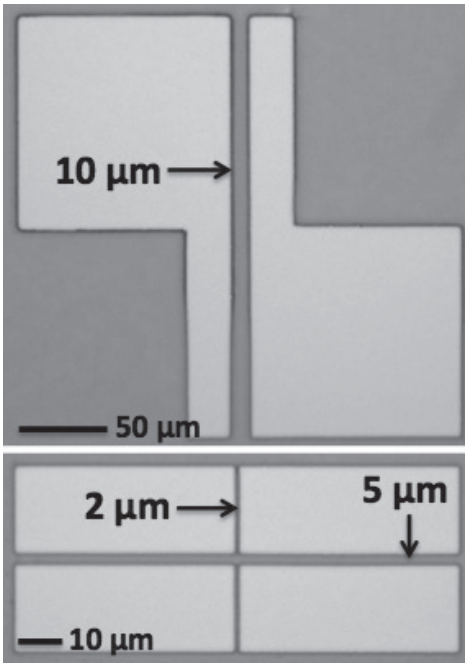

Figure 1: 2, 5, and 10 µm features etched into parylene on Si substrate.

Introduction:

Parylene-C is a polymer that is flexible, transparent, biocompatible, and relatively inexpensive. Its characteristics allow for Parylene-C shadow masks to have the potential for various micropatterning applications [1]. Unlike conventional hard masks, parylene masks adhere to the surface of the substrate for better contact between the substrate and the stencil. While conventional hard masks can create features as small as 50 μm wide, parylene masks have been used to make features as small as 4 μm wide. Previously, flexible transistors have been fabricated with semiconducting carbon nanotube networks [2]. Short-channel inflexible transistors have also been fabricated, using Parylene-C shadow masks [3]. To optimize the performance of our flexible transistors, we combined features of both previously fabricated devices. We aimed to make Parylene-C shadow masks for use in the fabrication of short-channel flexible transistors with solution-sorted semiconducting carbon nanotube networks.

Experimental Procedure:

To fabricate the parylene masks, we adopted a previously developed procedure to fit the capabilities of the Stanford Nanofabrication Facility and Bao lab equipment [1]. We exposed 4-inch silicon wafers coated with 15 μm of parylene to oxygen plasma at 150 W RF power and at 150 mTorr to roughen the parylene to enhance aluminum adhesion. Then we evaporated 200 nm of aluminum onto the parylene and created a hard mask through conventional optical lithography. We patterned the aluminum through a wet etch (72% phosphoric acid, 3% nitric acid, 3% acetic acid, 22% water). Then we etched the parylene with oxygen plasma for one hour at the same parameters previously used to roughen the parylene, and finally, we etched away the aluminum hard mask with the same wet etchant (Figure 1).

To fabricate transistors with the parylene mask, we prepared substrate samples by soaking them in purified semiconducting SWNT solutions. To purify semiconducting SWNTs from metallic SWNTs, we used the Bao group's previously developed sorting process [4]. We peeled the mask off of the silicon wafer and placed it on the new substrate with carbon nanotubes, and then evaporated 40 nm of gold over the mask to fabricate the transistors (Figure 2 and 3).

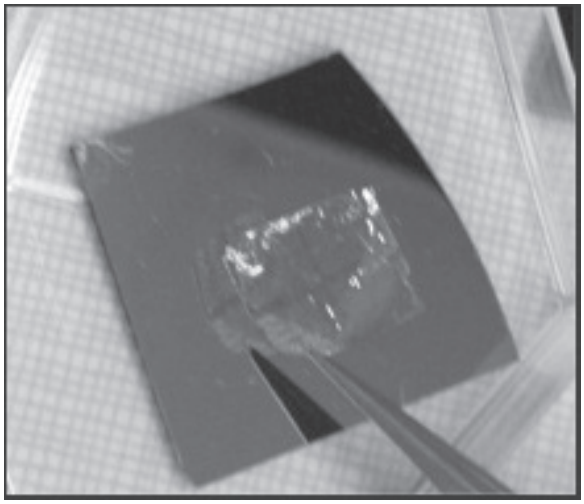

Figure 2: Parylene mask peeled off of Si substrate.

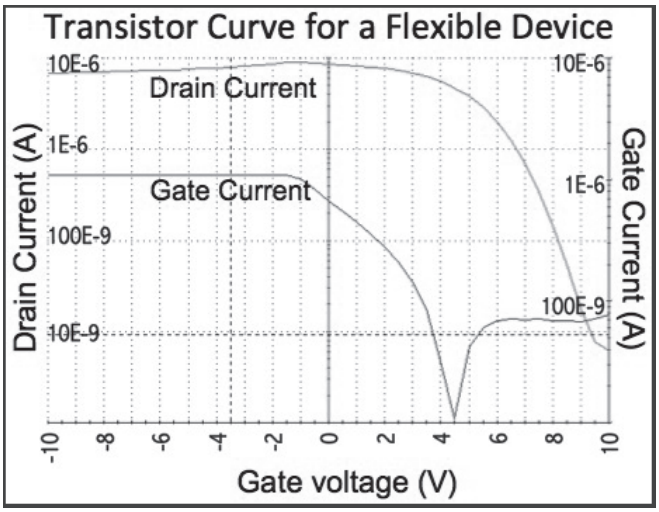

Figure 4: Keithley-generated flexible transistor curve.

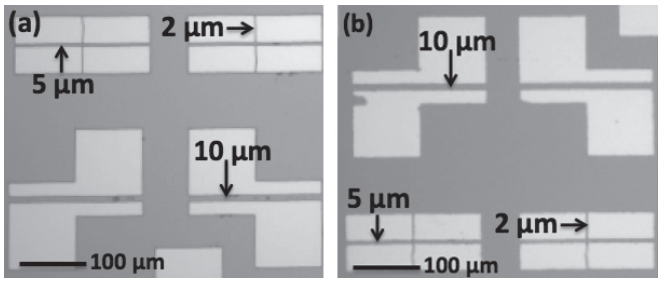

Figure 3: (a) Parylene mask placed onto SWNT-soaked substrate; (b) Gold on SWNT-soaked substrate after mask removal.

After the gold evaporation, we peeled the mask off and tested the transistors for their performance.

Results and Discussion:

We consistently fabricated Parylene-C shadow masks with etched features ranging from 2 μm to 50 μm wide. The process was optimized and scaled-up to full wafer scale production of shadow masks. We fabricated inflexible and flexible transistors with the parylene masks and then tested the performance by measuring the current flow across transistors at various applied gate voltages. Both types of devices had a mobility of 0.1 to 2 cm^2/V-s and on/off ratios on the magnitude of 10^2 to 10^3 for channel widths of 20 μm (Figure 4).

Although we fabricated transistors as small as 2 μm wide, it was difficult to test these transistors with the equipment we had. Therefore we only tested features 5, 10, 20 and 30 μm wide. From testing the inflexible and flexible transistors, the data indicated that we had fabricated functioning devices with good on/off ratios and mobilities. Furthermore, the parylene masks allowed for consistent transistor fabrication within a sample and between samples as well. The on/off ratios and mobility results for flexible transistors were similar to that of inflexible transistors, indicating that the flexible substrate did not hinder the performance of the device.

Future Work:

We aim to continue fabricating short-channel top-contact carbon nanotube flexible transistors to optimize their performance. Furthermore, bending tests will be conducted on the flexible transistors to assess their performance during and after strain. We also aim to optimize the purification process of the semiconducting carbon nanotubes using various solvents and polymers.

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