Influence of Optical Stress on Mixed Oxide Transistors

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Abstract:

To meet the growing demands of thinner and larger display panels, an improved and reliable semiconducting channel material must be used. Indium-gallium-zinc oxide (IGZO)-based thin-film transistors (TFTs) have presented themselves as a viable option to achieve better carrier mobility, optical transparency and robustness under optical stress conditions. However, the instability of IGZO TFTs remains a problem that must be resolved. In particular, there is deterioration in the threshold voltage (V_{th}) during continued operation because of continuous optical stress. In this investigation, we performed illumination stress on TFTs in an attempt to elucidate the root cause of the V_{th} shift, and several post fabrication anneals to reduce defects due to low temperature fabrication process. The as-fabricated TFTs displayed a V_{th} shift of -17 V under optical stress, but demonstrated high stability with post-fabrication anneals in different ambients.

Introduction:

As the ability to scale the dimensions of transistors down to nanometers has improved, the computing powers relative to the sizes of the devices have increased substantially. Thus, consumers have come to expect a level of sophistication and proficiency in everyday electronics that seemed unattainable until a decade ago. From high-resolution smartphones to liquid crystal and light emitting diode displays, the vast majority of electronic devices all rely on circuitry that is implemented in silicon. Although it is the most effective technology available, single-crystal silicon lacks optical transparency and flexibility. In addition, single-crystal silicon-based fabrication is expensive and unobtainable for large area electronics. Amorphous oxide semiconductors (e.g., IGZO) present a potential solution for applications that require transparency or flexibility.

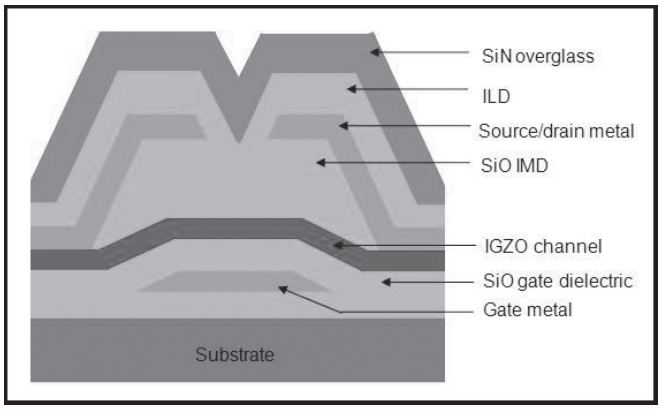

Figure 1: The structure of an IGZO TFT.

Experimental Procedure:

The structure of the IGZO TFT is shown in Figure 1. The gate metal was 150 nm thick molybdenum deposited using DC sputtering. After patterning the gate layer, a stack of silicon oxide (SiO_x), IGZO, and SiO_x was deposited through a series of steps. A 200 nm silicon oxide formed the gate dielectric. The 50 nm thick channel material IGZO, with 99.99% pure $InGaZnO_4$, was deposited at an RF power of 100 W and a chamber pressure of 10 mTorr at 80°C, and a 100 nm intermetal dielectric SiO_x is deposited at 180°C. The IGZO was patterned and the source-drain metal (Mo) was sputtered to form the source and drain contacts of the TFT. A final step involved deposition of silicon nitride to serve as a passivation layer.

The IGZO TFT samples were annealed in one of four ambients (oxygen, vacuum, forming gas, and air) for 12 hours at 150°C to improve optical and electrical characteristics. Current-voltage characteristics were acquired using a HP 4155B semiconductor parameter analyzer. The TFTs were illumination-stressed for 25,000 seconds in a dark, light-tight setup, and the transfer characteristics were obtained by sweeping the gate voltage, with the drain biased at 10 V and the source grounded. To perform illumination testing, a Dolan Jenner Fiber Lite Illuminator with a light source of intensity 0.5 W/cm^2 and a dual gooseneck optical cable attachment was used. A 410 nm wavelength filter allowed violet light from the source to be used for the illumination tests, and was chosen due to previous reports on illumination stress testing [1] that revealed increasing amounts of photo-induced defects with decreasing wavelengths of light.

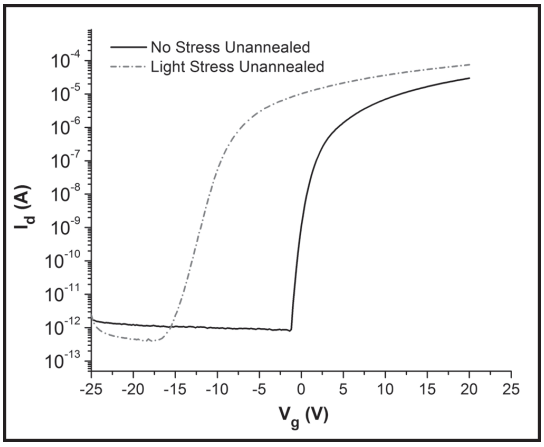

Figure 2: As-fabricated IGZO TFTs unannealed stressed under 410 nm light for seven hours.

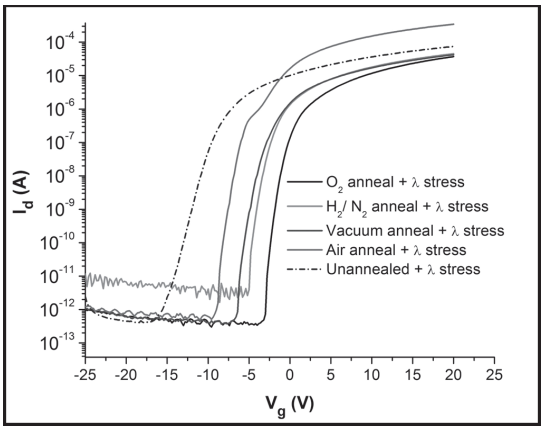

Figure 3: Illumination stress (λ = 410 nm for 7H) on post-fabrication annealed IGZO TFTs for 12 h at 150°C.

Results and Conclusions:

In Figure 2, during as-fabrication stress testing there was a considerable threshold voltage shift, making the turn-on voltage smaller, and leakage and off currents higher, along with a slight increase in mobility. The V_{th} change was -17 V during the seven hours of light stressing. In post-fabrication annealed testing, there was great improvement in the transistor performance seen as reduced V_{th} shift as Figure 3 demonstrates. In Figure 3, the oxygen-annealed sample showed the least deterioration with low off current and steep subthreshold swing. This can be explained by the annihilation of oxygen vacancies by annealing, which otherwise ionize

Air	Vacuum	Oxygen	Forming Gas	Unannealed
-3.6 V	-4.5 V	-1.3 V	-3.3 V	-17 V

Figure 4: V_{th} shift of unannealed along with air, vacuum, oxygen, and forming gas annealed IGZO TFTs under illumination stress.

to contribute as excess carriers due to photonic stresses [2]. Figure 4 displays the V_{th} shift of each sample after seven hours of light stress with respect to each device's own unstressed condition (e.g., ΔV_{th} for oxygen-annealed TFT is calculated by finding the difference between V_{th} after seven hours and V_{th} unstressed, but annealed in oxygen).

In conclusion, the results obtained emphasize the importance of post-fabrication annealing of IGZO TFTs whilst the as-fabricated TFT device was driven to near failure under stand-alone illumination stress. Annealing reduces the V_{th} shift due to annihilation of defects created during low temperature fabrication. The TFTs demonstrate highest stability after annealing in oxygen ambient due to annihilation of oxygen vacancies that contribute most towards excess carriers.

Future Work:

Future work will involve investigating the effects of electro-mechanical and mechanical strain on IGZO TFTs fabricated on flexible substrates. In addition, the findings of the current report will be presented at the TMS 2013 Conference.

Acknowledgements:

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References:

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