Temperature Dependent Electrical Resistivity of $La_xLu_{1-x}As$

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Abstract:

We report the temperature-dependent resistivity of lanthanum lutetium arsenide ($La_xLu_{1-x}As$) thin films grown by molecular beam epitaxy. Thicknesses of measured films were 30, 100 and 500 nm. Studies on the resistivity of $La_xLu_{1-x}As$ films suggest semimetallic behavior for temperatures ranging 78 to 295 K. Resistivity was measured using a cross sheet resistor van der Pauw (VDP) structure fabricated onto samples employing planar fabrication techniques. The linear fit of resistivity vs. temperature likely indicates electron-phonon scattering as the dominant mechanism, for temperatures from 78 to 295 K [1]. The increase in resistivity by increasing thickness was likely due to increasing interface roughness from imperfect growth at large thickness scales.

Introduction:

The discovery of graphene, a stable two-dimensional structure of carbon, has opened the door to the study of other thin films. Materials such as III/V and rare earth arsenides are suggested as “beyond graphene” materials. Investigation of electrical transport properties of rare-earth arsenides can lead towards a comprehensive understanding of carrier transport properties of these compounds and the development of novel electronic devices. To begin exploration of this, electrical properties of $La_xLu_{1-x}As$ (x = 47 and 48%) alloys were characterized as a function of thickness and temperature.

One of the most accurate methods for measuring sheet resistance of thin films is achievable by employing van der Pauw structures (Figure 1). The method is advantageous because it allows measurements to be taken of arbitrary lamellae by strategic placement of electrodes at the perimeter.

Experimental Procedure:

The sample stack was grown by molecular beam epitaxy (MBE). To account for impurities in the wafer left after heat treatment, 200 nm of gallium arsenide (GaAs) were grown onto a commercially available GaAs wafer. Ten monolayers (ML) of an LuAs spacer layer were grown next, followed by $La_xLu_{1-x}As$ and another 10 ML LuAs. The stack was capped

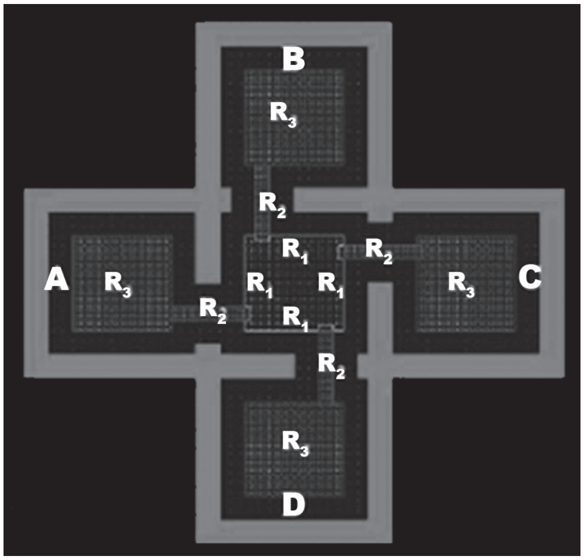

Figure 1: A van der Pauw structure where R_1 indicates resistance in the region of interest, R_2 the arm resistance, and R_3 the surface shunt resistance of the contact pad. Image courtesy S. Rahimi.

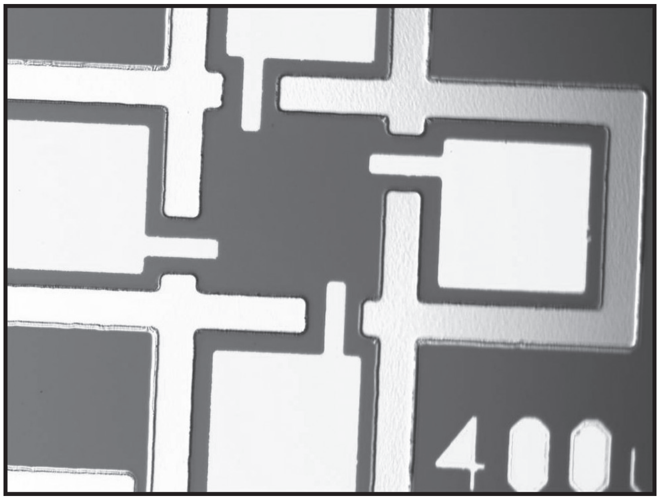

Figure 2: A fabricated VDP device.

by 15 nm GaAs to prevent oxidation of the alloy. Spacer layers separated LaLuAs from GaAs on both sides to prevent it from diffusing.

Fabrication of van der Pauw devices began by spin-coating cleaned samples with negative photoresist, AZ-5214. A Karl Süss MJB4 was used for lithography. Electrodes were deposited using electron beam evaporation (CHA SR-10 metal deposition tool), with a nickel adhesive layer and 41.1 nm gold. A lift-off process was required to form electrodes.

Following the second layer mask's lithography, devices were isolated by mesa-etching in a 1:1:20 solution of H_3PO_4:H_2O_2:H_2O. A fabricated device can be seen in Figure 2.

Low temperature measurements were taken using a Lakeshore cryogenic four probe system. The van der Pauw method was used [2, 3], requiring measurements be taken in two positions (see Figure 1). In the 0° degree position, current was run from pad A to B, and the voltage drop was measured between C and D. In the 90° position, current was run between pads D and A, and the voltage drop was measured between B and C. For both positions, measurements were first taken with a forward current (+I) and then with the reverse (-I). Using these four values, R_{00}' was calculated, according to the equation below. Similarly, R_{90}' was calculated.

$$R_{00}' = \frac{V_{CD}(+I) - V_{CD}(-I)}{I_{AB} - I_{BA}}$$

From the average of the two, sheet resistance was found from the VDP formula, below.

$$R_S = \frac{\pi}{\ln 2} R_{AVE} * f$$

A correctional factor, *f*, was used to correct for asymmetry in the structure. For this data, the correctional factor was 1.00, indicating high symmetry of devices.

Resistivity was calculated by multiplying the sheet resistance by thickness.

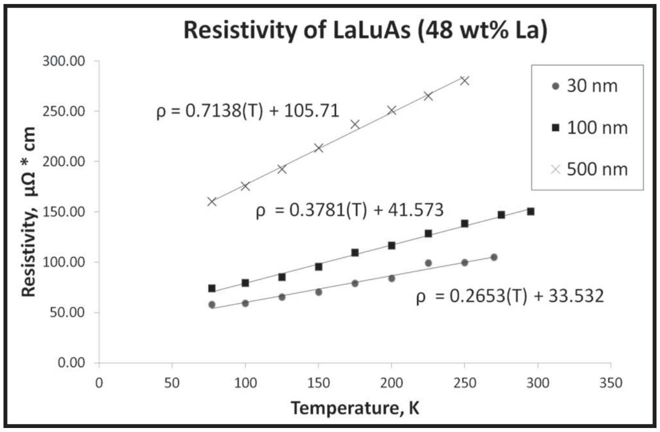

Figure 3: An analysis of data reveals increasing thickness corresponding with increasing resistivity.

The alloys exhibited semi-metallic behavior, increasing in resistivity with increasing temperature (Figure 3). The plots of resistivity vs. temperature and sheet resistance vs. temperature were linear. For this temperature range, 78 to 295 K, the linear fit likely indicates electron-phonon scattering as the dominant scattering mechanism [1]. The difference in resistivity between 30 and 500 nm samples averaged 193% and between 30 and 100 averaged 26%, with the 30 nm sample showing lower resistivity in both cases.

Conclusions:

The increase in resistivity with thickness was independent of temperature, suggesting impurities as an underlying cause. The trend likely also results from differing surface roughness. As thicker layers are grown by the MBE method, surface roughness between interfaces tends to increase [4].

Future Work:

Based on these results, as well as data showing temperature dependent resistivity of 3 nm $La_xLu_{1-x}As$, a paper will be drafted describing electrical transition properties of rare earth arsenides. This paper, "Temperature dependent electrical resistivity and resistivity tuning of LuAs thin films by Lanthanum" (coauthors S. Rahimi, E.M. Krivoy, J. Lee, M.E. Michael, S.R. Bank, D. Akinwande), will be submitted to Applied Physics Letters.

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