Substrate Conformal Imprint Lithography

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Abstract:

Substrate conformal imprint lithography (SCIL) is capable of high resolution and is less sensitive to defects inherent in traditional nanoimprints. This makes SCIL promising for both research and industrial applications. We report here progress toward imprinting dense features at 15 nm critical dimensions (CDs). The study includes an improved process employing ZEP resist to minimize line edge roughness (LER) on the master wafer mold down to 2-3 nm. Imprinted features on initial trials were found to exhibit a negative linewidth change on the order of tens of nanometers. The SCIL process employs a wave generation process making localized and global distortions possible from stretching the flexible PDMS-on-glass stamp. To characterize this, we created a second SCIL mask and printed wafers for pattern placement accuracy tests over the entire area of imprinted wafers.

Introduction:

Moore's law predicted that the number of transistors on a chip should double roughly every two years, due, in part, to ever smaller dimensions. However, photolithography, the technique most commonly used today, is nearing the resolution limit imposed by the wavelength of light. One common method for patterning features smaller than photolithography can achieve is electron beam lithography, but this is prohibitively expensive and unfit for use in manufacturing because of the time required. Patterns made using electron beam lithography can, however, be replicated using NanoImprint lithography (NIL), at a fraction of the cost. NIL is a stamping process used to transfer features from a previously patterned master wafer into imprint resist on daughter wafers, which can then be cured. However, NIL faces its own challenges—the high pressures used and repeated exposure to resist can wear down features on the master wafer over time. Additionally, because the stamps used are inflexible, any particulates on them can result in unpatterned regions and can damage the master.

Substrate conformal imprint lithography (SCIL) [1] is a new variant of nanoimprint lithography using a flexible polydimethylsiloxane (PDMS) replica of the master wafer, making it possible to pattern over particulates. Also, because the master wafer is only used as a mold, it is better protected, which reduces the cost of repeatedly patterning new masters. However, because the stamp is flexible, it may induce distortion either of the printed features or in their placement on the wafer. We wanted to characterize that distortion and test SCIL's resolution limits to see whether it would be a good candidate for manufacturing at the nanoscale.

Methods:

In the SCIL process, PDMS stamps are molded from features etched into silicon master wafers. These stamps are then imprinted into a resist on daughter wafers, which are then UV cured. When the stamp is peeled away, the features are left behind in the resist on the daughter wafers.

To create the master templates, we used photolithography or electron beam lithography to pattern wafers which we etched using a reactive ion etcher. After removing any remaining resist, we added a monolayer of perfluorooctyltrichlorosilane (FOTS), a highly fluorinated molecule, as an anti-stick coating. We applied a layer of custom PDMS to the thin glass stamp and cured it to use as a SCIL mask. We imprinted these into wafers coated with Amonil (AMO, GmbH) resist using a modified Suss MA6 contact aligner. This tool allowed us to precisely control the imprint force and separation between the stamp and the imprint resist.

The first stamps we tested were made using an ASML 5500/300C deep ultraviolet stepper to pattern the master. This stamp was used to confirm that SCIL was capable of reproducing fine features over a large area as well as to troubleshoot any initial problems.

Tests of SCIL's resolution limit, however, required a master wafer with extremely small features. Towards this end, we created a dense pattern of 15 nm lines using electron beam lithography using ZEP520 (Zeon Chemical) as a resist. To achieve these challenging results, we used a combination of feature size biasing, dose biasing, and shot pitch modulation.

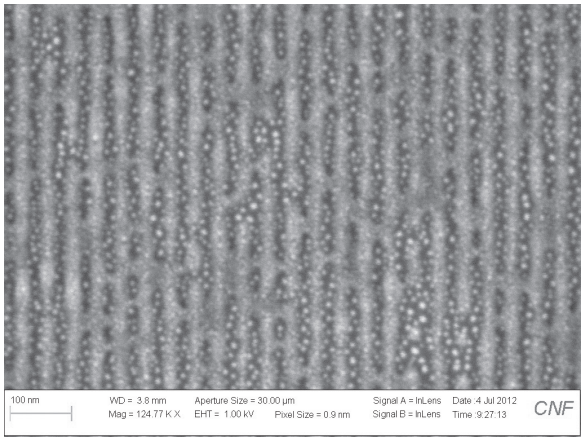

Figure 1: Early attempt to fabricate 20 nm trenches in ZEP520 resist before feature size biasing or cold development temperatures were used.

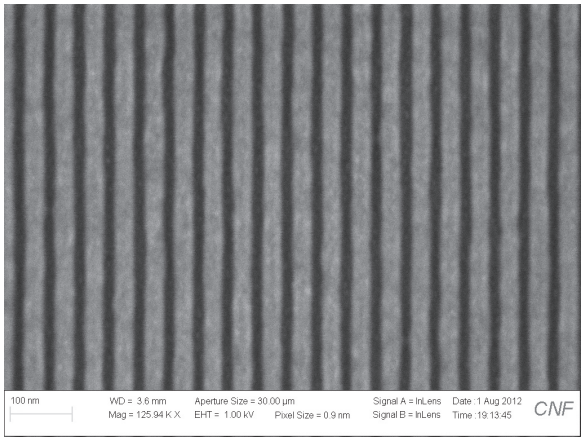

Figure 2: 15 nm trenches in 30 nm thick ZEP520 resist for patterning the master wafer needed for the SCIL resolution tests.

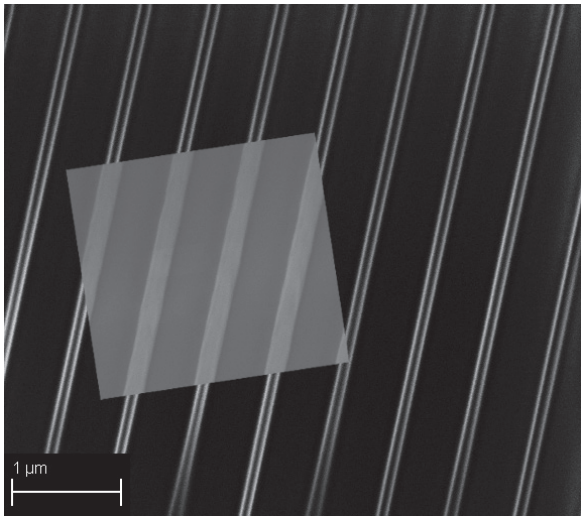

Figure 3: SCIL imprint and master wafer (inset) illustrating size changes in SCIL.

We also tested different development chemicals, temperatures, and times to optimize feature size and minimize LER. We also employed proximity error correction to compensate for the effect of backscattered electrons on the dosage [2].

The result was a silicon master wafer ideally suited to these resolution tests (Figures 1 and 2).

Finally, in order to characterize distortion in the pattern across the entirety of the wafer, we imprinted a stamp with an array of large crosses, 60 μm tall, onto a 6-inch wafer. Use of this stamp will indicate how accurately the stamp places these crosses across the wafer by comparing cross positions with the original master. The measurement will be made using the metrology capability of the JBX6300FS electron beam lithography system, which uses a laser interferometer to calibrate its stage position.

Results and Conclusions:

Using the stamp made with deep UV lithography, we initially confirmed that SCIL is capable of patterning submicron features over a broad area. We fabricated a stamp with crosses for the pattern placement accuracy tests, which we successfully imprinted. This awaits metrology measurements. To evaluate the resolution limits of SCIL, we optimized the process used to produce the master wafer. This process used cold xylenes as a developer and incorporated CAD corrections including proximity error correction and feature size biasing to improve resolution and LER. A master wafer with dense patterns of lines down to 15 nm was fabricated. Preliminary imprints with a similar mask demonstrate an overall decrease in linewidth of 80 nm from 170 nm lines as they were measured on the original master wafer (Figure 3). The source of this "shrinkage" has yet to be investigated.

Data from these pattern placement accuracy tests and resolution tests will make it possible to further improve the SCIL process in the future and to determine suitable applications for it as a manufacturing method.

References:

[1] Ji, Ran, et al., "UV Enhanced Substrate Conformal Imprint Lithography (UV-SCIL) Technique for Photonic Crystals Patterning in LED Manufacturing." Microelectronic Engineering 87.5-8 (2010): 963-67.

[2] Pavkovich, J., "Proximity Error Correction Calculations by the Integral Equation Approximate Solution Method." Journal of Vacuum Science and Technology 4.1 (1985): 159-63.