Fabrication and Characterization of Vertical Silicon Nanopillar Schottky Diodes

Adam Overvig
Engineering Physics, Cornell University

NNIN REU Site: ASU NanoFab, Arizona State University, Tempe, AZ
NNIN REU Principal Investigators: Stephen Goodnick and Clarence Tracy, Electrical Engineering, Arizona State University
NNIN REU Mentor: Nishant Chandra, Electrical Engineering, Arizona State University
Contact: aovervig@comcast.net, stephen.goodnick@asu.edu, cjtracy@asu.edu, nchandr5@asu.edu

Introduction:

Schottky (rectifying metal-semiconductor) contacts have widespread use, particularly in high frequency [1] and high power electronic devices [2]. It is important that Schottky diodes be miniaturized to preserve their functionality as devices shrink to the nanoscale [3], for applications such as voltage clamping, rectification in switched-mode power supplies, and reverse current protection in photovoltaic systems [4]. Standing upright, nanopillars can access vertical dimension in device fabrication, which is recognized as an important step in maintaining and/or surpassing Moore's law [5]. Here, we present a low temperature (no thermal oxide required), top-down process for fabricating arrays of vertical n-type silicon nanopillar Schottky diodes that can be incorporated into planar complementary metal oxide semiconductor (CMOS)-integrated circuits. We also characterize our metal-semiconductor (nickel-silicon) contacts and note that they differ from planar diodes.

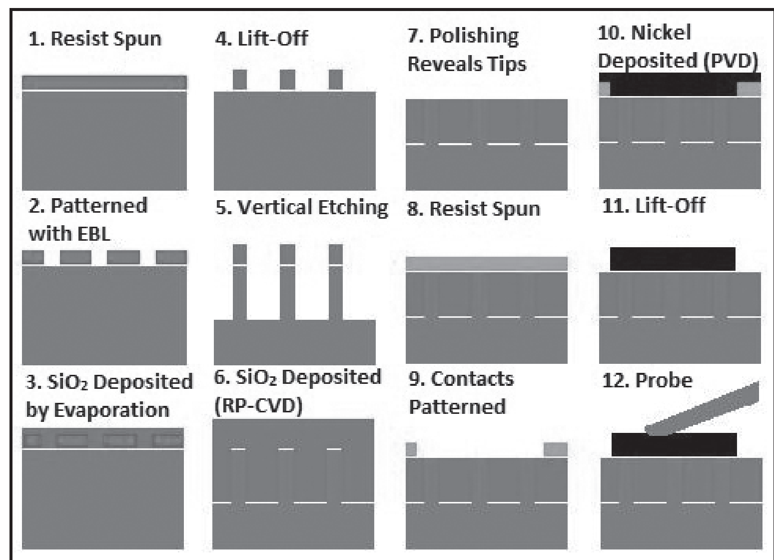

Figure 1: Schematic representation of fabrication process (not to scale).

Experimental Procedure:

A schematic representation of the fabrication process is shown in Figure 1. First, a hard mask of square-shaped SiO_2 islands (side lengths of 40 to 100 nm) was formed in arrays with a 4 μm pitch on an n-type (~ 2×10^{15} cm^{-3}) silicon (Si) substrate. This was done using electron beam lithography to expose arrays on a spin-coated 200 nm thick layer of 950K poly(methyl methacrylate) (PMMA). After developing the pattern at room temperature, roughly 50 nm of SiO_2 was deposited with electron-beam evaporation. The excess resist was dissolved in acetone, lifting off the oxide layer except for the SiO_2 islands.

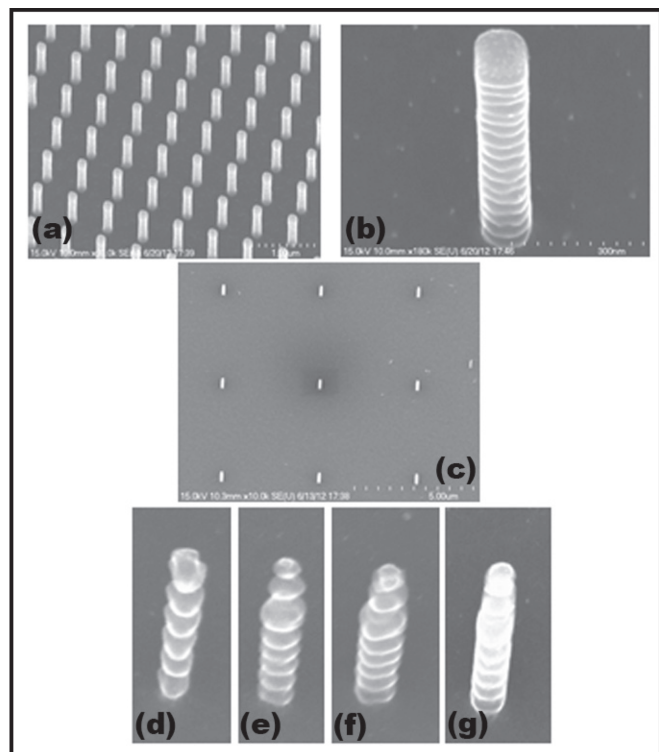

Figure 2: (a) SEM image of a 500 nm pitch array of 100 nm nanopillars after Bosch process using 4 sec etch, 2.5 sec deposition cycle. (b) Close-up of a 100 nm nanopillar in (a). (c) 4-micron pitch array of 100 nm diameter nanopillars obtained from using 8 sec etch, 5 sec deposition cycle. (d)-(g) Single nanopillars sized 40 nm, 60 nm, 80 nm, and 100 nm processed as in (c).

With this hard mask, nanopillars were formed with deep reactive-ion etching (RIE) making use of a Surface Technology Systems inductively coupled plasma (STS ICP) system. Employing what is known as the Bosch process, alternating modes of nearly anisotropic etching (using sulfur hexafluoride) and polymer deposition (using octafluorocyclobutane) produced vertical nanopillars approximately 1 μm tall.

Due to a small, unavoidable isotropic component in the etching mode, the nanopillar sidewalls were considerably scalloped. We were able to reduce the extent of scalloping by modifying the etching and deposition times during RIE. The resulting nanopillars are shown in Figure 2.

Finally, for support and electrical insulation, a conformal layer of SiO_2 was deposited using remote plasma chemical vapor deposition (RP-CVD). Chemical-mechanical polishing (CMP) then partially removed this layer, revealing the Si tips. 100 nm of nickel was sputtered after another electron beam lithography step patterned the contact windows. Excess nickel was lifted-off by ultrasonic agitation in an acetone bath, and rapid thermal annealing (RTA) formed a nickel silicide-silicon contact, creating the Schottky effect.

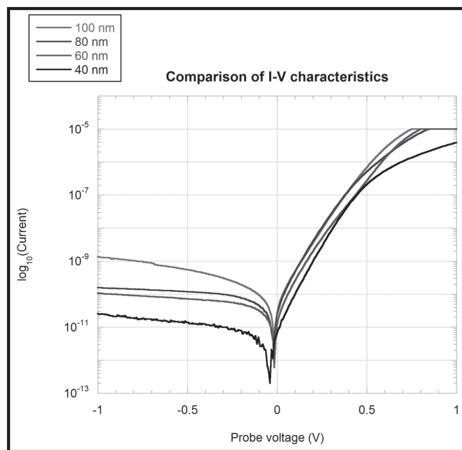

Figure 3: I-V characteristics of an array of 400 nanopillars of different diameters.

Results and Conclusions:

The resulting diodes' current-voltage characteristics (Figure 3) were analyzed to extract the barrier height, Φ_B; the ideality factor, n; and the series resistance, r_s in the thermionic current-voltage expressions (1) and (2):

$$I = I_s(\exp[q(V-Ir_s)/nkT)]-1) \quad (1)$$

$$I_s = AA^*T^2\exp[-qV/kT] \quad (2)$$

Where $q = 1.6 \times 10^{-19}$C, $k = 1.381 \times 10^{-23}$J/K, $T = 294$K, A is the diode contact area (assumed circular), and A^* is Richardson's constant, 112A/cm^{2}K^2 [6]. Typical values were 0.6 to 0.7eV for Φ_B, 1.5 to 2.5 for n, and 10 to 100 kΩ for r_s. These results confirm Schottky behavior.

An unexpected outcome that differentiates these diodes from planar diodes was non-ideal current scaling with respect to both number of diodes and radius. For the former, a linear relation was expected since the diodes are probed in parallel, but not observed: current ratios between the 40, 160, 240 to the 400 pillar array were roughly 1%, 10%, and 15%, respectively, compared to the expected 10%, 40%, and 60%. For the latter, dependence on area (radius squared) was expected because the heights of the nanopillars are consistent, but the power was found to be about 1.2 instead of 2. This indicates a dependence on perimeter size, and hence the increased importance of surface states due to a higher surface area to volume ratio.

Future Work:

Further research is needed to minimize scalloping to optimize nanopillar quality. The main parameter to be altered in this work should be the etch rate, in order to minimize the isotropy of the etching mode. Additionally, the non-ideal current scaling must be researched to be fully understood. One theory to account for this with respect to number of diodes is that a combination of inconsistent numbers of unintended "stray" nanopillars and faulty nanopillars are contacted with nickel, varying the actual amount probed from the assumed. Electron beam induced current (EBIC) is a method that could test this theory by illuminating the functioning diodes.

Acknowledgements:

Thank you to my mentor, Nishant Chandra, and my PIs, Drs. Stephen Goodnick and Clarence Tracy, for their time and effort. Additionally, to the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and the National Science Foundation for funding.

References:

[1] H.M. McGlothlin, D.T. Morisette, J.A. Cooper, and M.R. Melloch, "4 kV Silicon Carbide Schottky Diodes for High-Frequency Switching Applications," Device Research Conference Digest, 57th Annual, pp. 42-43, 1999.

[2] S. Steinhoff, M. Reddig, and S. Knigge, "A New Generation of 600V GaAs Schottky Diodes for High Power Density PFC Applications," PCIM Conference, Nuremburg, Germany, 2005.

[3] Q. Li, Y. Han, H. Min, and F. Zhou, "Fabrication and Modeling of Schottky Diode Integrated in Standard CMOS Process," White Papers Series, ed. 1, 2005.

[4] B.L. Sharma, "Metal-Semiconductor Schottky Barrier Junctions and Their Applications," New York: Plenum, 1984.

[5] G T. H. Lee, "A Vertical Leap for Microchips," Scientific American, vol. 286, pp. 52-59, 2002.

[6] D.K. Schroder, "Semiconductor Material and Device Characterization," 2nd ed., John Wiley and Sons, Inc., 1998.