Production and Characterization of Topological Insulators

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Abstract:

Topological insulators (TIs) represent a novel category of material whose bulk insulates, but whose surface conducts. The ability to produce topological insulators would be of great interest, because electron states can cross the insulating band gap, as well as surface conduction and spin-locking properties [1]. Bismuth selenide (Bi_2Se_3) is one of the best candidates for three dimensional (3D) TIs. Our project focuses on developing a method to produce undoped and doped Bi_2Se_3 via vapor-liquid-solid (VLS) deposition. Upon examination with a scanning electron microscope (SEM), energy dispersive x-ray spectroscopy (EDS) and x-ray diffraction (XRD), we found that both nanoribbons and nanowires about 5 μm in length formed; the doped sample with 61.4% selenium, 33.30% bismuth, 5.66% antimony by atomic percentage, and the undoped sample with 61.62% selenium and 38.38% bismuth. Being able to produce these doped and undoped topological insulators opens up exciting new avenues of research into their properties and possible applications.

Introduction:

In the last few years a new electronic crystal state was discovered, the topological insulator (TI). It is a unique state in which normal insulating states exist in conjunction with spin-momentum locked electronic states. These extra electronic states are the source of much interest due to the fact that they cross the electronic band gap, as shown in Figure 1; leading to various interesting properties [1]. However, these states are difficult to examine due to the fact that they only exist on the crystal's surface, and therefore could be masked by bulk conduction from unintentional doping. To eliminate this effect, nanostructures, such as wires and ribbons that have large surface-to-volume ratio, are the ideal structure to find these topologically insulating states.

In order to create the best TIs, we must choose the correct material. The material we chose in this case was bismuth selenide (Bi_2Se_3), due to the fact that it can exist as a nano-structured crystal, has a very simple band structure, is easily obtained, and can be doped with antimony [2].

Doping is the process where atoms in a crystal are substituted with similar atoms. In this case antimony substituted the bismuth atoms, which opened a band gap in the topological insulating states [3].

Our objective was to produce and characterize both antimony doped and undoped Bi_2Se_3 nanostructures in order to test TI properties.

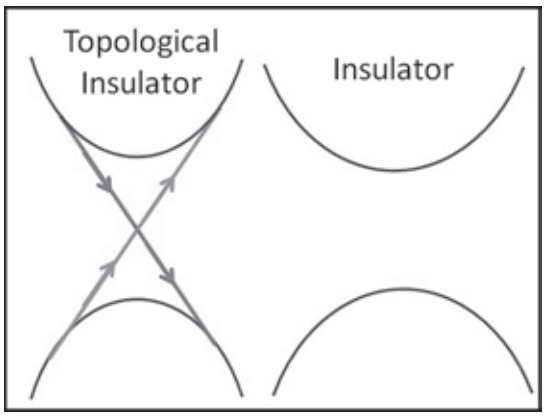

Figure 1, above: Band diagram of an insulator and a TI. The arrows represent spin-momentum locking.

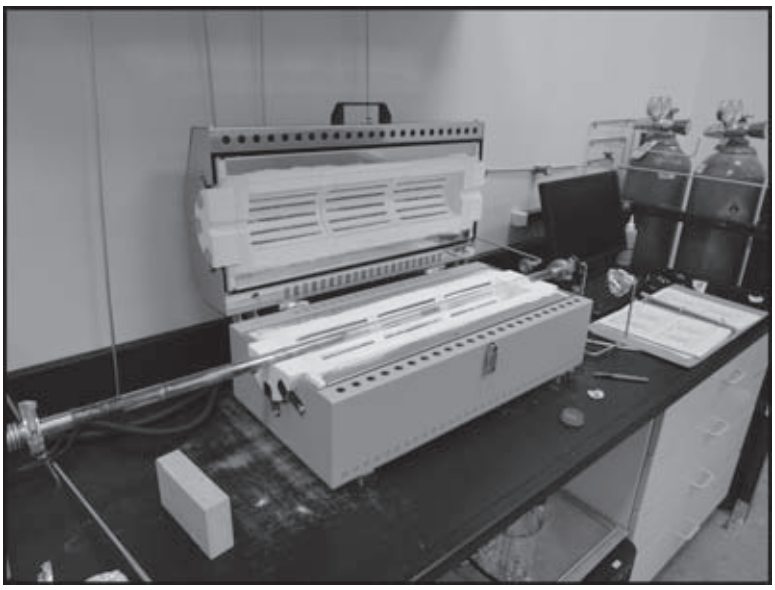

Figure 2, right: Our tube furnace setup where the growth took place, the crucible with Bi_2Se_3 at the center of the glass tube.

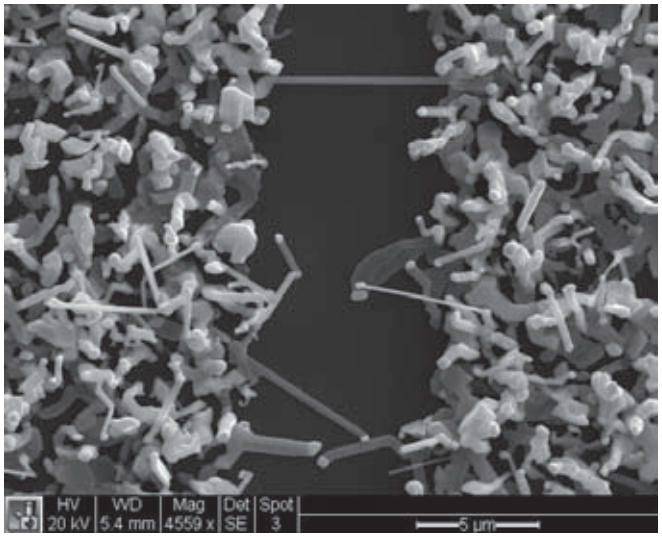

Figure 3: SEM image of Bi_2Se_3 wires 5-10 µm in length on a silicon substrate.

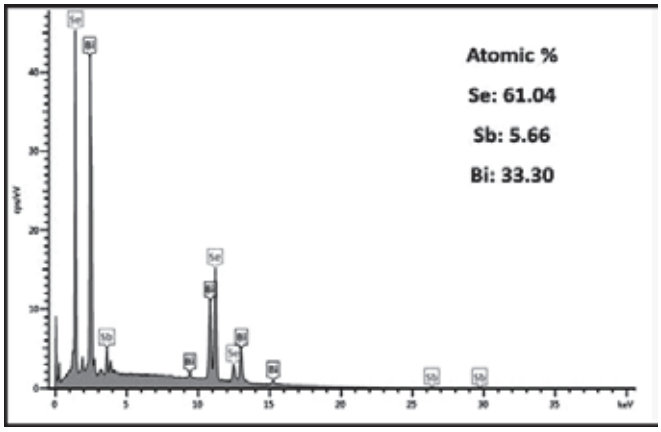

Figure 4: EDS graph on the atomic percentages of bismuth, selenium and antimony in a doped sample of Bi_2Se_3.

Methodology:

We went about producing the Bi_2Se_3 nanostructures via vapor-liquid-solid growth (VLS). In this process, the Bi_2Se_3 source material was heated up and then carried to the substrate by an inert carrier gas. The substrate itself was coated with a 20 nm gold film prior to growth, and also heated so that the film melted and beaded up. These gold droplets catalyzed crystal formation as the vapor Bi_2Se_3 deposited on the silicon substrate [4]. Our specific growth process used a tube furnace and argon as a carrier gas, as shown in Figure 2. The Bi_2Se_3 source was placed at the center of the furnace, while the substrate was placed 9-11 inches away (380°C ~ 450°C). The furnace was pumped down to 500 mtorr and heated to 490°C for 2.5 hours. The argon source was at a pressure of 12 psi.

Results:

Our growth resulted in many nanowires and some nano-ribbons forming that were 5-10 μm in length, as shown in Figure 3. The characterization with XRD showed that the crystal structure matched up with Bi_2Se_3 rather than other compounds containing bismuth and selenium. SEM and EDS verified that our bismuth selenium ratio was at 37.09% of bismuth and 62.91% of selenium, which was close to the expected 2:3 stoichiometry. Samples with antimony doping were characterized by EDS with atomic percentages of 33.30% bismuth, 61.04% selenium and 5.66% antimony, as shown in Figure 4, which agrees with direct substitution of bismuth with antimony.

Discussion and Future Work:

The production of these topological insulators was successful and matched our expectations. Now what is left to be done in this project is to perfect the drop casting method where the nanostructures are transferred from the silicon substrate to an insulating substrate in order to create electronic devices for testing.

Acknowledgements:

I would like to acknowledge the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and the National Science Foundation for allowing me this opportunity. I would also like to thank my principal investigator, Xiaodong Xu, my mentor Bo Zhao, and another member of the lab group, Jason Ross, for their help and guidance during this experience. I also wish to thank the Nanotech User Facility for their use of the equipment, and Paul Wallace for his aid in working with my material.

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AFM-Assisted Etching and Electrical Characterization of Graphene

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Abstract:

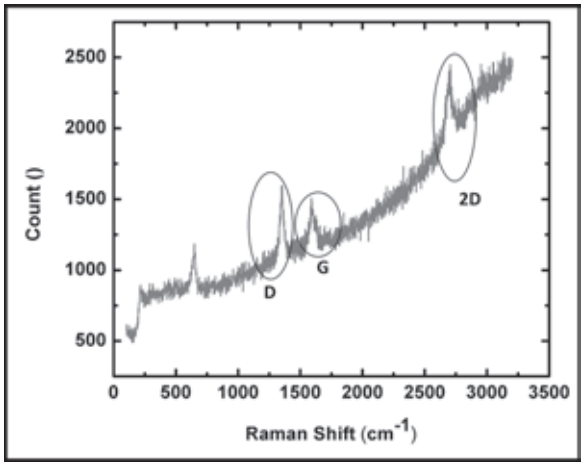
A pressure sensor, consisting of graphene transferred onto a chromium/ gold (Cr/Au) electrode and a silicon nitride (Si_3N_4) membrane, exhibits ultra high sensitivity. The device's high piezoresistivity was explored, and further measurements on the fabricated devices were taken for optimal design. Where typical, medical-grade pressure transducers have a sensitivity of 10 mV/V/mmHg, our device more than quadrupled this with as much as 50 mV/V/mmHg [1]. The transferred graphene was analyzed, employing scanning transmission electron microscopy (STEM), and both Raman and electron energy loss spectroscopy (EELS).

Introduction:

In the current era of electronics, the rate of increase in device density has decreased. Graphene, exhibiting exceedingly high electron mobility, has become a promising supplemental material to carry electrons for device operation, and its piezoresistivity has made it a candidate for high sensitivity strain transduction. Perfectly structured, low-area regions of mono-layered graphene have been produced through exfoliation, but larger areas are required for manufacturing. The process widely used for large-area synthesis involves chemical vapor deposition (CVD) on a copper substrate, and transferal via polymer. This commonly introduces impurities and defects within the graphene. Quality-assurance in the films can be verified through Raman spectroscopy and EELS, which respectively assure the number of layers and the composition of the film. STEM allows direct imaging of the film to verify the hexagonal crystal lattice.

Device Fabrication:

The device fabrication started with a double-sided polished (DSP), <100>, p-type silicon wafer, with 500 nm of low stress, low pressure CVD (LPCVD) silicon-nitride. After removing photoresist with an oxygen dry etch, an anisotropic KOH wet etch terminated on the nitride layer, forming the membrane. Electron-beam evaporated electrodes, consisting of 140 nm of gold on top of a 10 nm chromium adhesion layer, were patterned through optical lithography and lift-off in warm acetone. Copper (99.8%) foil was cleaned in chrome etchant, dried, and placed in a nanotube furnace, optimized to grow graphene through low pressure chemical vapor



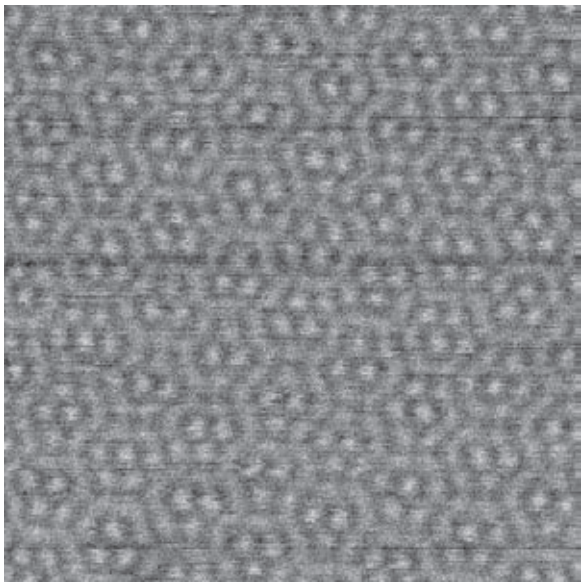


Figure 1, top: Raman spectroscopy of graphene on copper substrate, where the D, G, and 2D peaks characteristic of graphene are shown. The D peak, which shows defects within the lattice, is very high in this particular sample. The G peak verifies the sp^2-bonds of graphene. The 2D peak can be used for identifying the number of layers. In this case, it is likely mono or bilayer graphene.

Figure 2, bottom: Nion STEM image of multi-layer graphene. Honeycomb atomic structure visible.

deposition (LPCVD). Poly(methyl methacrylate) (PMMA) was spun onto each sample at 4000 rpm for one minute, and the copper was removed with iron (III) chloride etchant. After transferal through five baths of deionized water, each sample was placed onto the device membrane and left to dry. Lastly, the PMMA was ashed in a 325ºC air ambient for three hours.

Graphene Quality Measurements:

High-quality graphene consists of planar, sp^2-bound carbon atoms in a crystalline, honeycomb lattice. Raman spectroscopy was used to characterize the thickness of the carbon films. For our pressure sensor, multilayered graphene was suitable. Figure 1 shows a Raman spectrogram of graphene on Cu-foil. The background noise is due to the copper, but the D (defect), G (graphitic), and 2D peaks of graphene are clearly visible. STEM imaging of suspended graphene sheets is shown in Figure 2: an image of the atomic structure of a multi-layered film. The large defect peak of the sample shown is not necessarily representative of the graphene on our devices, as the growth process was improved. However, machinery issues hindered the acquisition of a better plot.

An unexpected finding of our film characterization was iron residue from the Cu-etching process. EELS confirmed a considerable amount of iron was found on our sample, but the existence of this iron has not shown to interfere with the efficacy of the device (Figure 3).

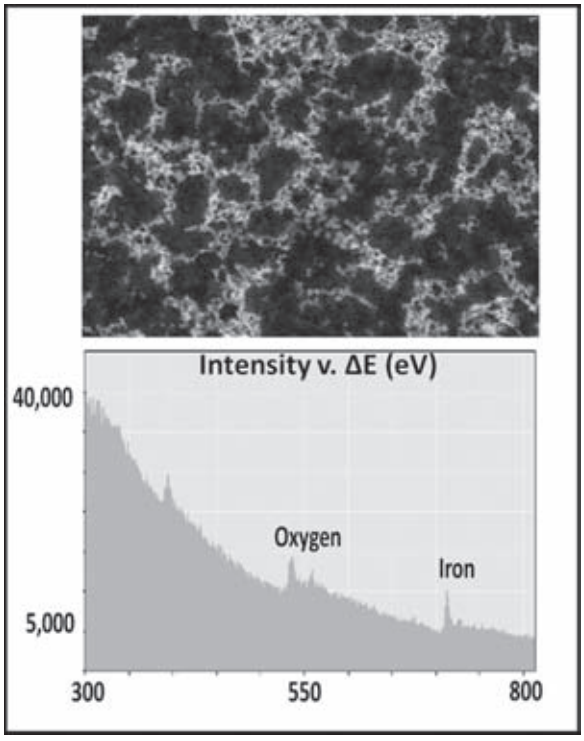


Figure 3: Nion STEM image of graphene on 50 nm silicon nitride (top). The amorphous, high-contrast material confirmed to be iron through EELS, coming from the copper etchant used in the graphene transfer protocol (bottom).

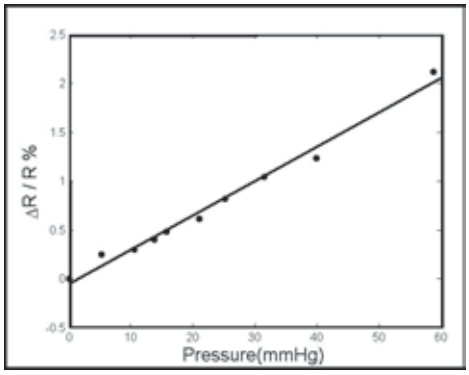


Figure 4: Fractional change in resistance vs. the applied pressure (mmHg). The current device, exhibiting 25% change at 5 mmHg, may be more sensitive for small pressures than its predecessor, which reached 15% at 6 mmHg. More measurements must be done for verification.

Pressure Sensitivity Measurements:

The set of four electrodes on each device were used for four-point probe measurements, using an applied pressure drop and measuring the corresponding change in resistance (Figure 4). The applied pressure causes strain in the graphene film, changing its resistance. As stated in the original paper for this device, the pressure sensor should be highly non-linear [2]. However, the thicker membrane used in this study did not rupture and reached significantly higher pressures than expected from the first study. It is therefore possible that the results displayed here are all within a relatively linear regime. Further measurements were not able to be taken to confirm this hypothesis.

Conclusions:

The current device is a viable microelectromechanical systems (MEMS) sensor, suitable for high sensitivity applications without requiring linearity. Further measurements will have to be taken. Hall effect measurements through the Van der Pauw method will have to be done to obtain the electron mobility of our graphene samples. Ascertaining piezoresistive non-linearity in the sensor via applied pressure, and actuating the membrane at resonance and using optical interferometry to determine strain, will be the likely next steps.

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Engineering the Charge Occupancy of Nitrogen Vacancies in Diamond

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Introduction:

Nitrogen vacancy (NV) centers are point defects in a diamond lattice that occur when a carbon atom is substituted with a nitrogen atom while a neighboring carbon atom is removed entirely. The resulting gap in the lattice has many desirable properties, such as paramagnetism and optical energy level transitions, that make it an ideal candidate for single-photon optics and quantum computing applications [1]. But the NV center tends to lose one of its surrounding electrons due to recombination with wandering positive charges in the crystal, providing a damaging barrier to the development of large-scale, multipartite quantum networks.

This project sought to deter this process by depositing transparent metal oxides and films on the surface of diamond nanowires, with a goal of inducing charge discontinuities at the surface that would stabilize the electronic configuration of the lattice by inducing a negative charge excess in the region around the defect. Additionally, metal oxide semiconductor field effect transistor (MOSFET) devices were designed that used a voltage gate on the surface of bulk diamond to accomplish the same effect, albeit with more control of the dopant level in the region due to modulation of surface voltage [2]. Designs and fabrication processes for both devices were created and ensemble measurements of devices using confocal microscopy have begun.

Procedure:

Nanowire Fabrication. High-temperature, high-pressure Type Ib diamonds were obtained (HPHT, Element Six) and polished, and surface contaminants were removed with a boiling bath of equal parts perchloric, sulfuric, and nitric acid. 1%XR was spin-coated onto the diamond surface, followed by equal parts FOx-16 and methyl isobutyl ketone resists. Arrays of disks ranging from 200 nm to 250 nm in diameter were then patterned with varying dosages using an electron beam lithography system (Elionix ELS-F125). Tetra-methyl ammonium hydroxide was used to develop the resist, and reactive ion etching was used to carve away diamond from around the disk patterns, creating pillars roughly 1.5 microns in height. Excess resist was removed using boiling Piranha etch (80% sulfuric acid, 20% hydrogen peroxide). Surface oxides were then deposited using atomic later deposition (50 nm SiO_2 and 16 nm Al_2O_3), and the nanowires subsequently underwent rapid thermal annealing (three hours in O_2).

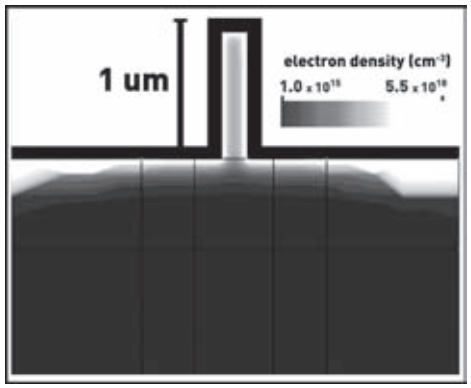

Figure 1: A finite element simulation of doping in a diamond nanowire due to a surface coating of silicon dioxide.

MOSFET Fabrication. Diamonds were obtained and cleaned in the same manner as the nanowire samples. Using plasma-enhanced chemical vapor deposition, the polished surface was coated with 400 nm of silicon dioxide, onto which HDMS primer and SH1813 photoresist were spin-coated consecutively. Exposure was performed using direct write photolithography on a Heidelberg uPG501 with typical doses in the range of 100mJ. The patterned sample was then developed and placed in buffered oxide etch for two minutes. After cleaning and optical inspection, the sample was coated with 300 nm lift-off resist LOR 3 3A followed by 500 nm SH1805. A second mask was then aligned to the visible oxide pattern and exposed with the same dosage. The SH1805 was developed, and the sample was then covered with 150 nm of gold using electron beam evaporation. The assembly was left overnight in Remover-PG at 80°C for gold lift-off. After the gold contacts were inspected and the sample was cleaned, 500 nm indium tin oxide was deposited on the sample using sputtering (AJA Orion 3) and then topped with HDMS/SH1813 photoresists in the same manner as the first layer. A final mask was aligned and exposed, and the ITO layer was then chemically etched using a mixture of equal parts concentrated hydrochloric acid and water.

Results and Future Work:

Based on numerical models, devices were designed and fabricated that locally doped the diamond surface by donating free electrons into the diamond conduction band. Nanowires [3] were chosen to receive passivation coatings because they had a high

ratio of surface area to volume, allowing maximal theoretical carrier concentration around the vacancy center (Figure 1).

After recipe optimization, wires were successfully created on the surface of bulk diamond that exhibited satisfactory deposition uniformity for two different oxides (Figure 2), suggesting that the method successfully can be adapted for a variety of different oxides and thicknesses.

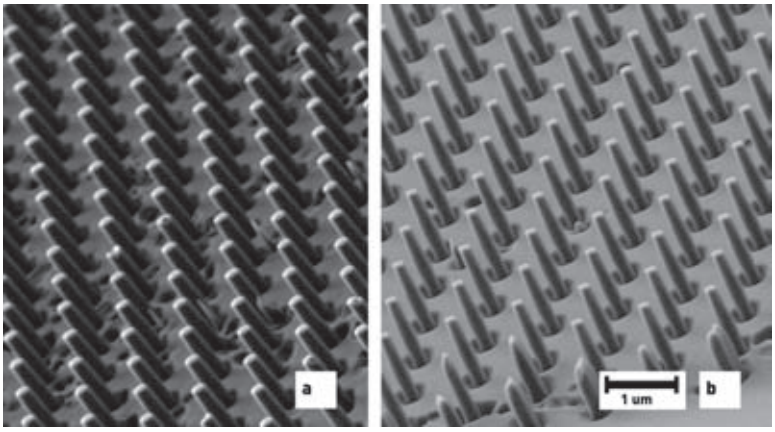

Figure 2: Diamond nanowires that have been coated with (a) 50 nm silicon dioxide, and (b) 22 nm aluminum oxide.

MOSFET devices were designed that adhered to material parameters determined by numerical simulations while allowing experimental flexibility. A three-mask photolithography process, including a gold lift-off step, was designed and optimized to yield high fidelity to the original digital design (Figure 3). While the process was originally developed on a silicon substrate for convenience, some difficulty was encountered in adapting the method for a smaller (2.5 mm square) diamond substrate, in part due to difficulty focusing and aligning on a smaller sample. These problems are purely technical in nature, and are expected to be resolved by the use of a specialized sample holder for the diamond during the lithography process.

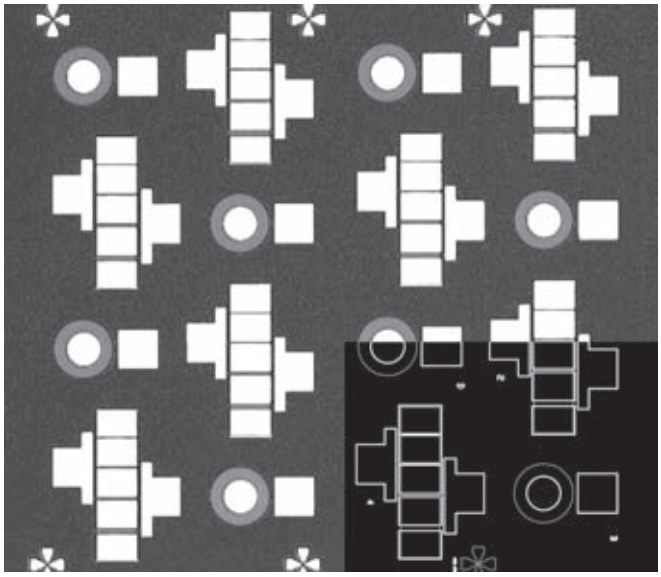

Figure 3: MOSFET structures on silicon. The smaller disks are 60 µm in diameter, and the original CAD design is inset.

Anti-correlation was successfully measured in photons emitted from the devices, and the nanowires yielded a clear fluorescence signal under laser excitation (Figure 4). Repeated measurements of ensembles of each type of device, however, are necessary to determine whether there is a significant increase in fluorescence from diamonds with devices, which would signal successful charge state stabilization of NV centers.

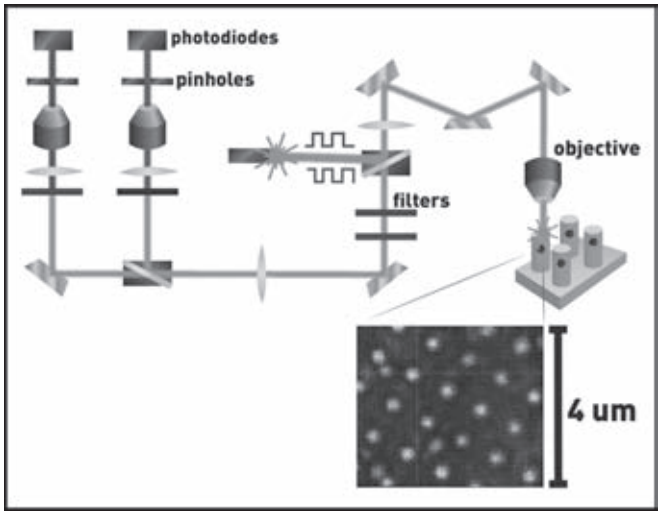

Figure 4: The confocal microscopy measurement setup, with a sample image of NV centers in nanowires.

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Sacrificial Polymers and Their use in Patternable Air-Gap Fabrication

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Abstract:

Patternable air-gaps are added to electrical and mechanical structures in semiconductor and MEMS devices as a means to decrease the dielectric constant, add mechanical compliance, and facilitate microfluidics. In this study, sacrificial polymers and standard photolithographic techniques were used as a way to create air gaps. A photodefinable sacrificial polymer was created by adding photoacid generator (PAG) to the sacrificial polymer mixture. Air gaps were made by patterning the sacrificial polymer into the desired structure, covering it with an overcoat polymer, and decomposing the remaining sacrificial material. There are three problems associated with this fabrication technique: (i) the patterning resolution was coarse, (ii) residue was produced during the decomposition of the polymer, and (iii) wide structures tended to collapse. These problems were investigated through process optimization, quartz crystal microbalance (QCM), and overcoat modification, respectively. In addition, a new sacrificial polymer, PDM-1088, was investigated. PDM-1088 increased the resolution of the pattern, QCM measurements indicated the amount of remaining residue, and hardening the overcoat allowed the fabrication of structures several hundred micrometers wide. Micrometer scale air gaps were successfully fabricated through common photolithographic techniques, permitting the integration of these structures into semiconductor processing.

Introduction:

Air-gaps have yet to be created using standard electronics processing techniques. They are desirable for use in semiconductor and MEMS devices as a means to decrease dielectric constant, add mechanical compliance, and facilitate microfluidics. In this study, photopatternable air-gaps were successfully fabricated by improving each of the three major problems associated with sacrificial polymers: i) difficulty patterning the sacrificial polymer, ii) residue after decomposition, and iii) wide structure collapse.

Experimental Procedure:

Sacrificial polymers were used to create patternable air gaps. First, a new polymer, PDM-1088, was mixed with a photoacid generator (PAG) so that it could be patterned. The PAG released a proton upon heating or by exposure to 248 nm UV light. The acid significantly decreased the decomposition temperature of the sacrificial polymer.

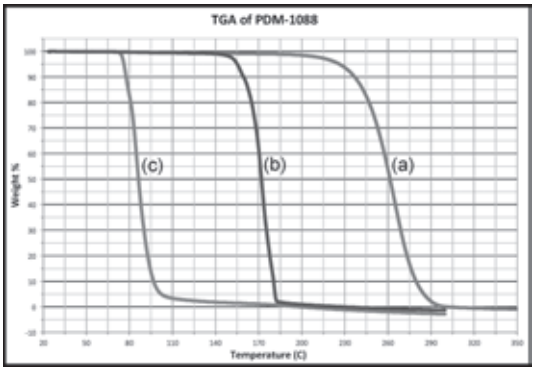

Figure 1: Thermogravimetric analysis graph of PDM-1088; (a) without additives, (b) loaded with PAG, and (c) loaded with PAG and exposed to 248 nm UV light.

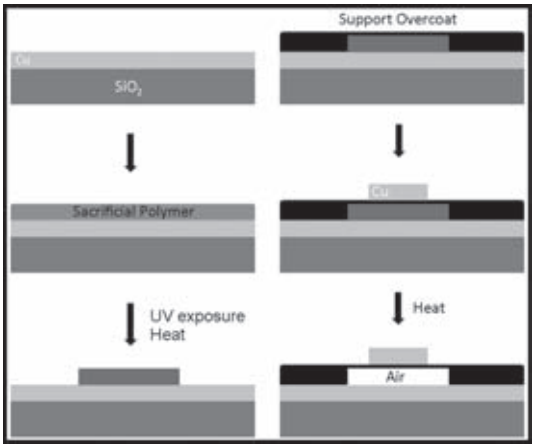

Figure 2: Schematic of air gap fabrication method.

As shown in Figure 1, PDM-1088 mixed with PAG has a lower decomposition temperature (170°C) than the next polymer (260°C) and the exposed polymer/PAG mix has an even lower decomposition temperature (85°C).

Through standard photolithography, as explained in Figure 2, PDM-1088 was spin-coated onto a copper (Cu)-sputtered

silicon wafer and a pattern was exposed. Upon heating to 120°C, the exposed portions decomposed. An overcoat material was then spin-coated onto the sample. Two different overcoat polymers were used in this study; polyimide and Avatrel 8000 (polynorbornene). The overcoat was then exposed to 365 nm UV light to activate the polymer cross-linkers and was cured at 150°C for one hour. Finally, the sample was exposed a second time at 248 nm, activating all remaining PAG, followed by a six hour cure at 150°C to decompose the remaining PDM-1088.

Results:

There are three major issues associated with this processing technique: i) patterns are coarse due to polymer reflow and proton diffusion, ii) the polymer leaves behind a notable residue after decomposition, and iii) wide structures tend to collapse in the center due to surface tension. These problems were solved systematically by modifying the processing approach in three ways.

PDM-1088 has a glass transition temperature of 90°C, which is higher than previous sacrificial polymers. Decreasing the processing temperature increased control of the polymer reflow resulting in the fabrication of clean patterns.

Quartz crystal microbalance (QCM) was used to measure the mass left behind after polymer decomposition. This quantification of the residue allowed modification of the processing techniques, polymer choice, and PAG loading to achieve minimal residue. Polymer samples were spin-coated onto quartz crystals. The crystal was allowed to equilibrate to its resonant frequency in the QCM, and then the residue was washed off without removing the sample from the instrument. Finally, the solvents were evaporated at room temperature and the crystal equilibrated again to its resonant frequency. The change in frequency allowed us to use the Sauerbrey equation [1] to calculate the mass of the residue left on the crystal. Figure 3 shows the linear relationship between polymer thickness and residue, meaning the residue is dependent on the composition of the formulation.

Wide air-gap structures were successfully fabricated by modifying the overcoat material. Avatrel 8000 was not strong enough to hold up air-gaps wider than 100 μm as the surface tension pulled the overcoat onto the substrate. To strengthen the Avatrel, extra trimethylolpropane triglycidyl ether (TMPTGE) was added to the polymer. TMPTGE is a trifunctional polymer crosslinker used with Avatrel 8000, and the addition significantly increased the hardness, as seen in Table 1. By increasing the hardness, the resulting polymer was able to withstand surface tension pull, even at a thickness of 7 μm. Adding TMPTGE worked significantly better than several other attempted methods, including the addition of surfactant (Triton X-100) and the addition of a second, glass-like polymer (epoxycyclohexyl polyhedral oligomeric silsesquioxane, or POSS).

Conclusions:

By modifying processing methods and incorporating the use of PDM-1088, we successfully fabricated air gaps several hundred micrometers wide and only 5 μm tall. For the first time, such structures were achieved with an overcoat thickness less than 10 μm.

Future Work:

The fabrication method we developed can now be used in direct applications including electronic interconnects, MEMS, and microfluidics. More work needs to be completed to increase resolution, reduce residue, and create wide structures for certain applications.

Acknowledgments:

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References:

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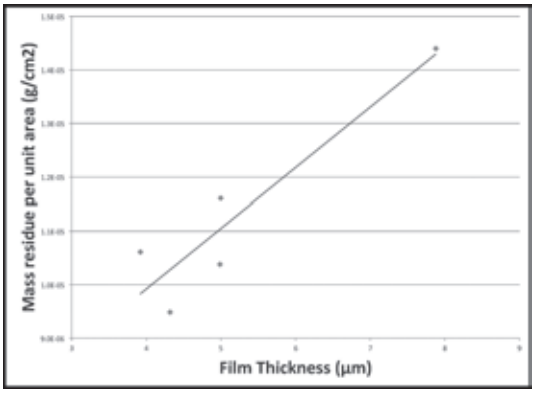

Figure 3: QCM results of mass residue vs. polymer thickness (PDM-1088 with PAG).

Overcoat	Elastic Modulus (GPa)	Hardness (GPa)
Avatrel	2.44	0.155
Avatrel + TMPTGE	3.19	0.199
Avatrel + POSS	1.49	0.169
Air Gap	0.71	0.121

Table 1: Hardness and elastic modulus values of modified Avatrel 8000 overcoats.

Biomineralized Nanopore Membranes on Silicon for Nanoparticle Translocation

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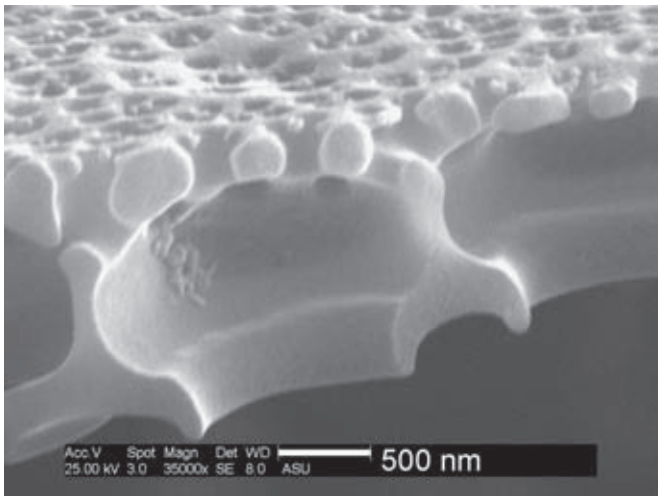

Figure 1: Scanning electron micrograph of the cross section of a diatom showing the different pore sizes.

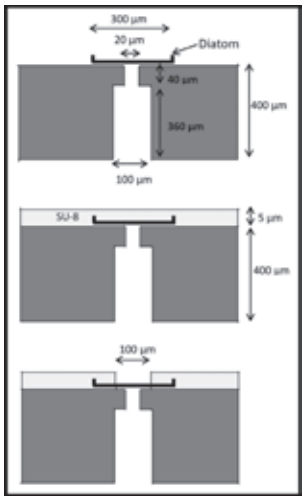

Figure 2: Schematic diagram of fabrication process.

Abstract and Introduction:

Nanopores have many biological applications. They can be used as single molecule detectors, deoxyribonucleic acid (DNA) sequencing, and potentially be functionalized to simulate lipid bilayers or nuclear pore complexes. However, these nanopores are expensive and time consuming to make using conventional microfabrication techniques. An alternative to these top-down processed nanopores is diatoms. Diatoms are a major group of algae that synthesize a three-tier network of silica pores for their cell wall, which can be seen in Figure 1. They can grow up to 300 μm in diameter, yet the smallest pores are approximately 40 nm wide. In order to have access to these nanopores, the diatoms need to be positioned and immobilized over 20 μm pores etched through silicon wafers.

Currently, the diatoms are manually placed over the pores and a UV curable epoxy, Norland optical adhesive-60 (NOA-60), is manually dispensed around the diatom. In order to create a more efficient process with a higher yield, standard contact lithography was explored to immobilize the diatoms over the micropore. The criteria used to determine the effectiveness of the process was to check for absence of leakages, breaking of the diatom or clogging of the nanopores.

Two photoresists were tested, SU-8 and NOA-60. SU-8 is a negative UV-curable photoresist that is well established in contact lithography. NOA-60 is polyurethane-based resin that adheres to glass. Therefore, it requires an anti-adhesion layer to enable release from the glass mask and the sample. Polydimethylsiloxane (PDMS) was used as the anti-adhesion layer as suggested in [1].

However, our experiments proved that the PDMS layer was ineffective in enabling separation of photomask and substrate after UV exposure. SU-8 proved to be successful in meeting the criteria in combination with a sulfuric-peroxide mixture (SPM) treatment.

Fabrication Process:

Oxidized silicon wafers with through-wafer pores were used as substrates. The pore diameter on the back side of the wafer was 100 μm and the pore diameter on the front side was 20 μm. Details on the fabrication process of the silicon micropores can be found in [2].

Diatoms were deposited on the wafer from a 1:1 water:ethanol solution and positioned over the silicon the micropore using a micromanipulator. Subsequently, positively charged poly-L-lysine was used to form a temporary bond between the negatively charged diatom and the oxidized silicon wafer. After poly-L-lysine was deposited on the chip, SU-8 3005 was spun on at 3,000 rpm for 30 seconds. Once the post-exposure bake was completed, the mask consisting of a 100 μm dot was aligned over the 20 μm through-wafer pore. Exposure was completed on an EVG-620 with a dose of 350 mJ.

After the post-exposure bake, the chip was developed in SU-8 developer for two minutes and rinsed with isopropyl alcohol. A schematic of the process can be seen in Figure 2. The SPM treatment was completed using a 3:1 ratio of sulfuric acid to

peroxide. The diatom chip was placed in the mixture for two minutes.

Results and Discussion:

Indication of open pores was found by testing for nanoparticle translocations using the setup in Figure 3. The diatom chip was placed between two chambers containing a nanoparticle solution of 100 nm polystyrene beads. Silver chloride-coated silver (Ag/AgCl) electrodes were inserted in each chamber and a constant voltage of 400 mV was applied. When a particle passed through a diatom nanopore, it changed the electrical resistance. Using the equation V = IR, a resistance increase lead to a decrease in current at a constant voltage. Therefore, a nanoparticle passing event resulted in a quick dip in ionic current.

Figure 3 shows the graph of multiple 100 nm polystyrene bead translocation events through diatom pores. The negative value of the current is due to an offset caused by the Ag/AgCl electrodes that have to pass the current. This also leads to the drift in baseline current.

One of the major concerns of using SU-8 was the possible stress it could put on the diatom during the baking process, which could cause cracking and breaking of the diatom. It can be seen in Figure 4 that SU-8 does not exert any excessive stress on the diatom. The SU-8 layer also formed a clean, complete seal around the diatom.

Conclusions:

The process described proved to be successful in immobilizing the diatoms without any leaks, breaking, and clogging the diatom's nanopores. It was found that NOA-60 was problematic to use via contact lithography, because its strong adhesion to glass, and even PDMS, prevented clean separation of the substrate from the photomask. The SPM treatment was effective in removing residual SU-8. However it is still unclear how much the cleaning step affects the pore size of the nanopores, because the size of the pores varies with each diatom.

Future Work:

Future work includes testing to determine the effect of the SPM treatment on the diatom membrane as well as a process for positioning and securing multiple diatoms over the micropores without using a micromanipulator.

Acknowledgements:

I would like to thank my PI, Dr. Michael Goryll, and my mentor, Xiaofeng Wang, for their guidance and time, and the staff at the Center for Solid State Electronics Research at Arizona State University. I would also like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program and the National Science Foundation for funding this great experience.

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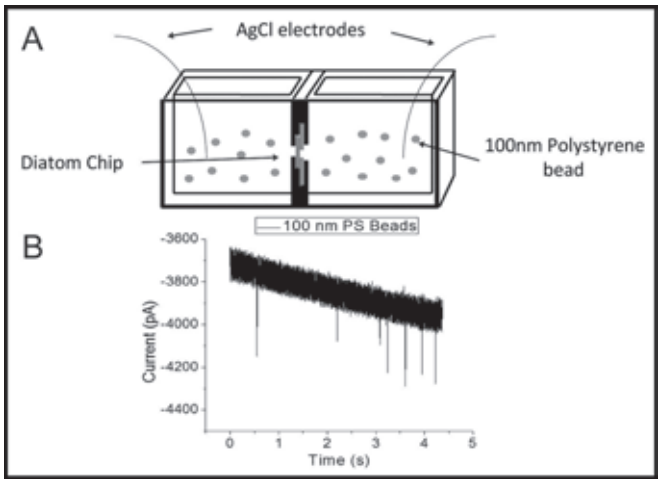

Figure 3: (a) Nanoparticle translocation setup. (b) Graph of multiple 100 nm polystyrene bead translocation events through open pores.

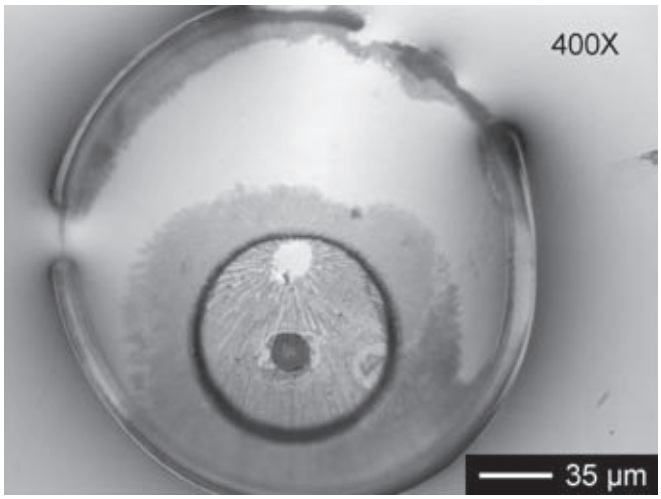

Figure 4: Optical micrograph of diatom after SU-8 coating and exposure.

Fabrication of Graphene Field Effect Transistors

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Abstract:

Graphene is an exciting new material because of its two-dimensional nature and interesting mechanical and electrical properties. There is still much room for development in methods for growing graphene, such as chemical vapor deposition (CVD) on copper. Making field effect transistors (FETs) with graphene is a practical way to assess the characteristics of a given sample of graphene and determine if a method for creating graphene is effective. The focus of this project was to fabricate graphene FETs to assess the quality of graphene grown through CVD on copper. This process was broken down into three main steps: (1) the electrochemical transfer of graphene from copper to silicon (Si) wafers, (2) the patterning of electrodes onto the graphene covered wafers, and (3) the electrical testing of resulting devices through four-point-probe and transistor measurements. Graphene was transferred through the application and removal of poly(methyl methacrylate) (PMMA) on copper (Cu). The electrodes were patterned using photolithography and evaporative metal deposition. Four-point-probe and transistor measurements were attempted as a means to assess the sheet resistance, carrier mobility, and carrier density of the graphene.

Introduction:

In the future, graphene may be used in a wide variety of devices, but if these devices are ever going to be produced commercially, there needs to be much improvement in methods for growing high quality graphene. The purpose of this project was to fabricate graphene field effect transistors (FETs) to assess the quality of graphene grown through CVD on Cu and examine problems in the fabrication process.

Experimental Procedure:

The experimental procedure broke down into five main steps: (1) the preparation of the substrate, (2) the transfer of graphene from copper onto the substrate, (3) the patterning of electrodes onto the graphene, (4) the deposition of the back-gate metal, and (5) the characterization of the graphene.

A heavily doped Si wafer (n-type, <100>, 0.01-0.02 Ω-cm) was used as the substrate for the graphene FETs. The wafer had to be oxidized to have an oxide thickness of 90 nm so that the graphene would be visible on top of the oxide [1].

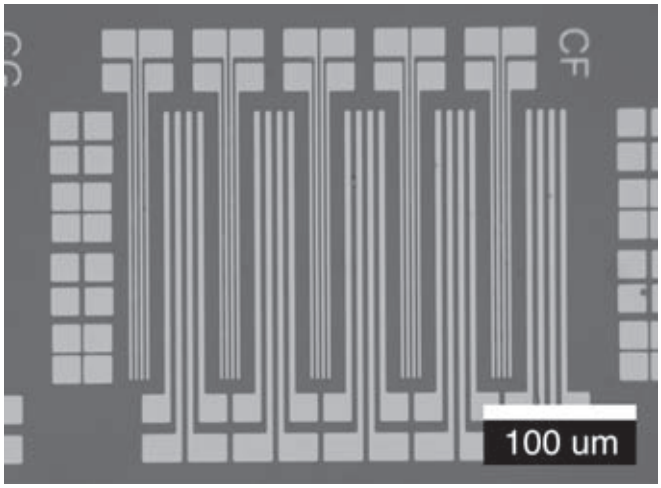

Figure 1: Electrode pattern; small fingers are 2 µm wide and large fingers are 4 µm wide.

Graphene was transferred from copper to the substrate through an electrochemical reaction. Poly(methyl methacrylate) (PMMA) was spun onto the copper sheet before hooking up the copper sheet to function as a cathode in a potassium hydroxide (KOH) bath with a steel electrode serving as the anode. Hydrogen gas forming on the surface of the copper lifted off the PMMA, with the graphene attached to its underside. This sheet of PMMA was then cleaned and scooped up with the substrate.

After removing the PMMA with remover PG and annealing the sample to clean the graphene, electrodes were patterned onto the surface of the graphene in a pattern that can be seen in Figure 1 through photolithography and evaporative metal deposition.

The final fabrication step was the deposition of the back-gate metal. The back-gate metal was deposited after stripping away the backside oxide with buffered oxide etch (BOE).

Characterization was done through use of a probe station and parameter analyzer. The goal was to use four-point-probe and transistor measurements, though in the end, only four-point-probe measurements were conducted.

Results and Conclusions:

Three main problems were encountered during fabrication: (1) the oxide had to have a specific thickness, (2) the transfer process caused the graphene to fold up on itself, as shown in Figures 2 and 3, and (3) the nickel electrodes adhered poorly to the graphene, as shown in Figure 4.

The first problem was addressed through using dry oxidation to make the oxide slightly thicker than desired and then using BOE to fine-tune the thickness of the oxide. The second problem was caused by remover PG attacking photoresist residue under the graphene during the PMMA removal step. This problem was addressed by changing the order of fabrication steps to allow for nanostrip cleaning directly before transfer to ensure that the surface of the substrate was clean. Given the limited amount of time for the research project, the third problem was not addressed although possible solutions have been formulated.

Due to the problems with fabrication, data was only successfully collected from a single device as the electrodes proved difficult to probe. The four-point-probe measurement suggested a sheet resistance of 7700 Ω/sq with very high probe contact resistances of 200 Ω per contact, and a nickel-graphene contact resistance of 5.38×10^{-4} Ω-cm^2. The measured sheet resistance was 20 times higher than expected, likely because of uneven contact between the nickel and graphene and discontinuities within the graphene sheet.

Three main ideas have been put forward to address the nickel-graphene adhesion problem in the future. First, the mask should be redesigned to have larger probe pads to make probing the devices easier. Second, new metals, such as platinum, should be experimented with as possible nickel substitutes. Finally, a reactive ion etching step might be done to etch the graphene into strips before patterning electrodes onto the surface so that contact pads can remain on the oxide with only fingers on the graphene. After this problem is addressed, more characterization needs to be done.

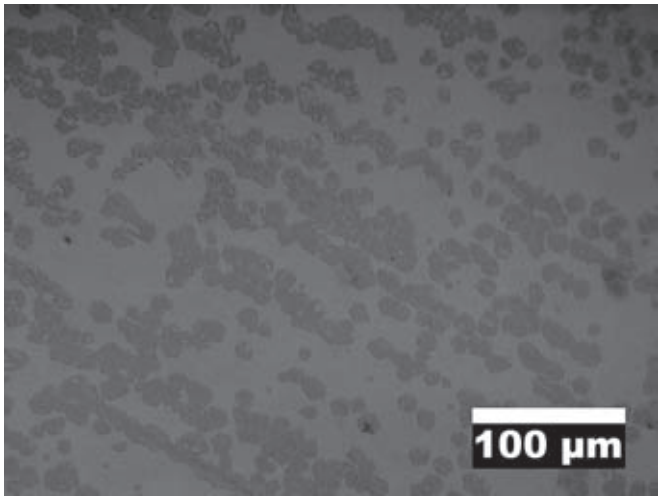

Figure 2: Graphene prior to PMMA removal.

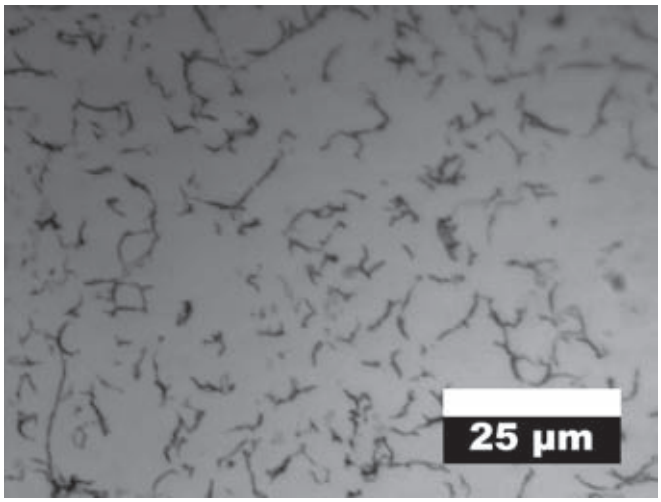

Figure 3: Graphene after PMMA removal.

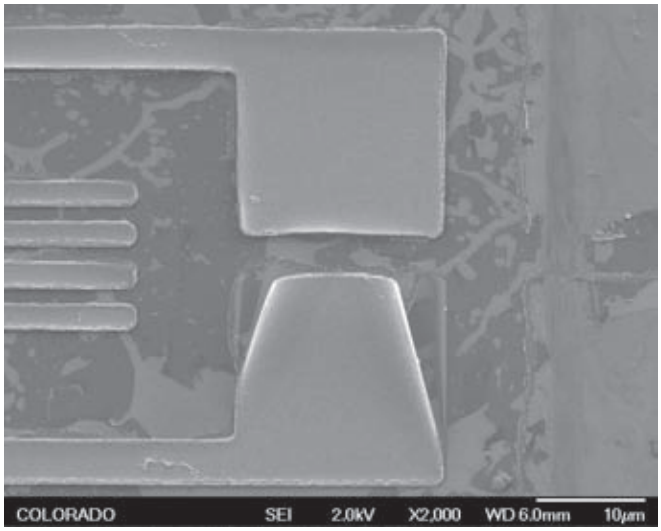

Figure 4: Nickel electrodes over graphene.

Acknowledgements:

I would like to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program for giving me the opportunity to do this research, the National Science Foundation for providing the funding, and the University of Colorado at Boulder and the Colorado Nanofabrication Lab for providing an excellent setting to conduct research. I would also like to thank my research group, Bart Van Zeghbroeck, Zefram Marks, Ian Haygood, Tomoko Borsa, and especially Tzu-Min Ou, for all of the assistance they gave me.

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Testing the Properties and Characteristics of Chitin Thin Films

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Abstract and Introduction:

Chitin, the second-most abundant polysaccharide found in nature, has increased biocompatibility and biodegradability compared to cellulose, the most abundant polysaccharide. Found in crustaceans, cephalopods and mushrooms, chitin can be used to create new polymeric devices and to reinforce pre-existing technologies for various applications [1]. In this project, chitin nanofiber thin films were fabricated and characterized to determine their material properties. The fabrication process used the highly-volatile solvent 1,1,1,3,3,3-hexafluoro-2-propanol (HFIP) [2]. As the HFIP slowly evaporated, chitin nanofibers self-assembled through hydrogen bonding to form a thin film sheet. The thin films were tested and measured for material properties: Instron 4505 (upgraded to 5500R) and dynamic mechanical analyzer (DMA) for mechanical properties, x-ray diffraction (XRD) for composition, thermomechanical analysis (TMA) for thermal properties, and a Porosimeter for physical characteristics. These fabricated thin films provide an avenue to create potential applications in wound healing, tissue scaffolds, and polymer reinforcement.

Experimental Procedure:

Chitin thin films were prepared from 0.5% (w/v) chitin/HFIP solutions. The solution was drop-casted and promptly covered to slow the evaporation of HFIP. A few holes were made in the cover to insure the complete evaporation of HFIP. The solution was placed in a fume hood and allowed to evaporate for 8-10 days. When the thin film was set, the characterization process began. First, TMA was performed to determine the coefficient of thermal expansion (CTE). The change in length was measured as temperatures were cycled from 25°C to 180°C and back down to 25°C three times.

To test mechanical properties, an Instron and DMA were employed. Both tests involved a simple tensile test on the sample, closely following ASTM D882-10 [3]. Kapton HN 100 sheets from DuPont were used as a control for both experiments. The Instron applied a maximum force of 20 N with an extension rate of 0.1 mm/min. Using the DMA, we performed a "Static Stress Test."

After calibration, the DMA applied a load that went from 110 mN to 5000 mN at 100 mN/min.

An XRD helped us determine the formation of our chitin. The test was performed on the samples by scanning from 2θ at 3° to 55° with a 0.02 step-size following all necessary precautions while dealing with radiation equipment.

Lastly, a Porosimetry test was completed to determine the presence and characteristics of pores in the thin films. Multiple thin films, weighing a total of 0.0455 g, were loaded into the testing apparatus and mercury was intruded through the samples to determine the existence and size of the pores.

Results and Conclusions:

As previously noted, chitin self-assembles into nanofibers due to HFIP evaporation. This fabrication process helped yield 3 nm nanofibers in a thin film that ranges from 10 to 200 μm in thickness [2].

The CTE values from the TMA test ranged from about 38 to 186 ppm/K, but literature states that the values should be closer to 9.8 ppm/K [1]. This discrepancy can be attributed to nanofiber alignment in a two-dimensional plane while experimentation was performed in the third dimension.

The Instron and DMA tests provided results for Young's Modulus (stiffness) that did not entirely match literature results. Our control Kapton® and chitin film were specified to have a stiffness of 2.5 GPa [1, 4], but our Instron results gave an average stiffness of 1.187 GPa. Nonetheless, chitin thin films were tested on the Instron and the chitin showed an average stiffness of 1.09 GPa with a large standard deviation of 815 MPa as seen in Figure 1. To double-check, DMA tests were carried out in hopes for more accurate and precise results. DMA tests showed Kapton and chitin stiffness at about 732 MPa and 307 MPa, respectively. These disagreements in values can be a result of the testing methods, testing equipment, and inconsistent samples. Interestingly enough, if outliers of the Instron tests were taken into account, the two experiments showed that Kapton was about twice as stiff as chitin.

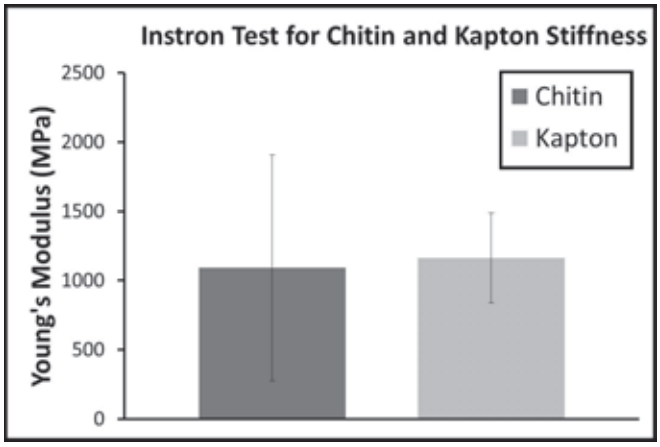

Figure 1: Kapton = 1.187 GPa with 325 MPa standard deviation. Chitin = 1.09 GPA with 815 MPa standard deviation.

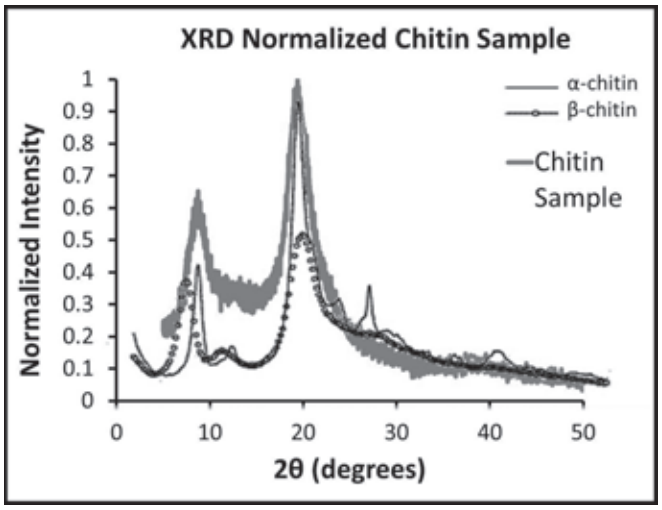

Figure 2: XRD of chitin thin film compared to α- and β-chitin.

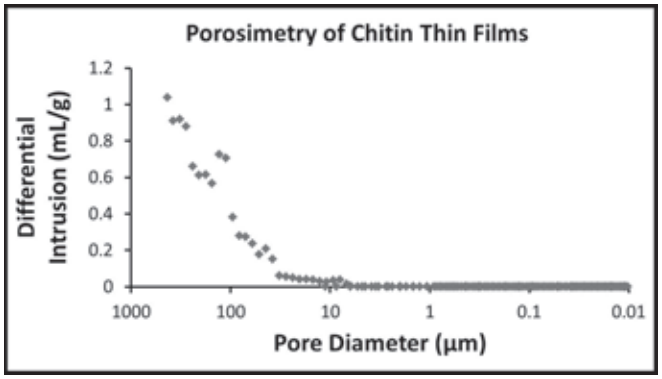

Figure 3: Porosimetry results of chitin thin film test.

XRD results, in Figure 2, were fairly conclusive in showing that our chitin thin films exhibited α-chitin (nanofibers are aligned parallel and antiparallel [5]). This orientation caused the nanofibers to pack closer together due to hydrogen bonding. This transformation of β-chitin in the chitin powder to α-chitin in the thin film was a result of the HFIP evaporation process.

The graph of the Porosimetry results, represented in Figure 3, shows spikes that occur at a higher pore diameter, a result of mercury filling the voids in between the different thin film samples. But with smaller pore diameters, the mercury could not penetrate through the thin films, meaning that if pores are present, they are smaller than 10 nm.

Future Work:

In the future, we will try to test our chitin thin films on equipment specifically designed for thin films testing. Hopefully, this will reveal better results for our stiffness values. Another aspect we would like to test is how the concentration of chitin/HFIP solution affects chitin thin film properties. Lastly, we will try to formulate sample preparation methods that yield consistent thin films.

Acknowledgements:

I acknowledge Professor Marco Rolandi, Dr. Jungho Jin, and the entire Rolandi Research Group for giving me an opportunity to help conduct this research and teaching me scientific research skills. I would also like to thank MSE User Facility and Nanotechnology User Facility personnel for their help and advice. Lastly, I wish to thank the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program and National Science Foundation for allowing me to participate in such an intellectual program.

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Temperature Dependent Electrical Resistivity of $La_xLu_{1-x}As$

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Abstract:

We report the temperature-dependent resistivity of lanthanum lutetium arsenide ($La_xLu_{1-x}As$) thin films grown by molecular beam epitaxy. Thicknesses of measured films were 30, 100 and 500 nm. Studies on the resistivity of $La_xLu_{1-x}As$ films suggest semimetallic behavior for temperatures ranging 78 to 295 K. Resistivity was measured using a cross sheet resistor van der Pauw (VDP) structure fabricated onto samples employing planar fabrication techniques. The linear fit of resistivity vs. temperature likely indicates electron-phonon scattering as the dominant mechanism, for temperatures from 78 to 295 K [1]. The increase in resistivity by increasing thickness was likely due to increasing interface roughness from imperfect growth at large thickness scales.

Introduction:

The discovery of graphene, a stable two-dimensional structure of carbon, has opened the door to the study of other thin films. Materials such as III/V and rare earth arsenides are suggested as "beyond graphene" materials. Investigation of electrical transport properties of rare-earth arsenides can lead towards a comprehensive understanding of carrier transport properties of these compounds and the development of novel electronic devices. To begin exploration of this, electrical properties of $La_xLu_{1-x}As$ (x = 47 and 48%) alloys were characterized as a function of thickness and temperature.

One of the most accurate methods for measuring sheet resistance of thin films is achievable by employing van der Pauw structures (Figure 1). The method is advantageous because it allows measurements to be taken of arbitrary lamellae by strategic placement of electrodes at the perimeter.

Experimental Procedure:

The sample stack was grown by molecular beam epitaxy (MBE). To account for impurities in the wafer left after heat treatment, 200 nm of gallium arsenide (GaAs) were grown onto a commercially available GaAs wafer. Ten monolayers (ML) of an LuAs spacer layer were grown next, followed by $La_xLu_{1-x}As$ and another 10 ML LuAs. The stack was capped

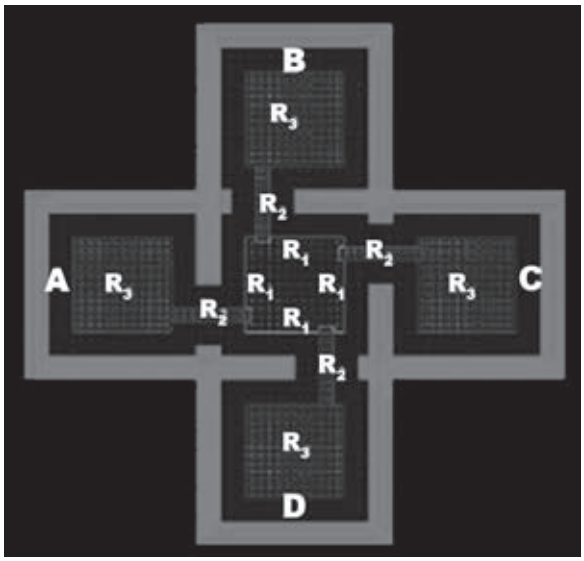

Figure 1: A van der Pauw structure where R_1 indicates resistance in the region of interest, R_2 the arm resistance, and R_3 the surface shunt resistance of the contact pad. Image courtesy S. Rahimi.

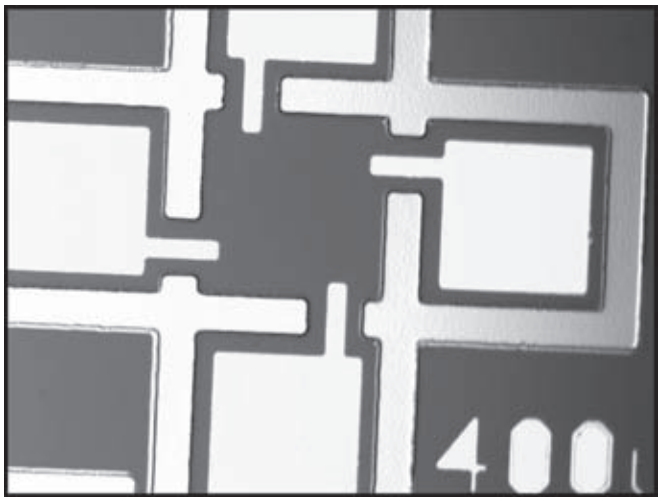

Figure 2: A fabricated VDP device.

by 15 nm GaAs to prevent oxidation of the alloy. Spacer layers separated LaLuAs from GaAs on both sides to prevent it from diffusing.

Fabrication of van der Pauw devices began by spin-coating cleaned samples with negative photoresist, AZ-5214. A Karl Süss MJB4 was used for lithography. Electrodes were deposited using electron beam evaporation (CHA SR-10 metal deposition tool), with a nickel adhesive layer and 41.1 nm gold. A lift-off process was required to form electrodes.

Following the second layer mask's lithography, devices were isolated by mesa-etching in a 1:1:20 solution of H_3PO_4:H_2O_2:H_2O. A fabricated device can be seen in Figure 2.

Low temperature measurements were taken using a Lakeshore cryogenic four probe system. The van der Pauw method was used [2, 3], requiring measurements be taken in two positions (see Figure 1). In the 0° degree position, current was run from pad A to B, and the voltage drop was measured between C and D. In the 90° position, current was run between pads D and A, and the voltage drop was measured between B and C. For both positions, measurements were first taken with a forward current (+I) and then with the reverse (-I). Using these four values, R_{00}' was calculated, according to the equation below. Similarly, R_{90}' was calculated.

$$R_{00}' = \frac{V_{CD}(+I) - V_{CD}(-I)}{I_{AB} - I_{BA}}$$

From the average of the two, sheet resistance was found from the VDP formula, below.

$$R_S = \frac{\pi}{\ln 2} R_{AVE} * f$$

A correctional factor, *f*, was used to correct for asymmetry in the structure. For this data, the correctional factor was 1.00, indicating high symmetry of devices.

Resistivity was calculated by multiplying the sheet resistance by thickness.

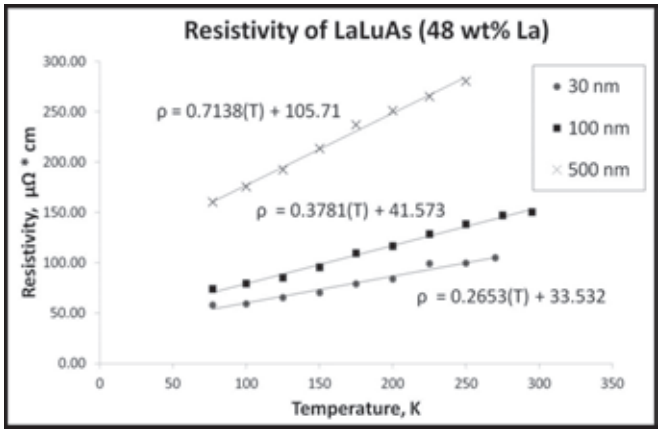

Figure 3: An analysis of data reveals increasing thickness corresponding with increasing resistivity.

The alloys exhibited semi-metallic behavior, increasing in resistivity with increasing temperature (Figure 3). The plots of resistivity vs. temperature and sheet resistance vs. temperature were linear. For this temperature range, 78 to 295 K, the linear fit likely indicates electron-phonon scattering as the dominant scattering mechanism [1]. The difference in resistivity between 30 and 500 nm samples averaged 193% and between 30 and 100 averaged 26%, with the 30 nm sample showing lower resistivity in both cases.

Conclusions:

The increase in resistivity with thickness was independent of temperature, suggesting impurities as an underlying cause. The trend likely also results from differing surface roughness. As thicker layers are grown by the MBE method, surface roughness between interfaces tends to increase [4].

Future Work:

Based on these results, as well as data showing temperature dependent resistivity of 3 nm $La_xLu_{1-x}As$, a paper will be drafted describing electrical transition properties of rare earth arsenides. This paper, "Temperature dependent electrical resistivity and resistivity tuning of LuAs thin films by Lanthanum" (coauthors S. Rahimi, E.M. Krivoy, J. Lee, M.E. Michael, S.R. Bank, D. Akinwande), will be submitted to Applied Physics Letters.

Acknowledgements:

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Photovoltaic Devices Fabricated with CIGS Nanocrystal Inks

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Introduction:

Photovoltaic devices (PVs), which convert sunlight into electricity directly, are a promising energy source because they are renewable and clean. To be widely used, they need high power conversion efficiency (PCE) and low cost. Spray-deposited [1] thin-film $CuIn_{1-x}Ga_xSe_2$ (CIGS) PVs have the potential to achieve this goal.

In this approach, a CIGS layer was deposited as an ink and then thermally annealed under selenium atmosphere—a process called selenization—to achieve high efficiency. The quality of the annealed CIGS nanocrystal film was highly dependent on the selenization conditions. We investigated various parameters related to selenization to improve power conversion efficiency (PCE).

Sel #	Pre-Se. Anneal	Mo Bake	NaCl Bath	PCE [%]	V_{oc} [V]	J_{sc} [mA/cm²]	*FF*
359	No	No	No	0.071	0.221	-1.163	0.276
360	No	No	Yes	0.096	0.163	-2.287	0.257
361	No	Yes	No	0.230	0.395	-2.088	0.279
362	No	Yes	Yes	0.243	0.334	-2.607	0.279
363	Yes	No	No	1.485	0.477	-10.460	0.298
364	Yes	No	Yes	1.006	0.478	-7.746	0.272
365	Yes	Yes	No	2.760	0.474	-20.075	0.290
366	Yes	Yes	Yes	1.832	0.410	-11.839	0.378

Figure 1: Measurement results of Mo baked, pre-selenization annealed, or NaCl bath soaked samples.

Fabrication Process:

Solar cells were fabricated on soda-lime glass with a layered molybdenum (Mo) / CIGS / cadmium sulfide (CdS) / zinc oxide (ZnO) / indium tin oxide (ITO) structure. One micrometer (μm) of Mo was sputter deposited on soda-lime glass (Delta Technologies), followed by spray deposition of approximately 1 μm of CIGS nanocrystals. The nanocrystal film was annealed in argon (Ar) for one hour between 475°C and 525°C. The substrate was then inserted into a graphite box and annealed under selenium atmosphere at 500°C for ten minutes. CdS was then deposited by chemical bath. A window layer of 50 nm of ZnO and 600 nm of ITO were sputtered to complete the device.

Experiments:

Various pre-selenization treatments of the CIGS nanocrystal films were studied. Devices were annealed in Ar before CIGS deposition (Mo bake), after CIGS deposition (pre-selenization anneal), or soaked in a sodium chloride (NaCl) bath [2]. The Mo bake consisted of annealing a back contact in an argon atmosphere at 475°C for one hour just after Mo deposition. The pre-selenization anneal was carried out at 475°C in Ar for one hour immediately after depositing the CIGS layer.

It is known that sodium plays a role in CIGS crystallization [2] and during these anneals sodium diffuses from the soda-lime to the Mo/CIGS interface. Sodium was also added directly to the CIGS film by soaking the CIGS-coated substrate in a 1 g/L aqueous NaCl bath of for 15 minutes before selenization.

Figure 1 shows the measurement results of samples with these pre-selenization treatments. All photovoltaic device measurements were performed under Air Mass 1.5 illumination. V_{OC} is open circuit voltage and J_{SC} is short circuit current density. *FF* is a fill factor—the ratio of the product of voltage and current at maximum power and the product of V_{OC} and J_{SC}. The Mo bake and pre-selenization anneal both exhibited a positive effect on improving PCE.

The effect of the temperature ramp rate during selenization was also studied. Films were selenized for ten minutes after ramping the temperature at 20, 50, 80 and 110°C/min to 500°C. The nanocrystal films were treated prior to selenization by annealing at 475°C and soaking the films in a NaCl bath.

Device PCEs were 0.008% for 20°C/min, 0.034% for 50°C/min, 0.230% for 80°C/min and 0.251% for 110°C/min. Higher ramp rates produced higher PCE. Scanning electron

microscope (SEM) images (Figures 2 and 3) show that the crystalline domains in the selenized CIGS films were larger when ramped at 110°C/min compared to 20°C/min. Films with larger crystalline grains are expected to have decreased recombination of electrons and holes for improved PCE. In addition, the thickness of the molybdenum selenide ($MoSe_2$) layer, generated by converting Mo to $MoSe_2$ during selenization, of 20°C/min was 664 nm, while that of 110°C/min was 373 nm. A thin $MoSe_2$ layer was better, as thicker $MoSe_2$ layers increased the series resistance in the device and degraded PCE.

Next, we investigated different CIGS layer deposition processes. Two processes were used where Process 1 was the conventional method and Process 2 was a new proprietary one. Pre-selenization and NaCl bath were performed in both of Process 1 and 2.

Figure 4 shows the I-V curve of the device fabricated with Process 2. The PCE of Process 2 was 6.564%, while that of Process 1 was 0.191%. Process 2 also improved *FF—FF* of Process 2 was 50.6%, while that of Process 1 was 30.1%. These results were supposed to be caused by the high quality of the CIGS layer fabricated with Process 2.

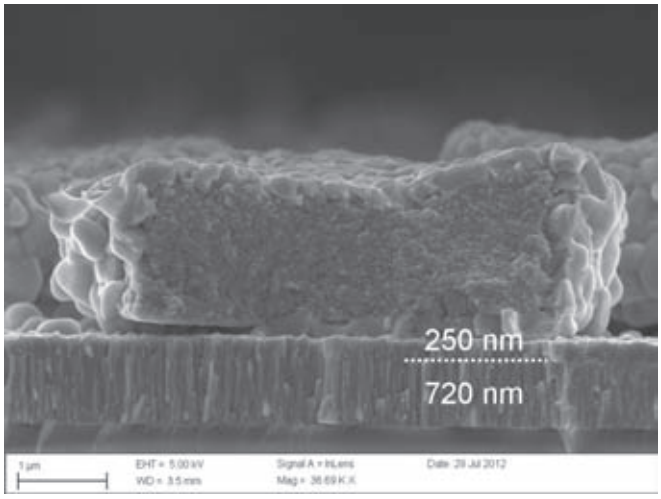

Figure 2: Cross section SEM image of 20°C/min ramp rate sample.

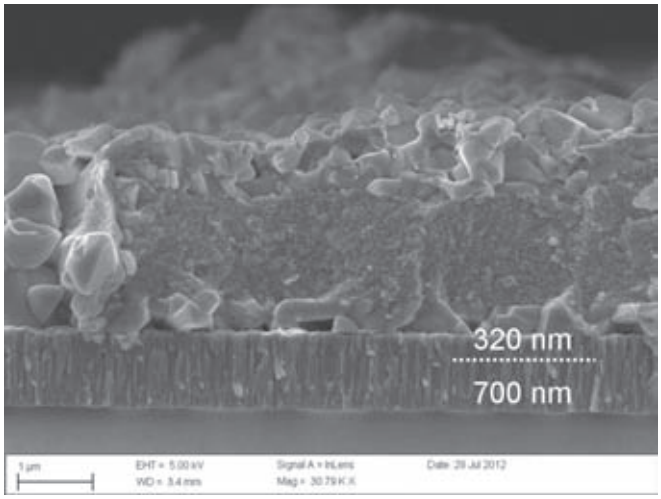

Figure 3: Cross section SEM image of 110°C/min ramp rate sample.

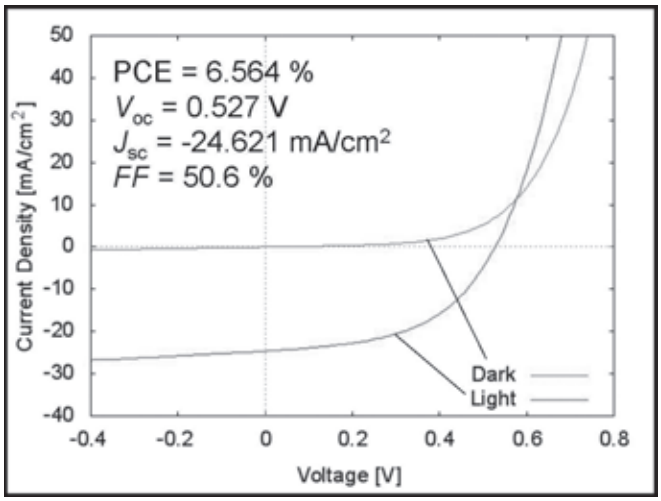

Figure 4: I-V curve of sample fabricated with new proprietary process.

Conclusions:

Spray-deposited CIGS nanocrystal films were selenized to increase PV device efficiency. Various processing parameters were studied. Pre-selenization anneal, molybdenum bake, higher heating ramp rate and new CIGS layer deposition process yielded substantial improvements in device efficiency.

Acknowledgments:

This is an achievement of the National Nanotechnology Infrastructure Network International Research Experience for Graduates Program funded by the National Science Foundation. My principal investigator was Dr. Brian A. Korgel and my mentor was Mr. Taylor Harvey, both of whom belong to the Department of Chemical Engineering, the University of Texas at Austin. Ms. Marylene Palard, Ms. Jean L. Toll, and Ms. Christine P. Wood helped me a lot during this program. My attendance at this program was also supported by the National Institute for Materials Science (NIMS) in Japan. Dr. Keijiro Hirahara and Ms. Noriko Ito, who belong to NIMS, also helped me a lot. I am from Shibata Mita Laboratory, Department of Electrical Engineering and Information Systems, Graduate School of Engineering, the University of Tokyo. I thank all of these organizations and people.

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Substrate Conformal Imprint Lithography

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Abstract:

Substrate conformal imprint lithography (SCIL) is capable of high resolution and is less sensitive to defects inherent in traditional nanoimprints. This makes SCIL promising for both research and industrial applications. We report here progress toward imprinting dense features at 15 nm critical dimensions (CDs). The study includes an improved process employing ZEP resist to minimize line edge roughness (LER) on the master wafer mold down to 2-3 nm. Imprinted features on initial trials were found to exhibit a negative linewidth change on the order of tens of nanometers. The SCIL process employs a wave generation process making localized and global distortions possible from stretching the flexible PDMS-on-glass stamp. To characterize this, we created a second SCIL mask and printed wafers for pattern placement accuracy tests over the entire area of imprinted wafers.

Introduction:

Moore's law predicted that the number of transistors on a chip should double roughly every two years, due, in part, to ever smaller dimensions. However, photolithography, the technique most commonly used today, is nearing the resolution limit imposed by the wavelength of light. One common method for patterning features smaller than photolithography can achieve is electron beam lithography, but this is prohibitively expensive and unfit for use in manufacturing because of the time required. Patterns made using electron beam lithography can, however, be replicated using NanoImprint lithography (NIL), at a fraction of the cost. NIL is a stamping process used to transfer features from a previously patterned master wafer into imprint resist on daughter wafers, which can then be cured. However, NIL faces its own challenges—the high pressures used and repeated exposure to resist can wear down features on the master wafer over time. Additionally, because the stamps used are inflexible, any particulates on them can result in unpatterned regions and can damage the master.

Substrate conformal imprint lithography (SCIL) [1] is a new variant of nanoimprint lithography using a flexible polydimethylsiloxane (PDMS) replica of the master wafer, making it possible to pattern over particulates. Also, because the master wafer is only used as a mold, it is better protected, which reduces the cost of repeatedly patterning new masters. However, because the stamp is flexible, it may induce distortion either of the printed features or in their placement on the wafer. We wanted to characterize that distortion and test SCIL's resolution limits to see whether it would be a good candidate for manufacturing at the nanoscale.

Methods:

In the SCIL process, PDMS stamps are molded from features etched into silicon master wafers. These stamps are then imprinted into a resist on daughter wafers, which are then UV cured. When the stamp is peeled away, the features are left behind in the resist on the daughter wafers.

To create the master templates, we used photolithography or electron beam lithography to pattern wafers which we etched using a reactive ion etcher. After removing any remaining resist, we added a monolayer of perfluorooctyltrichlorosilane (FOTS), a highly fluorinated molecule, as an anti-stick coating. We applied a layer of custom PDMS to the thin glass stamp and cured it to use as a SCIL mask. We imprinted these into wafers coated with Amonil (AMO, GmbH) resist using a modified Suss MA6 contact aligner. This tool allowed us to precisely control the imprint force and separation between the stamp and the imprint resist.

The first stamps we tested were made using an ASML 5500/300C deep ultraviolet stepper to pattern the master. This stamp was used to confirm that SCIL was capable of reproducing fine features over a large area as well as to troubleshoot any initial problems.

Tests of SCIL's resolution limit, however, required a master wafer with extremely small features. Towards this end, we created a dense pattern of 15 nm lines using electron beam lithography using ZEP520 (Zeon Chemical) as a resist. To achieve these challenging results, we used a combination of feature size biasing, dose biasing, and shot pitch modulation.

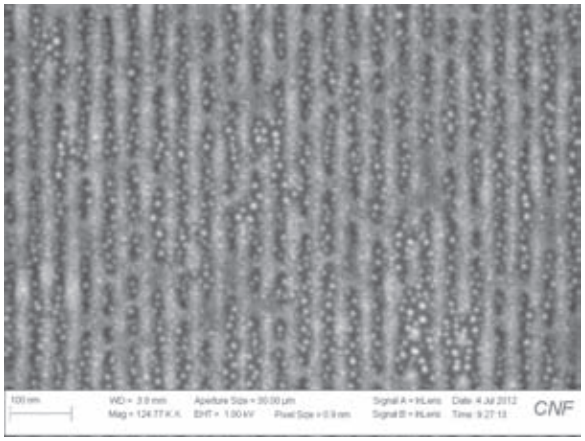

Figure 1: Early attempt to fabricate 20 nm trenches in ZEP520 resist before feature size biasing or cold development temperatures were used.

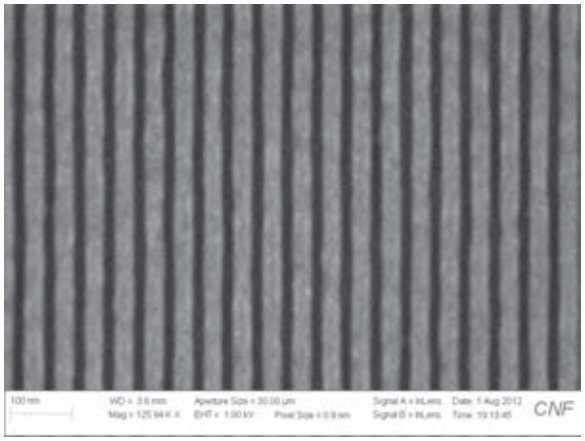

Figure 2: 15 nm trenches in 30 nm thick ZEP520 resist for patterning the master wafer needed for the SCIL resolution tests.

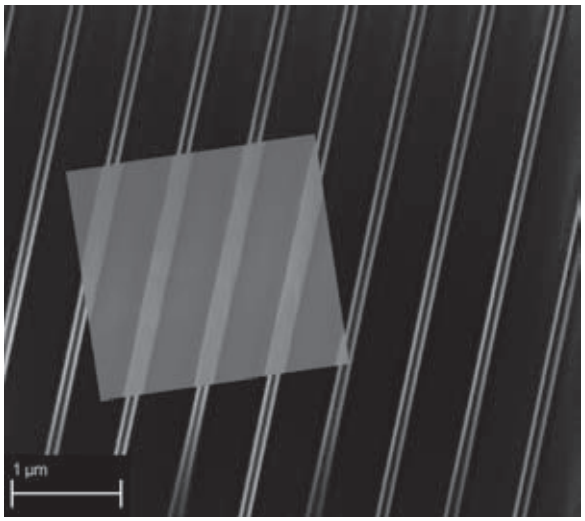

Figure 3: SCIL imprint and master wafer (inset) illustrating size changes in SCIL.

We also tested different development chemicals, temperatures, and times to optimize feature size and minimize LER. We also employed proximity error correction to compensate for the effect of backscattered electrons on the dosage [2].

The result was a silicon master wafer ideally suited to these resolution tests (Figures 1 and 2).

Finally, in order to characterize distortion in the pattern across the entirety of the wafer, we imprinted a stamp with an array of large crosses, 60 μm tall, onto a 6-inch wafer. Use of this stamp will indicate how accurately the stamp places these crosses across the wafer by comparing cross positions with the original master. The measurement will be made using the metrology capability of the JBX6300FS electron beam lithography system, which uses a laser interferometer to calibrate its stage position.

Results and Conclusions:

Using the stamp made with deep UV lithography, we initially confirmed that SCIL is capable of patterning submicron features over a broad area. We fabricated a stamp with crosses for the pattern placement accuracy tests, which we successfully imprinted. This awaits metrology measurements. To evaluate the resolution limits of SCIL, we optimized the process used to produce the master wafer. This process used cold xylenes as a developer and incorporated CAD corrections including proximity error correction and feature size biasing to improve resolution and LER. A master wafer with dense patterns of lines down to 15 nm was fabricated. Preliminary imprints with a similar mask demonstrate an overall decrease in linewidth of 80 nm from 170 nm lines as they were measured on the original master wafer (Figure 3). The source of this "shrinkage" has yet to be investigated.

Data from these pattern placement accuracy tests and resolution tests will make it possible to further improve the SCIL process in the future and to determine suitable applications for it as a manufacturing method.

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Engineered Metallic Structures and Nanofabrication Techniques for Plasmonic Biosensors

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Abstract:

Optical energy can be harnessed on the nanoscale by exploiting plasmonic resonances in metallic nanostructures. These resonances are the result of the unique optical properties of metals and their abundance of conduction electrons. Utilizing these properties, it is possible to engineer metallic nano-devices that operate with large electric field intensities confined in and around the structure. Due to these large fields, optical, chemical and spectroscopic properties can be probed with high sensitivity. This project covers the various fabrication methods unique to the precise fabrication of metallic nano-structures as well as some applications as nano-optical sensors.

Introduction:

Plasmons are collective oscillations in the electron cloud density of a conductor, usually metal. At the surface of a material, they are called surface plasmons. These oscillations can be induced by electromagnetic radiation at specific frequencies. If certain conditions are met, a photon can couple with a plasmon forming a surface plasmon polariton (SPP). This is a propagating electromagnetic wave on the surface of the metal at the interface of a dielectric and the conductor. The SPP is transverse-magnetic, meaning that an evanescent electric field extends into both the metal and dielectric, normal to the interface. This electric field extends no more than a few hundred nanometers (nm) into the dielectric and is strongest near the surface. We are able to use this electric field to probe the near-field region [1]. If a plasmon is induced on a small metal particle, i.e. with size dimensions on the order of or less than the wavelength of incident light, a propagating electromagnetic wave is not formed. Instead, electrons oscillate with the changing electric field, forming areas of high electric field, or "hot-spots" [1]. This is known as localized surface plasmon resonance (LSPR). These hot-spots can be employed to trap particles and perform surface enhanced Raman spectroscopy (SERS) [2].

We can engineer structures on the nanoscale that exhibit these plasmonic properties. However, because plasmons can be excited by deformities on the surface, it is critically important that our devices have smooth surfaces to ensure optimal performance.

Fabrication Procedures:

Because smooth surfaces were so important for our devices, we platformed the entire fabrication process around the technique of template-stripping. This process required a silicon mold, which was then deposited over with metal. The metal was then epoxied to a glass slide, cured, and finally removed from the mold; this resulted in the inverse of the mold patterned in the metal, possessing ultrasmooth surfaces. Template stripping also allowed the mold to be reused, enabling high-throughput fabrication of devices [2]. We used two different methods to fabricate the molds.

For high resolution patterning, we employed electron beam lithography. After patterning a spin-coat layer of photoresist, we used etch processes to carve the mold. Depending on the etch depth needed, sometimes a hardmask layer was utilized. For lower resolution patterning, we used focused ion beam lithography. This method did not require photoresist, however it could not match the resolution capabilities of electron beam lithography. This method did enable the direct fabrication of molds.

In some cases, we determined that we did not need to template-strip our structures. In these situations, we used electron beam or photolithography to pattern a stencil mask. We then deposited metal over the mask and performed a chemical liftoff. All open areas of the stencil were filled in with metal, resulting in surfaced patterned structures.

Devices:

Using the methods described above, we fabricated an assortment of devices, some of which are not contained within this report. The following figures show several devices in various stages of production.

Bowtie Array (Figure 1). These bowties were fabricated by depositing gold over a stencil mask and performing liftoff. They facilitated the formation of LSPRs, with hot-spots focused in the gap at the center of the bowtie. They have been used to trap particles in this hot spot and to aid in performing SERS.

Sharptips Prior to Template Stripping (Figure 2). Using electron beam lithography, dry etching, atomic layer deposition, and thermal metal evaporation, an array of sharp-tipped lines were fabricated. When template stripped, they focused to a narrow point. These devices displayed interesting plasmonic effects and concentrated hot spots at the tips of the structures. (*Image courtesy of Timothy W. Johnson.*)

Nanochannels, HSQ on Silicon (Figure 3). Using electron beam lithography, it was possible to achieve high resolutions, as exemplified here. These were 20 nm lines of HSQ on silicon. After development, HSQ becomes chemically similar to SiO_2 and can be used as a hardmask for etching. This image was taken prior to etching.

Future Work:

The main thrust of this research was designing and building plasmonic biosensors.

As demonstrated, devices are in various stages of completion. The obvious next steps include finishing fabrication and testing the devices. Based on test results, the devices can be optimized and results published.

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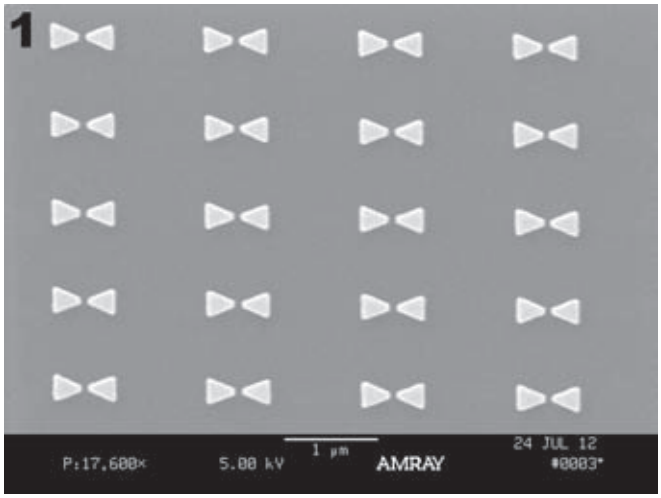

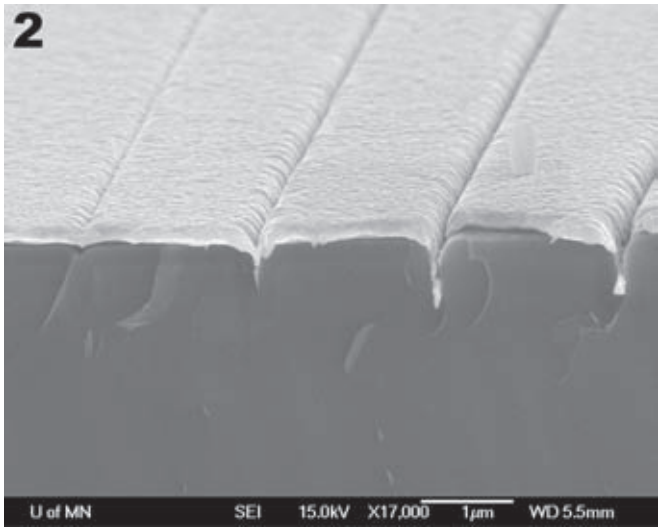

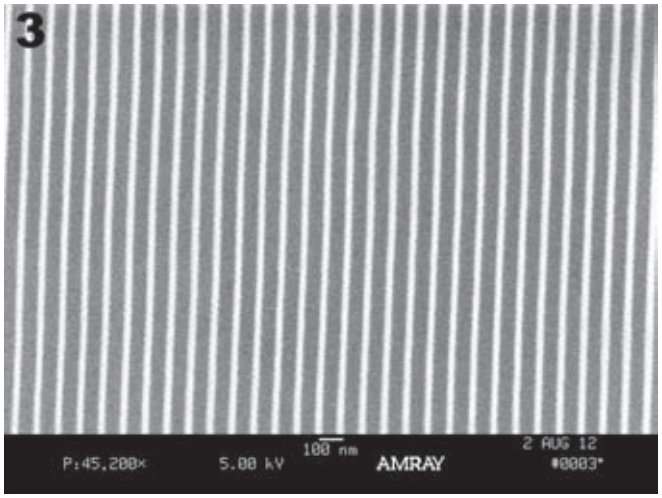

Atomic Layer Deposition Process Optimization and Characterization of Amorphous Metal-Oxide Films

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Abstract:

Atomic layer deposition (ALD) is used to create conformal thin films that have many applications due to the wide range of available materials and precisely-controlled thicknesses. Amorphous metal-oxide thin films are good candidate materials for dielectric gates, diffusion barriers and biocompatible coatings, among many other applications. ALD processes that have not been fully optimized and characterized result in wasted precursor, longer fabrication times and incomplete understandings of the films themselves. In this work, the processes for hafnium dioxide (HfO_2) and zirconium dioxide (ZrO_2) films were optimized for uniformity by varying precursor pulse and carrier gas purge times to create the most uniform films. The temperature dependence of film characteristics and differences between thermal and plasma-enhanced processes was explored for titanium dioxide (TiO_2) films. Uniformity was determined by comparing thicknesses measured by an ellipsometer at different positions in the reaction chamber. This project yielded ALD metal-oxide processes optimized for uniformity and a better understanding of film characteristics. All data is available on the Stanford Nanofabrication Facility's website.

Introduction:

ALD is a nanofabrication process consisting of a cyclic self-limiting chemical reaction with vapor-phase precursors, but only surface-phase reactions. A cycle of ALD consists of four steps; 1) surface saturation by precursor A, 2) purge of excess precursor A from the reaction chamber, 3) surface saturation by precursor B, and 4) purge of excess precursor B. For metal-oxide films, precursor A is the base metal with ligands attached and precursor B is water (for thermal processes) or oxygen plasma (for plasma processes). Steps 1 and 3 are quantified by the "pulse time," which is how long the valve on the cylinder containing the precursor stays open and is thus related to the amount of precursor in the reaction chamber. Steps 2 and 4 are quantified by the "purge time," which is how long the background carrier gas (Ar or N_2) flows through the reaction chamber without carrying any new precursor.

We sought to maximize film uniformity, minimize precursor waste, and minimize process runtime by varying only Steps 1 and 2. Thus, "pulse time" and "purge time" specifically refer to the precursor A pulse time and the purge time immediately after that, respectively. Other parameters varied were temperature, background carrier gas flow rate, type of deposition tool and water or oxygen plasma as precursor B. We also determined deposition rates.

Experimental Procedure:

Depositions were performed on two simultaneously-run 4-inch silicon wafers (placed side-by-side in the reaction chamber) after a standard RCA clean. The film thickness was measured at nine points per wafer, resulting in 18 thicknesses per deposition. These were used to compute the average thickness and non-uniformity, which was the standard deviation divided by the average thickness. We ran 100 cycles of ALD for all depositions (except those used to determine the deposition rate) on one of two Cambridge Nanotech ALD systems: Fiji or Savannah.

Results and Conclusions:

The ZrO_2 processes on both the Savannah and Fiji systems were wasting precursor A. We were able to determine the threshold for surface saturation by decreasing the pulse time for the Savannah process. A lack of surface saturation was indicated by a significant decrease in average thickness (Figure 1) as well as high non-uniformity. The standard recipe was adjusted from having a pulse time of 0.40s to 0.15s, saving a significant amount of precursor A. Increasing the purge time decreased the non-uniformity of the film (Figure 2), indicating that vapor-phase reactions took place at shorter purge times. This was also why the Fiji process had a non-uniformity of over 10% until the purge time was increased from 20s to 50s.

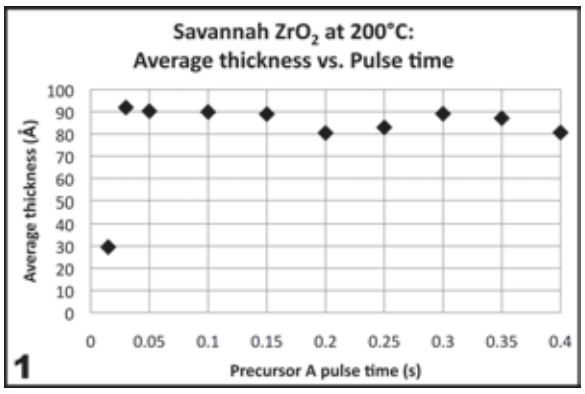

Figure 1: The thickness dropped off at a pulse time of 0.015s. The pulse time must be at least 0.03s to reach surface saturation.

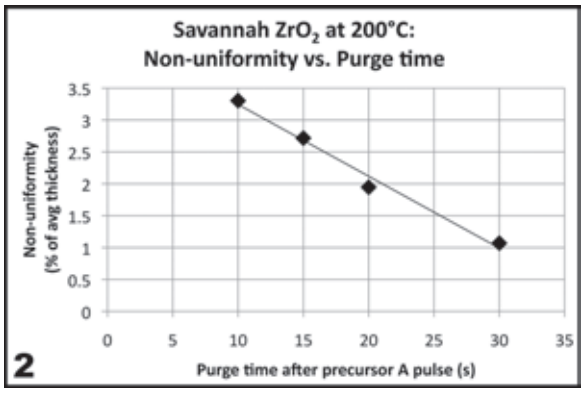

Figure 2: The non-uniformity of the film decreased as the purge time increased, indicating vapor-phase reactions occurred at shorter purge times.

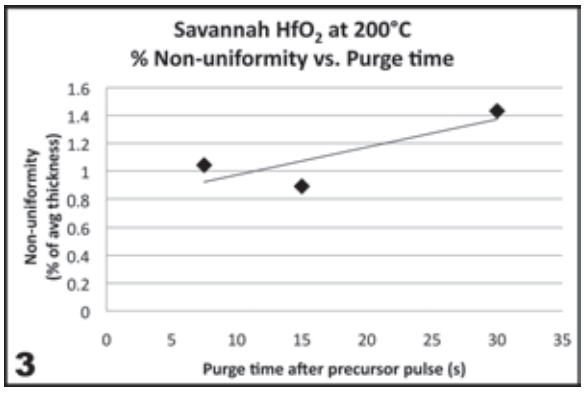

Figure 3: The non-uniformity of the film increased as the purge time increased, indicating desorption occurred at longer purge times.

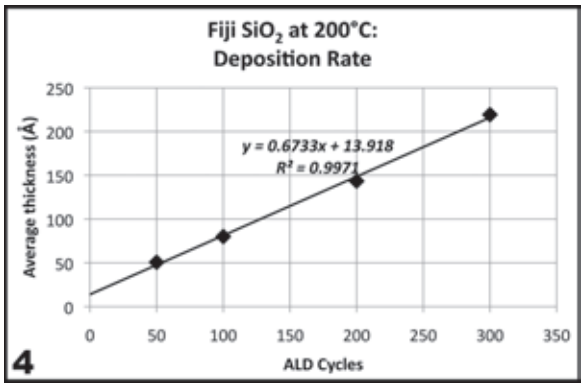

Figure 4: The Fiji SiO_2 deposition rate is 0.7Å/cycle.

The Savannah HfO_2 process was verified to be at optimal performance. Pulse time, purge time and background flow were varied to confirm that the standard recipe had the highest uniformity. However, it was found that desorption of precursor A occurred at longer purge times (Figure 3) due to excessive volatility. Despite this trend, the initial purge time of 15s had the lowest uniformity, indicating that it was a good balance between desorption and potential vapor-phase reactions.

The deposition rate of Fiji SiO_2 was 0.7Å/cycle with 14Å of native oxide (Figure 4), which is due to oxygen diffusing into the substrate at room temperature before deposition. The deposition rate of Savannah ZrO_2 was 0.8Å/cycle with 11Å of native oxide.

Thermal and plasma Fiji TiO_2 films were deposited at 100-300°C. The plasma films showed little change in average thickness over the temperature range. The thermal films were thicker at lower temperatures due to precursor condensation.

Future Work:

The Fiji ZrO_2 process should be further optimized to increase uniformity and reduce precursor waste. More process optimization should be done on the plasma Fiji TiO_2 process because most films had twice the non-uniformity of those from the thermal process for the explored temperature range. The Fiji TiO_2 deposition rate should also be determined. Capacitors can be made with the films to determine the electrical properties such as breakdown voltage and capacitance with respect to both high and low sweeping voltages. These properties could then be compared for films deposited at different temperatures, by different tools or through different processes (thermal vs. plasma).

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