Nanoscale High-Speed Transparent Electronics using E-Beam Patterning of Zinc Tin Oxide Thin Film Transistors

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Introduction:

Zinc tin oxide semiconductors can be used to produce transparent thin film transistors. These transistors are needed for many new applications in heads up displays and invisible microsystems. The focus of this project was to miniaturize the gate length of zinc oxide-based transistors to below 100 nanometers and characterize the performance of these transistors as a function of their gate length. As the gate length of a transistor is reduced the drive current increases, thus increasing circuit speed and performance [1].

Here, we used electron beam (e-beam) lithography to fabricate narrow gate length zinc tin oxide transistors. A beam of electrons bombards a layer of resist, creating the desired patterns. Since the size of the beam is very narrow we are able to fabricate very small features. However, when using e-beam patterning to create sub 100-nm geometries, we must take into account the proximity effect. The proximity effect involves the back-scattering of electrons once they penetrate the resist and substrate and interact with other atoms. Back-scattering of electrons causes further exposure and enlargement of the desired pattern [2].

Experimental Procedure:

First, we characterized the e-beam exposure and lift off of molybdenum (Mo) and titanium (Ti) electrodes with narrow gaps using poly(methyl methacrylate) — PMMA — resist on glass (Corning Eagle XG). Pairs of electrodes had designed gaps ranging from 10 μm to 40 nm. We exposed these structures with dosages of 600, 700, 800, 900, and 1000 microCoulombs/cm^2 using the JEOL 6300FS Electron Beam Lithography System. Lift off was then performed and the electrodes were inspected by scanning electron microscope (SEM) and electrically tested to determine whether the gap was open (as intended) or electrically shorted (indicating incomplete patterning or lift off).

The detailed process is as follows. We spun a 10 nm thick layer of PMMA A2% and soft baked for three minutes at 180°C. A 200 nm layer of e-spacer was spun on top of the resist and soft baked at 110°C for two minutes. E-spacer is a conductive polymer needed to ground the glass substrate and prevent electron deflection when using the e-beam. After e-beam lithography, the sample was dipped in distilled water for 45 seconds to strip the e-spacer, the PMMA resist was developed in 1:3 methyl isobutyl ketone : isopropyl alcohol for 30 seconds, and the sample was rinsed in isopropyl alcohol for 30 seconds. Finally, 40 nm of source/drain metal was deposited. For liftoff, the samples were left in a room-temperature acetone bath overnight, following which the bath is heated at 60°C for 1.5 hours with moderate sonication.

Once the narrow-gap electrode process was complete, we used photolithography to pattern the larger source/drain structures needed for electrical testing. E-beam lithography is a serial write process and would require a massive amount of time to write these structures. We used SPR 1813 resist and exposed using an MA/BA6 contact aligner tool. We developed the resist in MF 319; 100 nm of the secondary source/drain material was then deposited and lifted off in acetone. The electrodes were characterized using a SEM and current-voltage (I-V) measurements were taken using an Alessi probe station and HP 4155A semiconductor parameter analyzer.

For transistor processing, the samples additionally contained patterned gate metal, insulator, and patterned semiconductor layers which were prepared before the source/drain metal was deposited.

Results and Conclusions:

Figure 1 plots the measured gap between e-beam patterned electrodes as a function of the designed gap width and the e-beam dose. Gaps larger than 100 nm were not significantly affected by the differences in dosage. Using evaporated Ti, we consistently obtained separated electrodes for gaps of 40 nm and above. The electrode separation was verified by electrical testing, which indicated a very high resistance of greater than 5×10^8 Ohms, as seen in Figure 2. Electrodes with gaps down to 20 nm were fabricated using Ti (Figure 3), although their yield was not consistent. In contrast, sputtered Mo had difficulty lifting off for electrode gaps of < 500 nm. We then fabricated working transistors using photolithography to determine the effectiveness of a new separated gate and gate insulator process. Figure 4 shows electrical data for a transistor with a channel width of 100 μm and a channel length of 6 μm. The low off current and gate current, as well as the large on current indicate that the transistor is working properly.

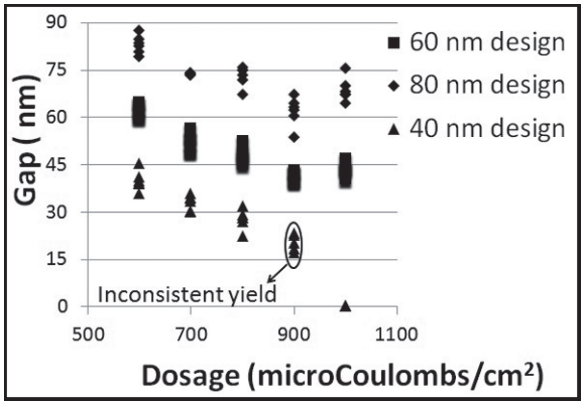

Figure 1: Electrode gap as a function of electron beam dose.

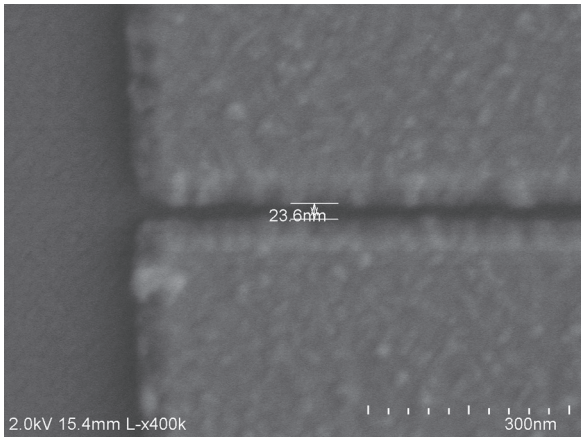

Figure 3: Open gap between 40 nm designed titanium electrodes.

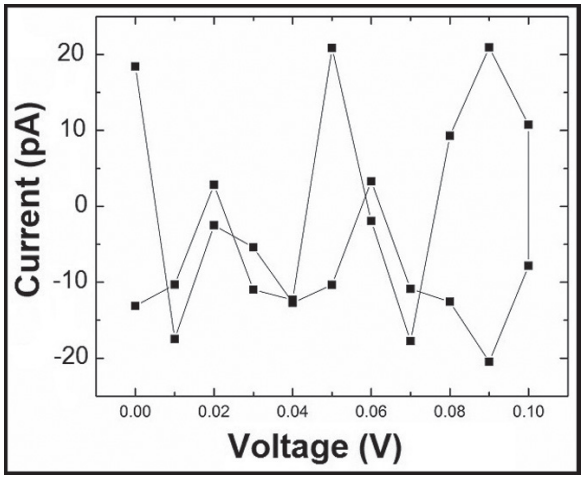

Figure 2: I-V measurement of 40 nm designed titanium electrode, indicating an open gap.

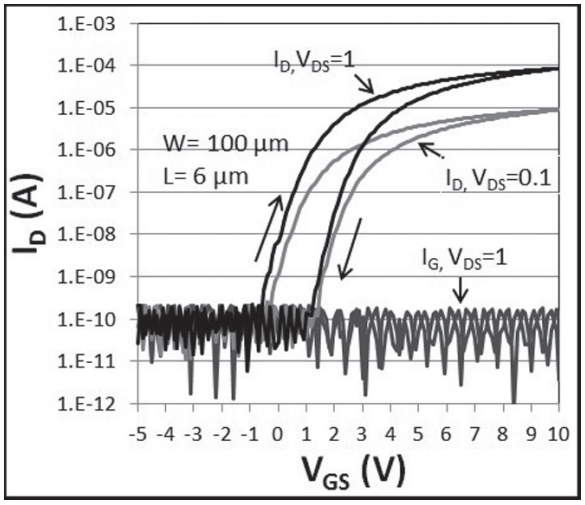

Figure 4: Electrical characteristics of photolithographically-defined transistor.

In conclusion, we were able to use e-beam lithography on transparent glass substrates to fabricate electrodes with sub 100-nm gaps. Since we were using a non-conductive substrate, a conductive polymer layer was needed to disperse charge build up. Evaporated titanium electrodes with gaps of 40 nm and above and sputtered molybdenum electrodes with gaps of 500 nm and above were consistently produced. We believe the conformality of sputtering causes difficulty for molybdenum lift off. We also were able to produce working transistors using a new separated gate and gate insulator process.

Future Work:

With successful transistors produced using photolithography, the next step is to integrate the narrow gap electrodes made using e-beam lithography into the new gate and gate insulator process to form transistors with sub-100 nm gate lengths, and then characterize their performance.

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