Polymer Process Optimization for Electrical and Optical I/O Interconnect Pillar Fabrication

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Abstract:

Polynorbornene polymers have long been considered desirable materials for electrical and optical interconnects due to their low dielectric constants, high indices of refraction, low elastic moduli, and photodefinability.

In recent developments, polymer pillars have been coupled with metallic conductors to transmit electrical and optical signals. These more complicated structures require precisely constructed features. For optical interconnects, the sidewalls of the pillars should be smooth to reduce scattering and subsequent optical losses. For electrical applications, interior cavities should be cleanly developed down to the underlying surface to ensure reliable electrical contacts. Choosing an appropriate polymer formula is essential to obtain these results. Each formula yields different results in fabrication, so preliminary tests are necessary to determine the optimal material for each application.

Three different formulas of the polynorbornene polymer Avatrel were tested under different exposure doses, post exposure bake temperatures, and durations. The formula that developed best overall with respect to structural perpendicularity, smoothness, depth of interior development, and top surface flatness was then further tested in fabrication applications. Through these fabrication processes, it was shown that the chosen formula can be used to create smooth 130 μm tall polymer pillars for optical uses and copper-core polymer pillars for solid electrical interconnection between a chip and a board.

Introduction:

Norbornene-based polymers make good electrical and optical input-output interconnects due to their innate structural properties. This type of polymer has a low dielectric constant to limit crosstalk, high index of refraction for optical signal conduction [1], low elastic modulus to compensate for thermal expansion coefficient mismatch between board and die [2], and the material is photodefinable for ease of fabrication.

An effective electrical-optical interconnect should have a cleanly developed interior to allow for solid electrical connection and smooth exterior surfaces to reduce optical losses. Such development characteristics vary among different polymer formulas. For best results, polymer formulas should undergo preliminary testing to determine which formula is best for which application. Here high aspect ratio polymer pillar-like structures are used to provide a physical optical path or waveguide between the chip and the board, while metal-core polymer pillar-like structures are used to provide electrical interconnection.

Materials and Methods:

The experiment described here tested the structural development of three polymer formulas. Polymer pillar processing began with a 36 μm film of polymer spun onto the wafer. The samples then underwent a 10 minute soft bake on a 100°C hotplate. Wafers were cleaved into standardized rectangles for better mask contact. Subsequent UV exposure doses were 150 or 350mJ/cm^2. The post exposure bake condition was also subject to variable temperature (95°C or 105°C) and duration (10 or 20 minutes). Finally, development occurred in a beaker of limonene floating in an ultrasonic developer for a duration of 90 seconds for all samples, followed by a 30 second immersion bath in isopropyl alcohol. A reduced factorial experimental design governed the conditions of each trial.

In order to obtain photographs of the samples on a scanning electron microscope (SEM), the samples had to be diced into one by two centimeter rectangles, mounted perpendicularly, and coated with gold. It was desirable that cleavage planes bisect structures with interior cavities for the purpose of demonstrating the depth and clarity of development.

To determine whether pillar-type waveguides are possible with that material, 130 μm pillars were fabricated and evaluated using SEM imaging. To achieve a 130 μm film, a 50 μm layer was spun and soft baked for 8 minutes before another layer was spun at the same speed. The wafer was then soft baked for 45 minutes.

Copper-filled coaxial pillars were also fabricated. A silicon wafer was layered with first copper, then silicon dioxide. Using photoresist, the silicon dioxide was etched away to leave exposed circles of copper. Polymer was spun onto the wafer and patterned to form hollow-core pillars centered above the copper circles. A copper core was then grown from these circles using electroplating (electrodeposition). The pillars were bonded by hand to a copper-plated wafer using solder.

Results:

The criteria used to evaluate the development of each formula were side smoothness, perpendicularity, top flatness, and interior clarity. Evaluation was based on a standardized rubric describing the characteristics associated with each numerical score in each category. Most OEM-41 samples showed good depth of development and perpendicularity, but sidewalls had extensive vertical ridging. OEM-61 samples had smooth sides, but interior cavities were often occupied by "buttress" filaments spanning the gap between walls. A few samples also exhibited structural warping not attributed to development or cleavage artifacts. All precipitated OEM-61 samples exhibited poor perpendicularity and interior clarity.

The surface-normal waveguide pillars had excellent perpendicularity. Some bending at the edge of the sample was attributed to wafer cleavage. Sidewalls showed smooth exterior surfaces, but top flatness seemed to be reduced with increased height, possibly due to unevenness in the thick film.

The copper-core polymer pillars were successfully bonded, from visual inspection, to a copper surface using solder.

Conclusion:

Polynorbornenes like Avatrel are becoming an important material in microsystems packaging owing to their physical properties. Due to variances in formula development characteristics, preliminary experiments were conducted on three formulas of Avatrel to choose the best for different packaging applications. The OEM-41 formula demonstrated characteristics best suited for electrical applications while the OEM-61 is best suited for optical uses. Fabrication processes were then developed for optical waveguide pillars and the bonding between die and substrate using copper-filled coaxial pillars.

Acknowledgements:

Thanks to Dr. Kohl, Ate He, Dr. Bakir, Ed Elce and Dr. Meindl for their knowledge and guidance in this research.

References:

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[2] M. Bakir, et al, "Sea of Polymer Pillars: Compliant Wafer-Level Electrical-Optical Chip I/O Interconnections," IEEE Photonics Technology Letters, vol. 15, pp. 1567-1569, Nov. 2003.

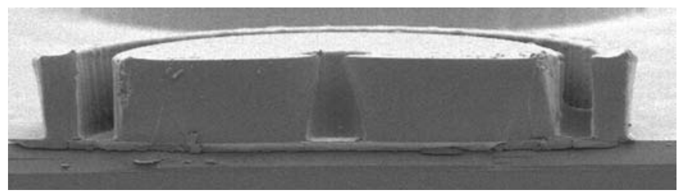

Figure 1: OEM-41 result.

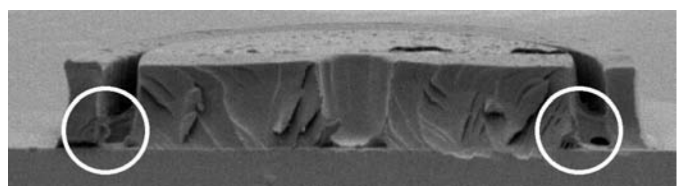

Figure 2: OEM-61 result.

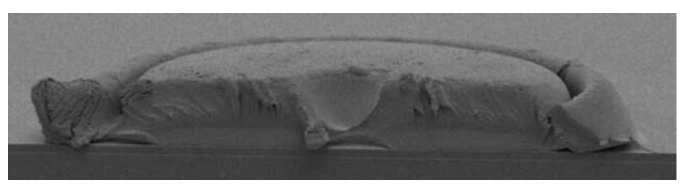

Figure 3: OEM-61 precipitated result.