

# Characterization of the DRIE Process for ETWI for Piezoresistive Inertial Sensors

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## Abstract

Electrical through-wafer interconnects (ETWI) are often integrated with inertial sensors for harsh liquid environment applications. Devices with metal interconnects are very susceptible to corrosion in aquatic environments. An alternative approach is to form highly doped, conductive polysilicon through the wafer from the back side (unexposed to harsh environments) to the front side of the device's chip. ETWI technology requires etching through the wafer. This places a high demand on the through wafer etch profile, critical dimension control, and feature size dependent etch rate (etch lag). On test structures, we measured the sidewall profile and etch rate as a function of several etch parameters (etch cycle time, platen power, current power,  $C_4F_8$  flow, etc). In addition, we assessed practical methodologies for handling the wafer during the etch. The objective of this project is to use statistical design of experiment (DoE) to optimize the deep reactive ion etch (RIE) recipe for through wafer etching and test wafer bonding for through wafer via formation. From the development of electrical through wafer interconnects, more reliable sensor devices can be fabricated for studies in hydrodynamics in harsh environments in addition to a plethora of other applications.

## Introduction

We began by optimizing a baseline recipe using STS-HRM (Surface Technology Systems). Then, we used those results to develop a reliable method for through wafer etching. STS-HRM is based on the Bosch method, which uses a process that alternates between the etch gas ( $SF_6$ ) and the deposition gas ( $C_4F_8$ ). Moreover, etching occurs by two mechanisms: a chemical process in which fluorine from the plasma bonds with the silicon atoms and becomes a volatile gas, and by a physical process in which the fluoride ions bombard the surface, sputtering the material away. Under proper tuning, the Bosch method achieves an anisotropic (downward direction) etching profile because of the alternating etch passivation cycles. The objective of this optimization was to achieve the following conditions: very straight walls, no grass, and small scallops. However, our major challenge for through wafer etching using STSHRM was thermal management due to backside helium (cooling gas) release, and due to photoresist burning.

As a result of etching completely through the wafer, we lose the helium that is located beneath it; hence, we lose the uniformity of the etch across the wafer, and the cooling that we need in order to prevent the photoresist from burning. Therefore, the single wafer was substituted with a polymer-bonded pair of wafers.

## Experimental Procedure

The preparation of the wafers for etch optimization was as follows: spinning  $3\ \mu\text{m}$  SPR 220-3 positive photoresist on an SVG coater track; then, a pattern was formed by exposure using

a Karl Suss MA-6 i-line mask aligner. The wafers were then developed in LDD 26W developer. The STS-HRM etcher was used for the experimental etch matrix.

Based on "Smooth Shallow Template" ( $Dep_{\text{time}} = 2\text{s}$ ;  $Etch_{\text{time}} = 3\text{s}$ ; Throttle Valve $_{\text{dep}} = 15\%$ ; Throttle Valve $_{\text{etch}} = 12.5\%$ ;  $C_4F_8$  flow = 100 sccm;  $SF_6$  flow = 400 sccm;  $P_{\text{source}} = 2500\text{W}$ ,  $P_{\text{platen}} = 45\text{W}$ , Electromagnet - Etch $_{\text{main}} = 1\text{A}$ ; Electromagnet - Delay $_{\text{time}} = 0\text{s}$ ), we selected six parameters to optimize: platen power, etch cycle time, deposition cycle time, pressure,  $C_4F_8$  flow,  $SF_6$  flow. We maximized and minimized the ranges and etched twelve wafers with different recipes. Following the cleaving, we proceeded to examine the samples under scanning electron microscope (SEM).

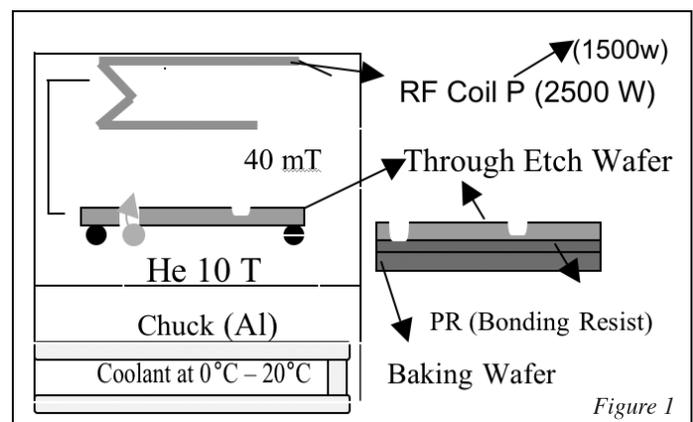


Figure 1

In order to complete a through-wafer etch, a backing wafer was polymer bonded to the through-etch wafer to prevent helium from escaping and to add structural support. First, 10  $\mu\text{m}$  SPR 220-7 photoresist was spun onto the through-etch wafer and 0.5  $\mu\text{m}$  oxide was placed on the backing wafer. Furthermore, 2  $\mu\text{m}$  SPR 3612 photoresist was used as the bonding polymer in between the wafers (Figure 1). Then, both wafers were placed on a 90°C hot plate for 7 minutes with a weight on top. Afterwards, we tested their bond in a vacuum for 5 minutes. Then, we used STS-HRM (“Smooth Shallow Template”), but we lowered the coil power down to 1500 W, because it was discovered that the source power was the principal factor in overheating the wafer. Hence, this reduction in power to 1500 W enabled the masking resist to survive the etch. Finally, we separated the wafers by soaking in acetone for approximately one hour.

### Results and Conclusions

In addition, we can conclude that based on the optimization experiment in STS-HRM, reducing the thermal load by decreasing the source power was the key to bonded wafer through etching. Moreover, a wafer-to-wafer polymer bonding technique and a release method were developed for successful through wafer etching in the high rate STS-2 machine.

### Future Work

In the future, we could explore new methods for through wafer using aluminum as an etch stop. Moreover, we could set the interconnects through the device’s chip and conduct tests in harsh environments.

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### References

- [1] Barlian, AA, Park, S-J, Mukundan, V, and Pruitt, “BL Design and characterization of microfabricated piezoresistive floating element-based shear stress sensors.” Sensors and Actuators A: Physical, vol. 134, pp. 77-87, 2007.

Figure 2, top: We observed very straight and vertical walls, no grass formation, and negligible scallops.

Figure 3, middle: The etch rate achieves 4.5  $\mu\text{m}/\text{minute}$ .

Figure 4, bottom: The computer lights passing through the etched vias in the silicon wafer.

