Post 22 Nanometer, III-V MOSFET Fabrication

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Abstract:

In order to increase the number of transistors on an integrated circuit (IC) in accordance with Moore's Law, we must find new ways to decrease transistor size. As we reach the limits of silicon transistors, new materials such as III-V's, i.e. indium gallium arsenide (InGaAs), may be used for complementary metal oxide semiconductors (CMOS) in sub-22 nm transistors. Key steps in this new process include epitaxial re-growth using molecular beam epitaxy (MBE), planarization, very thin sidewalls, and deposition of gold for self-aligned source/drain contacts. Gold deposition using electroplating will be one of the final steps in creating a functional transistor.

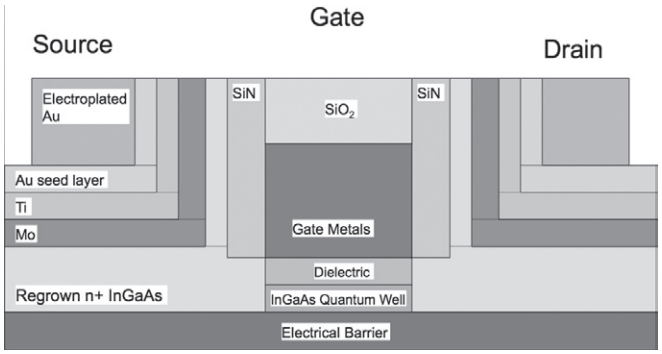

Figure 1: Model of complete InGaAs transistor.

Introduction:

Moore's Law predicts that the numbers of transistors on an integrated circuit will double every two years. In order to continue this trend, the size of transistors must be minimized. In the past, most transistors were made using silicon dioxide as the oxide insulator between the gate electrode and the path. However as transistors become smaller than 45 nm, the silicon dioxide insulator becomes too thin to prevent leakage of electrons to the gate electrode. Silicon is expected to be able to scale to 22 nm, but after that other material alternatives, such as III-V's, may be used in CMOS fabrication (Figure 1).

The group objectives are to demonstrate a working concept transistor using III-V technology, confirm the record breaking current density of 6 mA/μm that theory predicts, and then scale the device to sub-22 nm gate lengths.

Experimental Procedure:

The major focus of this summer research was to achieve self-aligned source/drain contacts using an electroplating system.

Figure 2: SEMCON 1000 electroplating system.

Self-aligned contacts are important because they decrease access resistance and increase the overall speed of the device. Using an electroplating system makes this process easier because we are able to control where our contacts will grow.

The electroplating system that we used was called the SEMCON 1000 (Figure 2). It consisted of a bath full of gold salts, water, and various chemicals, and a drag out cell that rinsed our wafers with de-ionized water. There were also controls for time, temperature, and current. The tool was

a new addition to the clean room, so part of our job was to characterize it for future users. Our main focus was to determine the rate of deposition for gold, based on variations of time and current.

The wafers that we used to run our tests were 2 inch diameter silicon wafers covered with a seed layer of titanium and a seed layer of gold. We then patterned the wafers with LOL 2000 and photo resist AZnLOF5510, and broke them into quarters. We attached our wafers to a plastic wafer carrier, and attached probes to them. The wafer carrier was then immersed in the bath, and a current was applied. The current caused the gold ions in the bath to deposit uniformly on the wafer (Figure 3). We experimented with a variety of currents and times in order to achieve our ideal growth of 100-200 nm.

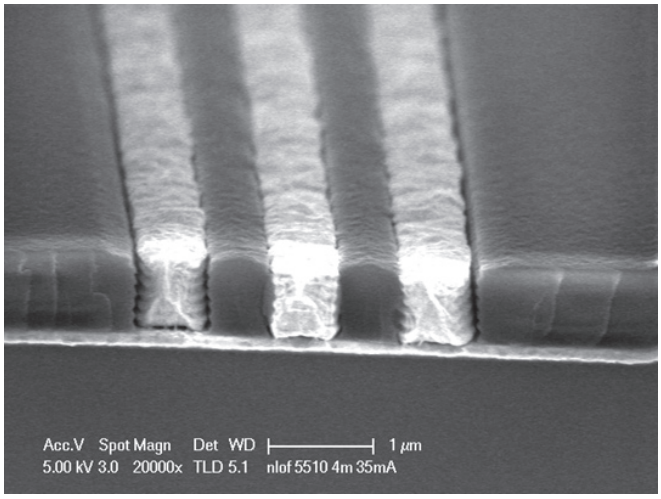

Figure 3: Electroplated gold grown between towers of photo resist.

Results and Conclusions:

We found that the gold deposition seemed to increase fairly linearly with respect to both time and current (Figure 4). We ran experiments varying the current between 20 mA and 45 mA, and varying the time between 1 minute and 4 minutes. Our ideal growths occurred at 25 mA or 30 mA for about 2 minutes. There were some inconsistencies in our results which we suspect are due to the chemistry of the bath.

Although there are still more experiments to be run, we were very encouraged by our results.

Future Work:

The future work for the project will be to build a working proof of concept transistor. There are still issues with making extremely thins sidewalls and using molecular beam epitaxy (MBE) to re-grow InGaAs. Once these issues have been resolved, self-aligned, electroplated, source/drain contacts will be the final step before testing the properties of these new metal oxide semiconductor field effect transistors (MOSFETs).

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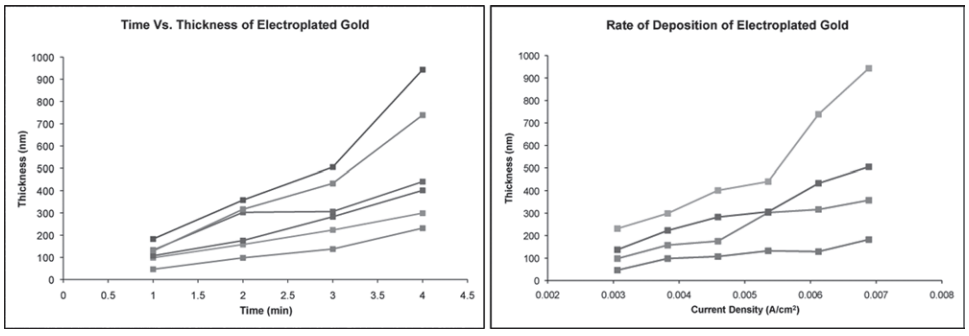

Figure 4: Results of gold electroplating experiments.