

Fabrication of an Array of Thin Film Solid Oxide Fuel Cells

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Abstract:

Thin film solid oxide fuel cells (SOFC) offer unique advantages for diverse applications because of their high efficiency and small size. Thin film SOFCs can operate at much lower temperatures than common large-scale SOFCs. Planar thin film SOFCs ranging from 10^2 to $1.2 \times 10^5 \mu\text{m}^2$ in area were fabricated using conventional microelectromechanical systems (MEMS)-based photolithographic, etching and deposition techniques. Radio frequency (RF) sputtering was utilized to deposit 150-300 nm of yttria-stabilized zirconia (YSZ) to form the electrolyte membrane. The YSZ was then annealed to improve crystallinity. Layers of 6 nm porous platinum (Pt) were deposited as catalyst on both sides of the YSZ membranes to form the anode and cathode electrodes. The array of these small devices will ultimately allow for the investigation of new electrolyte materials using a combinatorial approach.

Introduction:

In recent years, fuel cells have been investigated for clean, portable energy production. Of the different types of fuel cells, the solid oxide fuel cells (SOFC) is among the most common. Normal large-scale SOFC require high temperatures, above 700°C , to be functional. This is caused by the high ionic transfer resistivity in the oxide membrane which necessitates large amounts of kinetic energy in order for trans-membrane oxide movement to occur. Recent research has focused on lowering the operating temperature of SOFC; thus far researchers have been able to fabricate working low-temperature SOFC (300°C - 500°C). To overcome the ionic transfer resistivity in low-temperature SOFC, the thickness of the oxide membrane has been reduced down to the nanoscale; this reduction in the oxide path from cathode to anode reduces the overall resistivity of the cell. This device with a nanoscale membrane is called a low-temperature Thin Film SOFC.

Procedure:

The fabrication process requires a double side polished silicon wafer. 500 nm of low stress silicon nitride (Si_3N_4) was deposited on each side of the wafer by low pressure chemical vapor deposition. Photoresist was spun, exposed and developed on one side of the wafer. The exposed silicon nitride on this side of the wafer was reactively ion etched (RIE) to form a robust mask for the potassium hydroxide (KOH) wet etch later in the fabrication process. After the RIE, the remaining photoresist was removed. On the unpatterned side of the wafer 150-300 nm of YSZ ($\text{Y}_{0.1}\text{Zr}_{0.9}\text{O}_{2.8}$) was RF-sputtered and annealed at 600°C to form the oxide electrolyte membrane.

On the YSZ side of the wafer, the previously delineated photolithographic techniques were employed with identical

photoresist. 6 nm of porous Pt was then evaporated onto the YSZ side to function as the cathode catalyst. A platinum metal lift-off was subsequently performed to expose the Pt pads over the YSZ. A KOH wet etch test showed that the KOH slowly etches the YSZ; therefore, a protective layer of ProTEK B1-18 was coated on the YSZ. A 105°C 50% KOH solution was used to wet etch the exposed Si, on the patterned Si_3N_4 side of the wafer, all the way through the wafer. Upon termination of the KOH wet etch a transparent membrane ProTEK™-Pt-YSZ-silicon nitride is observed, after which the ProTEK™ was removed. Removing the Si_3N_4 makes the membrane very delicate, so the wafer was first cleaved into single die. RIE was used to remove Si_3N_4 on the membranes, leaving the desired Pt-YSZ membranes. In the last step of the fabrication process, 6 nm of evaporated porous Pt was deposited as the anode catalyst, on the KOH side of the die.

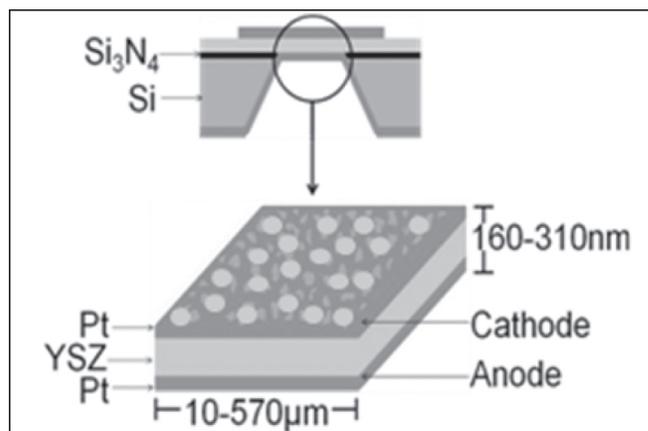


Figure 1: SOFC's YSZ membrane and porous Pt scheme.

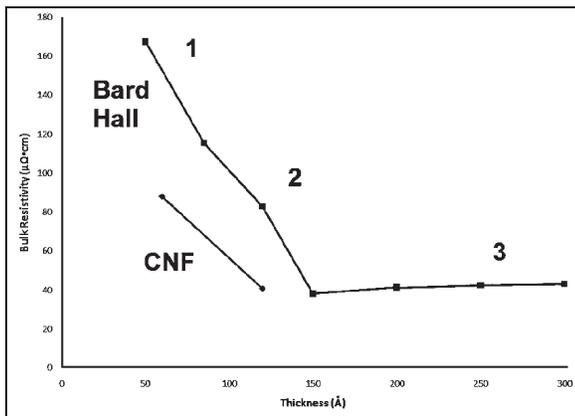


Figure 2: Bulk resistivity vs thickness. Four point resistivity measurements, on different Pt thickness. Interpretation: Region 1; isolated Pt, Region 2; porous Pt, and Region 3; continuous Pt. Pt samples evaporated in two systems located in the CNF and Bard Hall, at Cornell University.

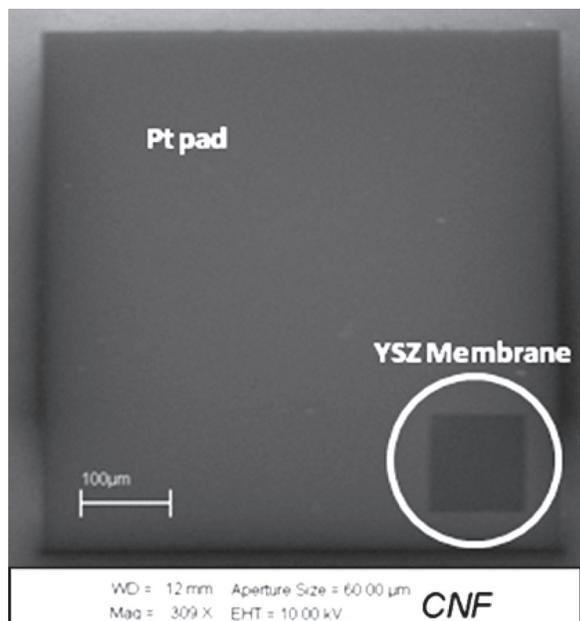


Figure 3: SEM of $1 \times 10^4 \mu\text{m}^2$ YSZ membrane and Pt pad.

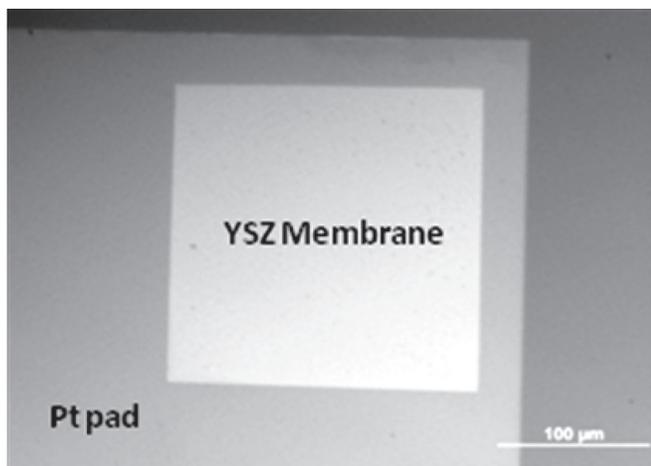


Figure 4: Optical micrograph of $4 \times 10^4 \mu\text{m}^2$ YSZ membrane and Pt pad.

Accomplishments:

The evaporated Pt films on anode and cathode must be porous to form a “triple boundary” interface between the YSZ, the Pt and the gases. This interface allows the reactants, intermediates, and products to permeate the YSZ surface to complete the reaction. The Pt film porosity as result of the Pt thickness film was determined by bulk and sheet resistivity measurements. These measurements allowed us to infer that a Pt film nominally 6 nm thick is porous, therefore this thickness was chosen for all the Pt layers in our thin film SOFCs.

We developed a reliable recipe for fabrication procedure for 10^2 to $3.2 \times 10^5 \mu\text{m}^2$ membranes of the novel material YSZ. Membranes up to $1.2 \times 10^5 \mu\text{m}^2$ survived all the fabrication processes. At this point only the smaller membranes (up to $1 \times 10^4 \mu\text{m}^2$) successfully survived temperatures up to 500°C .

Future Plans:

The next step of the project will be electrical characterization of the thin film SOFCs. I-V curves and power curves will be constructed to determine the maximum power output of the cell. Once the fabrication process has been standardized, and functional thin film SOFC can be fabricated routinely, the focus of the research will change to find new catalysts and oxide electrolytes to enhance performance.

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