Optical Fiber Packaging for Integrated Photonic Structures

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Introduction:

The focus of this summer project was the light coupling of chips. The Lipson group uses tapered fibers to bring laser light close to the edges of the chips they work with. The light is then coupled into waveguides patterned onto the surface of the chip. Each of these chips is fabricated as one of many on a wafer and, after fabrication, wafers have to be diced into the separate chips. This dicing procedure leaves very rough edges, which are not conducive to efficient light coupling. Therefore, after dicing, the edges of each individual wafer needs to be polished smooth. The polishing process takes about two hours per chip. The purpose of this research was to replace the dicing and polishing with a process that would leave smooth edges for better light coupling and, hopefully, reduce the amount of time needed. To this end, we decided to use an etching method.

The wafer we used was a silicon wafer with 3 μm of silicon dioxide grown on the surface. The waveguides would be patterned into this layer of silicon dioxide. The theory was that we could pattern the waveguides to be slightly longer than needed, then etch trenches through the layer of silicon dioxide into which it was patterned. The trenches would intersect the ends of the waveguides, exposing the edges. Then we would etch down into the silicon substrate, far enough that we could cleave the wafer without damaging the waveguides. This process is depicted in Figures 1 and 2. If the sidewalls of the trenches are smooth, then the exposed section of the waveguide should be able to couple light effectively.

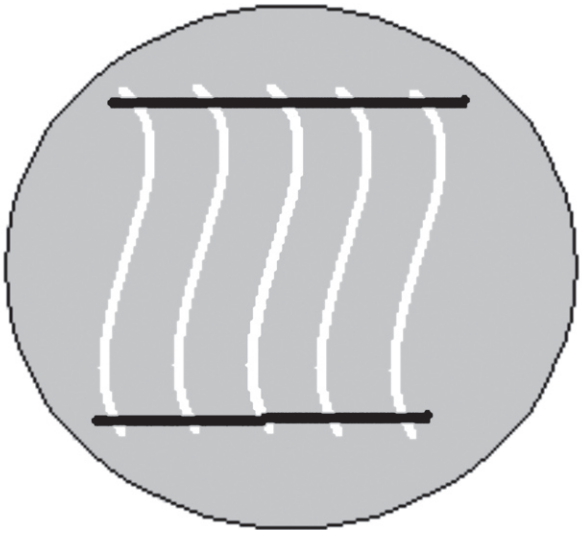

Figure 1: Diagram showing waveguides (white) and etched trenches (black).

Experimental Procedure:

The first part of this process was resist characterization. We used SPR220-3.0 to get a 3 μm layer resist. The exposure dose was first characterized on the EV 620, and the resist development was also characterized. An exposure time of 3.0 seconds with a 90 second development (in MIF 300) were found to be optimal.

The next step was to characterize the etch rate of a whole wafer. For this process we used two machines: the Oxford 100 for silicon dioxide etching, and the Unaxis 770 for deep silicon etching. We evaluated the etch time to be 24 minutes for the Oxford, and the Unaxis etch required 150 to 170 etch cycles to go through approximately 120 μm of silicon.

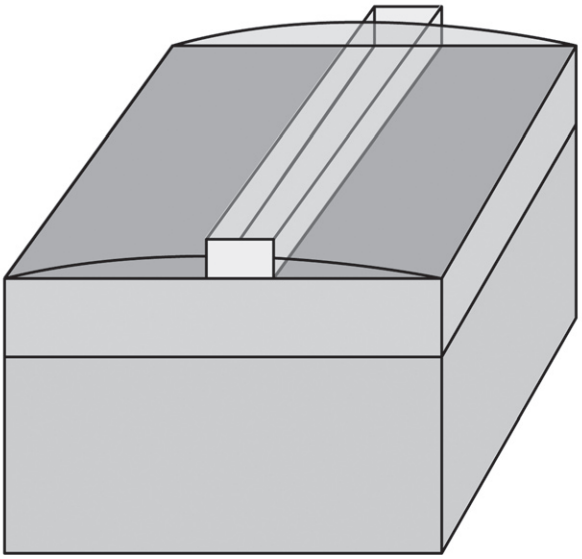

Figure 2: Cross-section of chip with exposed waveguide.

This etch process also had to be characterized on a piece of wafer. The etch time remained the same for the Oxford, however it decreased dramatically for the Unaxis as expected due to etch loading. We initially had been using virgin silicon wafers as carriers for the sample and, as a larger Si area is exposed during the etch, this increased the etch time. The etch loading was resolved by using a Si wafer which had a ~ 3 μm thick thermal oxide layer grown on it.

Since the HTG exposure tool is better suited to handle pieces, we had to perform a dose test on it as well. Before doing so, since we realized that a thicker resist was required so that the samples could undergo the etch steps (since the initial oxide etch had to remove ~ 5 μm), a thicker resist layer was necessary. To this end, since the oxide etch time needed to be 48 minutes, we decided to use SPR220-4.5 to get a 6.7 μm resist layer. After solving adhesion problems by lengthening the soft-bake time and adding a rehydration period, we characterized the exposure and development.

Our next major problem was reticulation. Our initial etch tests were performed with relatively thin photoresist layers, but the 6.7 μm resist was near the range of thicknesses which required a change in process. After the development, we left the chip in a 90°C oven for approximately 4 hours to allow for any solvent remaining from the developer to evaporate. We also needed to etch in 6 minute intervals, leaving time for the sample to cool down between the etches. It was at this point that the Unaxis 770 went down, and remained unusable for the remainder of the summer.

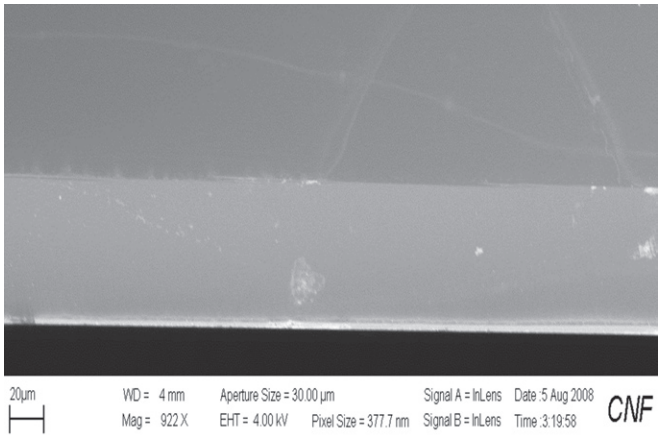

Figure 3: SEM image of trench sidewall.

We were unable to complete the project and verify that the side-wall was indeed smoother. We were, however, able to get some SEM images of the sidewalls that looked promising, one of which is shown as Figure 3. The entire process took approximately 8 hours for a wafer, which may or may not be comparable with the original dice and polish process that took 2 hours per chip.

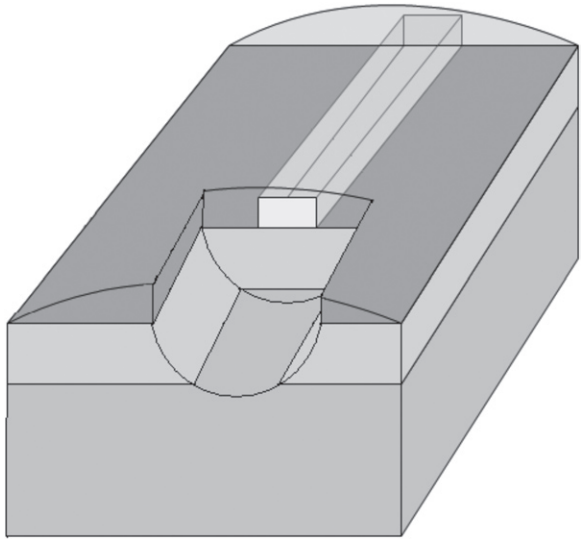

Figure 4: Diagram of chip with etched fiber-holder and exposed waveguide.

Future Work:

The next step in our process would be to etch 125 μm diameter trenches into the chip intercepting and running parallel to the ends of the waveguides. This would act as a fiber holder, allowing the tapered fibers to sit close to the etched-through and exposed ends of the waveguides. Also, this set-up would make for more efficient packaging of the chip after the entire process was completed.

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