Sidewall Metallization of High Aspect Ratio Perpendicular Polymer Structures for Chip I/O Interconnections

Tajudeen Shodeinde
Electrical Engineering, North Carolina Agricultural and Technical State University

NNIN REU Site: Microelectronics Research Center, Georgia Institute of Technology
NNIN REU Principal Investigator: Dr. Muhannad Bakir, Electrical Engineering (Microelectronics), Georgia Institute of Technology
NNIN REU Mentor: Calvin R. King Jr., Electrical Engineering (Microelectronics), Georgia Institute of Technology
Contact: S.P.Shodeinde@gmail.com, Muhannad.bakir@mirc.gatech.edu

Abstract:

As complementary metal oxide semiconductor integrated circuits (CMOS ICs) continue to advance, the need for ever better chip input/output (I/O) interconnect technology becomes ever more critical. In this research, we explore the use of a "Sea of Polymer Pillars" to transmit electrical and optical signals rapidly from the die to the substrate. The intrinsic polymer pillars (or optical I/Os) are processed through microelectronic fabrication techniques that include spin coating, soft baking, exposing to UV light, hard baking, developing, and curing. Mechanical reliability plays a major role due to the fact that these pillars must be compliant enough to withstand the thermo-mechanical stresses induced as a result of the difference of the coefficient of thermal expansion (CTE) of the die and the substrate. On the other hand, before these polymer pillars can actually transmit electrical signals, the pillars need to be metallized with an electrical conductor, copper, on the sides and not the tips. The primary focus of this research is to develop a unique process for single sided metallization of polymer pillars to allow them to operate as electrical and optical I/Os.

Introduction:

Chip I/O interconnects provide mechanical interconnection between the silicon die and the substrate. They also provide a path for delivering power supply current, high frequency signals and heat dissipation [1]. There are various types of compliant I/O interconnects including micro-springs, helix-like interconnects, coil-like interconnects, and "Sea of Polymer Pillars" [2].

"Sea of Polymer Pillars" is an I/O interconnect technology that represents modern day micro-electro-optical-mechanical systems (MEOMS) [3], in the sense that they are very small structures that transmit electrical and optical signals while undergoing mechanical deformations. These polymer pillars are mechanically compliant cylindrical structures that mitigate thermo-mechanical expansion mismatches between the chip and substrate. A scanning electron microscope (SEM) image of such pillars can be seen in Figure 1. Our research goals were partitioned into two tasks. The first task of this research project involved fabricating the polymer pillars and metallizing one side of their sidewall (instead of the complete sidewall) and not the tips with a good electrical conductor, such as copper (Cu), so that the electrical-optical pillars would be more flexible.

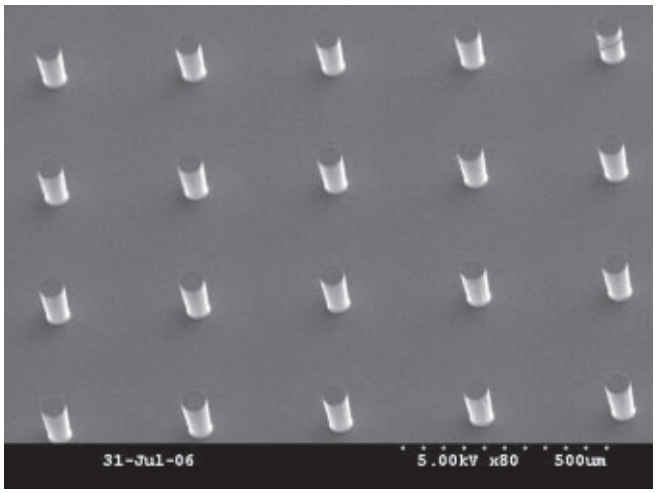


Figure 1: SEM micrograph of 100 µm tall polymer pillars.

It is known that the CTE of the silicon die and a substrate have a large mismatch. While the CTE of the silicon die is 3 ppm/°C, the CTE of the printed wiring board (PWB) is 17 ppm/°C. Thus, this indicates that when these two materials undergo thermal cycling, the substrate will have a greater expansion than the silicon die, leading to bending of the I/O interconnections. Therefore, the last half of the project included making these I/O interconnections (polymer pillars) more compliant by increasing their high aspect ratio.

An illustration of the problem can be seen in Figure 2, while the goal is illustrated in Figure 3. In addition, we discovered that we can utilize our unique process technology to fabricate solely very high aspect ratio (> 20:1) vertical copper wires by thermally decomposing the polymeric material. While this result was not part of

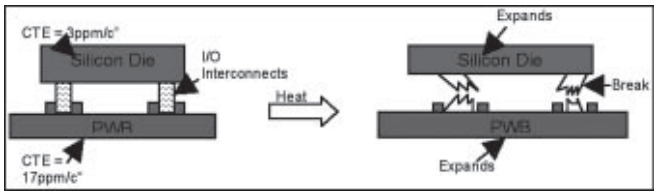
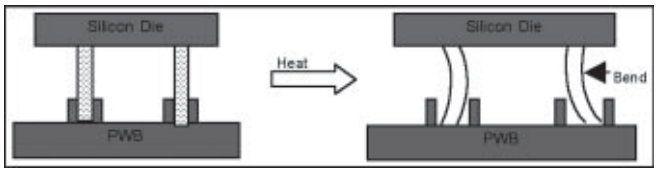


Figure 2: Short I/O interconnects break during thermal cycling.

Figure 3: Long I/O interconnects bend instead of break during thermal cycling.



the original research plan, it was a critical demonstration as it could potentially have very significant applications in a number of areas.

Experimental Procedure:

Two layers of Avatrel polymer were spun on an oxidized wafer. The first layer was pre-baked for 8 minutes at 108°C before the second layer was spun on the sample. The second layer of Avatrel was soft baked for 75 minutes at the same temperature to reduce any solvents. After the sample cooled, lithography was performed on the sample. Next, the wafer was hard baked for 20 minutes and the sample was developed to produce the required polymer pillars. The pillars were cured for one hour. Once the pillars had been cured, thin layers of titanium and gold were uniformly deposited. A second set of polymer pillars were fabricated on the metallized surface using the same recipe. During the lithography step, the mask was aligned so that the patterns on the mask covered half of the polymer pillars on the sample. The sample was then hard baked and developed. The first layer of titanium covering the gold layer was etched using buffered oxide etchant (BOE). Next, copper was metallized on the sidewall of these pillars by electroplating. This step concluded the first half of the project.

To proceed with the last half of the project, after the sidewalls of the pillars had been metallized, the sample was heated in a furnace at 450°C to thermally decompose the polymer. After the polymer had been decomposed, the gold and the titanium seed layers were etched using gold and BOE etchants, respectively, to produce the high aspect ratio copper pillars (Figure 4).

Results and Conclusions:

The pillars were fabricated and their sidewalls were metallized with copper. Figure 4 illustrates how the sample looked after the polymer had been decomposed when heated in the furnace.

The sidewall metallization remains as very high aspect ratio copper pillar (> 20:1).

Future Work:

Future work includes optimizing the fabrication process of the structures under consideration and testing the mechanical, electrical, and optical properties of the electrical and optical polymer pillar I/Os. Assembly of these I/Os on a PWB should also be performed in the future.

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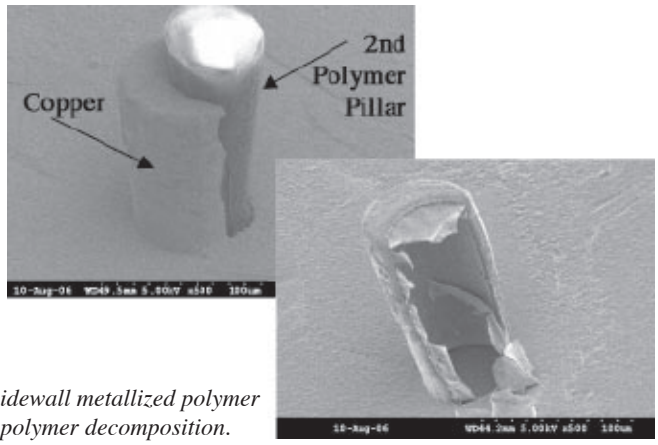

Figure 4: SEM images of sidewall metallized polymer pillars before and after polymer decomposition.