**Interconnects and Reliability**

Sandip Tiwari  
st222@cornell.edu

**Logic Interconnects**  

**Prologue**

Global  
Middle  
Local  

Schematic X-section  
- Passivation  
- Dielectric  
- Etch Stop Layer  
- Dielectric Capping Layer  
- Copper Conductor with Barrier/Nucleation Layer  
- Pre Metal Dielectric Tungsten Contact Plug

30 nm
Interconnects

- Technology scaling occurs with increasing average interconnect length and routing density and increased interconnect aspect ratio
  - Interconnects grow linearly with cells in ordered arrays (memories, e.g.)
  - Interconnects grow as the square of the elements in random logic
- Local (intra-block) wires scale with block size, but global (inter-block) wires do not.

Below the Interconnect

Strip Line Capacitance

Reducing line width will not reduce $C_0$ proportionally for small $w/h$

Clock skewing

Clock signals in 400 MHz IBM Microprocessor (measured using e-beam prober)

- Transmission line effects cause overshooting and non-monotonic behavior

P. Restle (1998)
**Time Scales of Pulse Propagation**

Scale of distances and delays (c/n):

<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>Board</td>
<td>20 cm</td>
<td>0.67 ns</td>
</tr>
<tr>
<td>Chip</td>
<td>1 cm</td>
<td>33 ps</td>
</tr>
<tr>
<td>Logic Units</td>
<td>0.1 cm</td>
<td>3.3 ps</td>
</tr>
</tbody>
</table>

**Short Interconnects:** Capacitive (lumped), Cross-talk & Noise

**Long Interconnects:** Transmission lines, cross-talk & noise, ground loops

Interconnects that need to maintain precise timing and match in jitter: Clocks

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**Short Transmission Lines**

$$Z_0 = \sqrt{\frac{R+j\omega L_0}{G+j\omega C_0}}$$

$$\lim_{R \to 0, G \to 0} C_0 l$$

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

$$v = \frac{1}{\sqrt{L_0 C_0}}$$

- Open: $C_0 = \frac{1}{vZ_0}$
- Short: $L_0 = \frac{Z_0}{v}$

*example:* if $Z_0 = 50 \, \Omega; \ v = c/2 = 0.15 \, \text{mm/ps}$

$\Rightarrow C_0 = 0.1 \, \text{pF/mm}; \ L_0 = 0.33 \, \text{nH/mm}$
**Transmission Line Implication**

<table>
<thead>
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<th>Scale of distances and delays (c/n):</th>
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<tr>
<td>Board</td>
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<tr>
<td>Chip</td>
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<tr>
<td>Logic Units</td>
</tr>
</tbody>
</table>

- Transmission line effects should be considered when the rise or fall time of the input signal \((t_r, t_f)\) is quite smaller than the time-of-flight of the transmission line \((t_{flight})\), \(t_r (t_f) << 2.5 t_{flight}\)
- Transmission line effects increasingly important when the total resistance of the wire is limited: \(R < 5 Z_0\)
- The transmission line treatable as lossless when the total resistance is substantially smaller than the characteristic impedance: \(R < Z_0/2\)

**Matching**

Series Source Termination

Parallel Destination Termination
**Lossless Transmission Line**

Pulse impedance:

\[ = Z_0, \text{ i.e. } \frac{V}{I} = Z_0 \]

For a load, \( Z \), reflection coefficient

\[ \rho = \frac{Z - Z_0}{Z + Z_0} \]

Open: \( \rho = 1 \)
Short: \( \rho = -1 \)

---

**On Chip Transmission Line**

On chip, usually, \( R_s > Z_0 \)
**Capacitively Coupled Noise**

From Odd and Even mode analysis:

\[
\frac{V_n}{V} = \frac{1}{4} \left( \frac{C_{12}}{C_{11}} + \frac{L_{12}}{L_{11}} \right) \times f
\]

- \[f = \frac{2\tau_t}{\tau_r} \text{ for } \tau_r > 2\tau_t\]
- \[f = 1 \text{ for } \tau_r \leq 2\tau_t\]

Inductive Coupling, Short line:

- \(\tau_r > \tau_t\), capacitor termination
- \[\frac{V_n}{V} = \frac{L_{12}}{L_{11}} \frac{\tau_t}{\tau_r} \left( \tau_t + \frac{Z_0 C_L}{\tau_r^2} \right)\]

Inductively coupled component is negligible for most on-chip conditions

**Loosely Coupled Transmission Lines**

From Odd and Even mode analysis:

- Inductive Coupling, Short line:
  - \(\tau_r > \tau_t\), capacitor termination
  - \[\frac{V_n}{V} = \frac{L_{12}}{L_{11}} \frac{\tau_t}{\tau_r} \left( \tau_t + \frac{Z_0 C_L}{\tau_r^2} \right)\]

Inductively coupled component is negligible for most on-chip conditions
**Crossing Lines on Chip**

Non Transverse EM (non TEM)
Slow wave structure
Strong coupling between parallel lines

![Diagram of crossing lines on chip]

Source of ground loop problems

**Lossy Lines**

For low loss:
\[ r < Z_0 \frac{r_L}{r_T} \]
\[ V = u \left( t - \frac{x}{v} \right) \left[ \exp(... \right] + \text{slow RC response} \]

Voltage doubling at line end compensates for loss, but may cause problems at intermediate points

For high loss:
\[ r > Z_0 \frac{r_L}{r_T} \]

Extra Delay = \[ \frac{r(C_0 t + C_L)}{2} \]

<table>
<thead>
<tr>
<th>( r )</th>
<th>( w \times h )</th>
<th>( \tau )</th>
<th>( \frac{r_L}{r_T} )</th>
<th>( \frac{r}{r_T} )</th>
<th>( \frac{r \Sigma C}{2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>ns</td>
<td>( \mu m^2 )</td>
<td>( \Omega )</td>
<td>ps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.2</td>
<td>5x1.5</td>
<td>60</td>
<td>2.4</td>
<td>90</td>
<td></td>
</tr>
<tr>
<td>0.2</td>
<td>1x0.5</td>
<td>900</td>
<td>540</td>
<td>1350</td>
<td></td>
</tr>
</tbody>
</table>
**Skin Effect**

Skin Depth \[ \delta = \sqrt{\frac{2\rho}{\omega \mu}} \]

On chip TEM line \( t \leq h \)

Assume delay is limited by wire resistance

Then, \( \delta > \sqrt{wt} \) for \( w < h \) Narrow line

\( \delta > \sqrt{ht} \) for \( w \gg h \) Wide line

Skin effect is unimportant for usual case of on-chip propagation.

For \( \tau_r = 100 \, ps \) and \( \rho = 3 \mu \Omega \cdot cm \), \( \delta = 2 \mu m \)

But, if size becomes too small, scattering effects from surfaces would contribute

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**Using Bypass for Resistive Lines**

Driver

WL

Polysilicon word line

Metal word line

Driving a word line from both sides

Metal bypass

WL K cells Polysilicon word line

Using a metal bypass
Long Lines: Reducing RC Delay

Impact of inductance on supply voltages:

Change in current induces a change in voltage

Longer supply lines have larger L

Critical to design power lines for low inductance
**Segmenting Matched Line Drivers**

Initial design

Revised design with matched driver impedance

**Output Driver Terminations**
Parallel Terminations: Using Resistance from Transistors

Electromigration
A Cross-Section

Maxwell's Equations

Original
\[ \nabla \times E = -\frac{\partial B}{\partial t} \]
\[ \nabla \cdot D = \rho \]
\[ \nabla \times H = J + \frac{\partial D}{\partial t} \]
\[ \nabla \cdot B = 0 \]
\[ J = \sigma E \]

Scaled
\[ \nabla' \times E' = -\frac{\partial B'}{\partial t'} \]
\[ \nabla' \cdot D' = \rho' \]
\[ \nabla' \times H' = J' + \frac{\partial D'}{\partial t'} \]
\[ \nabla' \cdot B' = 0 \]
\[ J' = \sigma E' \]

Scaling Factors
\[ x : \lambda \]
\[ \nabla : \frac{1}{\lambda} \]
\[ t : \lambda \]
\[ \phi : \kappa \]
\[ E : \frac{\kappa}{\lambda} \]
\[ H : \frac{\kappa}{\lambda} \]
\[ J : \frac{\kappa}{\lambda^2} \]
\[ \rho : \frac{\kappa}{\lambda^2} \]
\[ \sigma : \frac{1}{\lambda} \]
### Table: Key Properties of Low-κ and Oxide Materials

<table>
<thead>
<tr>
<th>Property</th>
<th>Low κ</th>
<th>Oxide</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density (g/cm³)</td>
<td>1.03</td>
<td>2.2</td>
</tr>
<tr>
<td>Dielectric constant (κ)</td>
<td>~1.9-2.5</td>
<td>4.1</td>
</tr>
<tr>
<td>Modulus (GPa)</td>
<td>~3-9</td>
<td>55-70</td>
</tr>
<tr>
<td>Hardness (GPa)</td>
<td>~0.3-0.8</td>
<td>3.5</td>
</tr>
<tr>
<td>cTE (ppm/K)</td>
<td>~10-17</td>
<td>0.6</td>
</tr>
<tr>
<td>Porosity</td>
<td>~35-65%</td>
<td>none</td>
</tr>
<tr>
<td>Average Pore</td>
<td>&lt;2.0-10 nm</td>
<td>none</td>
</tr>
<tr>
<td>Thermal Conductivity (W/m.K)</td>
<td>0.26</td>
<td>1.4</td>
</tr>
</tbody>
</table>

### Table: Comparison of Various Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low-κ Values</th>
<th>ESL Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant of Low-κ</td>
<td>3.6</td>
<td>6.8</td>
</tr>
<tr>
<td>Effective Dielectric Constant</td>
<td>~3.9</td>
<td>~4.4 - 4.8</td>
</tr>
<tr>
<td>Aspect Ratio</td>
<td>~3.5</td>
<td>~6.0</td>
</tr>
<tr>
<td>Min Width (MET3, nm)</td>
<td>175</td>
<td>140</td>
</tr>
<tr>
<td>R_sheets for Min Width</td>
<td>79</td>
<td>113</td>
</tr>
</tbody>
</table>

### Notes
- ESL: Enhanced Substrate Low-k
- Low-κ materials are characterized by lower dielectric constants, lower thermal conductivity, and lower cTE compared to oxide materials.
Damascene

Capping/ Etch-stop layer
Side wall barrier
Bottom wall barrier

Percentage Lost Copper Area due to Liner

130 nm  90nm  65nm  45nm

0%  5%  10%  15%  20%  25%  30%
Metal Resistivity

At <200 nm, Cu Resistance starts to rise
Grain boundaries and interface scattering – with Ta based barriers

Voids and accumulation caused by flux divergence, accelerated by stress and temperature
Interconnects

Passivated Cu:
350 nm, width 600 nm

Stress temperature: 230°C

Current densities increased up to $10^7$ A/cm² during ~17 hrs

Sneider, Fut Fab Vol 19

Electromigration

Technology & Reliability Issues

Hillocks

Nucleation on defects

Before

After

Metal Voids

(100)
**Technology & Reliability Issues**

- **Electromigration**
- **Voids!**
- **Diffusion Barrier!**
- **Dielectric cracking!**
- **Porosity!**

**Electromigration**

Drift of atoms in the direction of electron flow caused by fields: electron wind

**Aluminum:** mitigated by alloying with Cu and conductive barrier/liner layers

**Nernst Equation:**

\[
v_d = F_e \cdot M = Z_{eff}^* e \frac{D_{eff}}{k_B T} = Z_{eff}^* e \rho \frac{D_{eff}}{k_B T}
\]

- Atom drift velocity
- Electromigration driving force
- Intrinsic atom mobility
- Effective charge
- Field
- Current density
- Diffusivity
- Resistivity

\[
D_{eff}(T) = D_0 \exp \left( -\frac{\Delta H}{k_B T} \right)
\]
**Reliability of Insulators**

In transistors:
- thick and thin oxides and consequences of high $\kappa$
- with particular emphasis on NBTI
- Implications for circuits

In Flash Memories
- implications of relatively thick oxides

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**Gate Dielectric: Nitrided Oxide with polySi**

Leaky, difficult to control, B penetration, SILC, soft breakdowns, NBTI, PBTI, …
**Metal Gates and High $\kappa$**

- Work Function Stability
- Impact of Deposition Process: PVD, CVD, etc.
- Oxidation
- S/D Implant Impact
- Plasma Charging
- Electromigration
- Adhesion
- SER Impact
- High-k Gate Dielectric
- Charge Trapping
- Defect Density
- TDDB Physics
- Mobility
- Leakage Physics
- NBTI, PBTI
- CHC Stability

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**Plasma Damage**

Linder, P2ID(1948)

Thin Oxides (scaled devices) reduced damage
Thick Oxides (IO devices) damage persists
New effects at small dimensions: new dielectrics, different BEOL dielectrics and processing techniques (UV cure?) and heavy dose implants
Old: Charge to Breakdown

Defect generation to Breakdown

FIG. 1. Charge-to-breakdown as a function of gate voltage at room temperature on large area FETs ($5 \times 10^{-4}$ cm$^2$) for gate oxide thickness in the range from 2.2 to 6.0 nm.

DiMaria, APL(1997)

Bias Dependence of Breakdown Growth

From 0 to 100 $\mu$A breakdown leakage in 300 years of continuous operation

J. Stathis (2008)
**Charge to Breakdown**

Stathis, IRPS(2001) and JAP (1999)

**SILC**

Stress Induced Leakage Current
Oxides and Transport in Insulators

Oxides:
The properties of SiO₂ change to bulk like over a length scale of about 2 monolayers. Direct tunneling is certainly quite significant at sizes below about 1.5 nm.

What does electron transport do when biases are applied in oxides?

Energy losses in the insulator – breaking bonds and trapping carriers (so charge in oxides, and sites in oxides through which electron transport can take place (e.g. by percolation)

Energy losses at interfaces – breaking bonds, releasing ionized species that can then move in applied fields

Magnitudes of various effects depend on how thick oxides are, bias conditions and multiple phenomena may be important simultaneously.

Effects may be hard, i.e. "abrupt" or soft, i.e. a gentle degradation

Dielectric Reliability: Nitridation Hardening

Bulk properties lost below 2 monolayers

Below 32 nm, SiON required for appropriate EOT (electrical thickness) is very high in N

Power law mechanisms may involve the release of H₀ and H⁺ from poly-SiON interface
Outline

- Ultra-thin oxide breakdown
  - “Progressive” breakdown
    - Circuit implications
- Negative Bias Temperature Instability (NBTI)
  - Role of Nitrogen
- New materials
- Comments for thick Oxides (NVRAMs)

Progressive Breakdown

- Hard Breakdown doesn’t happen suddenly as a catastrophic process
- Happens gradually over a measurable time scale
- Degradation rate is slower for lower stress voltages

Log time scale

Hosoi, IEDM(2002)
What does it Mean?

Thick Oxide High Voltage Stress

Ultra-Thin Oxide Low Voltage Stress

Interface State Distribution

More mid-gap centers in pure oxide

More defects in the upper portion of the Si band gap for nitrided oxides

Mid-gap defects with gated diode peak

Conduction band edge defects with flat-band gate leakage (LV-SILC)

Stathis, INFOS(2005)
Interpretation

- All breakdown is progressive
  - Continuum of rates of post-BD current growth
  - Progressive BD can be "stopped" at intermediate current level
  - Operational definitions are circuit dependent

Negative Bias

(a) Positive bias shifts away from the SiO2/Si interface

(b) Charge exchange: Hole trapping or electron detrapping increases the net positive charge at the Si/SiO2 interface
**NBTI: A Serious Reliability Issue**

- pMOS threshold shift (drain current reduction)
  - Interface states and positive oxide charge
- Serious concern for low $V_{DD}$ new technologies
- Nitridation worsens NBTI

**Channel Hot Carrier Issues with Scaling**

Decreasing lifetime
$L_{o}$ shrinking while $V_{DD}$ scaling limited
Increased use of well bias $\Rightarrow$ additional stress

*JW McPherson, IEDM(2005)*
**NBTI: Negative Bias Temperature Instability**

- Power law dependence of $t^n$ with $n \sim 0.15-0.25$
- Source believed to be electrochemical reaction with a hydrogen related species in the oxide
  - Reaction/diffusion

![Diagram of NBTI](image)

Miura & Matukura, JJAP(1966)

- Characterization $V_{DD}$ (V)
- Power law dependence of $t^n$ with $n \sim 0.15-0.25$
- Source believed to be electrochemical reaction with a hydrogen related species in the oxide
  - Reaction/diffusion
**NBTI: Dispersive Transport**

Zafar, JAP(2005)

- Hydrogen density calculated from kinetics (is statistical)
  - Creation of interfacial and oxide traps
  - Interfacial and oxide traps have charged and neutral states
  - Charge state densities follow Fermi function
- Correct treatment of the drift/diffusion of [H] including dispersive nature of process in amorphous medium
  - Dispersive transport arises when mobile species experiences a broad distribution of barrier heights leading to an exponentially broad distribution of hopping times
- Causes stretched exponential

\[
\Delta N_{it} = N_0 \left[ 1 - \exp \left( -\frac{R(vt)^\beta}{N_0} \right) \right]
\]

This reduces to power law form \( \Delta N_{it} = R(vt)^\beta \) at short times, and accounts for saturation at long times

**Process Influence**

- Nitridation of gate oxide enhances NBTI
- Deuterium – some publications show improvement
- Fluorinated gate oxide reduces NBTI
  - Improvement diminishes with nitridation
- Oxidation conditions and tooling
- BEOL charging enhances NBTI effect
- Composition of contact etch stop layer and stress films
Circuit Implications

SRAM

Increasing asymmetry from NBTI and PBTI

PBTI more sensitive to $T_{\text{inv}}$
SRAM cell itself more sensitive to NBTI
Read affected more than Write

A. Bansal, Micro Rel (2009)
**Implications of Progressive Breakdown**

Many characteristics are not strongly perturbed by oxide breakdown, e.g., transconductance ($gm$) and threshold voltage ($V_T$).

Strongest implication is in an increase in off current in gate-drain or gate-source leakage.

\[ \Delta I = K(V_{gd})^p \]

\[ \Delta I = K(V_{gs})^p \]

Include power law equation from breakdown curves.

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**Inverter Transfer Characteristics**

Loads output of 1st inverter by breakdown in 2nd.

Logic may tolerate high breakdown leakage ($\sim 10 \mu A$) with reduced noise margin (is another source of variability).
SRAM Static Noise Margin

At breakdown current > 50 μA, SNM reduced by 50%

Worst case: n-source breakdown
• Pulls down voltage at opposite node
• Loads a weaker pFET

Rodriguez, EDL(2002)

Circuit Failure Distribution

\[
F(t) = \frac{1}{T_{63} - T_{PBD}} \left\{ T_{63} \left[ 1 - \exp \left( -\frac{t}{T_{63}} \right) \right] - T_{PBD} \left[ 1 - \exp \left( -\frac{t}{T_{PBD}} \right) \right] \right\}
\]

Follows from

Weibull distribution of oxide BD times

(\(\beta=1\) for \(t_{ox} < 2\) nm): \(F_{BD}(t) = 1 - \exp \left[ -\left( \frac{t}{T_{63}} \right)^{\beta} \right] \approx \frac{t}{T_{63}}\)

Assumed exponential distribution of post-BD times (\(\Delta t\)):

\[
f_{PBD}(\Delta t) = \frac{1}{T_{PBD}} \exp \left( -\frac{\Delta t}{T_{PBD}} \right)
\]

E. Wu, IEDM(2003)
Circuit Failure Distribution

Example:

\[ T_{63} = T_{PB} \]

\[ F(t) = 1 - \exp \left( -\frac{t}{T_{63}} \right) \left( 1 + \frac{t}{T_{63}} \right) \approx \frac{t^2}{T_{63}^2} \]

For 100 ppm failure (F=10^{-4})

\[ t_{1stBD} = 10^{-4}T_{63} \Rightarrow t_{circuit} = 10^{-2}T_{63} \]

A 100x increase in lifetime

High \( \kappa \)
**HfSiON: SiO₂**

*Shanware, IEDM(2003)*

2-3 orders of reduced leakage over SiO₂
Carrier mobility is ~20% below universal curve at high fields
Thermal stability to 1100°C

**High κ Breakdown**

Breakdown strength decreases with κ
Field/voltage acceleration γ increases with κ (useful in burn-in and stress testing)
**NBTI in High \( \kappa \)**

- Similar to SiO\(_2\)
- Interface dominated
- Power law time dependence
- Saturation
- Relaxation
- Dependence on temperature & field

**High \( \kappa \) Stability**

Some of the high \( \kappa \) dielectrics are quite unstable under stress.
Lower breakdown strength will affect thickness scaling.

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*Zafar, EDL(2005)*

*Shanware, IEDM(2003)*
**HfO\(_2\)/SiO\(_2\) Stack Stressing**

\[ I = I_{\text{SAT1}}[1 - \exp(-t_{\text{STRESS}}/\tau_1)] + I_{\text{SAT2}}[1 - \exp(-t_{\text{STRESS}}/\tau_2)] \]

![Graph showing current vs. stress time](image)

Fig. 2. Average current measured as a function of the stress time during the 10 s, 1 V CVS applied when the stress is stopped. HfO\(_2\)/SiO\(_2\) stacks with 1 and 1.8 nm thick SiO\(_2\) interfacial layer have been considered.

Two time constants (others have observed three)

At the beginning: due to pre-existing traps (?)

Then, degradation due to stressing

A third one, depending on thicknesses, due to hard breakdown

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**Recovery: Metal Gate with high \(\kappa\)**

Recovery and recovery rate after stressing

![Graphs showing recovery and recovery rate](image)

Interface properties affect \(\Delta V_T\), but little effect on recovery

Stress field, rather than stressing voltage, influences NBTI recovery in pMOSFET

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*E. Amat, Microelectron Rel (2007)*

*M. Wang, Micro Eng (2009)*
**Metal Gate**

FUSI: fully silicided

Higher dielectric leakage and reduced breakdown strength with metal gates (FUSI)

Electric stressing show higher $V_T$ shifts in metal gates

Metal gates:
- Stability of interface under NBTI and PBTI
- Process impact of charging, breakdown, TDDB
- Workfunction variability
**Metal Gate Breakdown Transients**

Fast breakdown transients (i.e. hard breakdown) observed in metal gates FETs in the voltage range where polySi gate show progressive breakdown

Advantage of progressive breakdown lost for metal gates

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**Metal Gate with High \( \kappa \)**

At <1 \( \mu \)A, progressive breakdown before catastrophic breakdown

The increase in stress current just before hard breakdown is progressive breakdown since independent of device area and localized in the same position as final hard breakdown

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*Palumbo, IRPS(2004)*

*S. Lombardo, ISAGST(2006)*
Charge Trapping Dependence on Gate

- Metal gates are better
- Silicide is similar to polySi
- polySi/high $\kappa$ interactions appear to be prime suspect for charge trapping instabilities in polySi and FUSI devices
- PBTI has a stretched exponential dependence similar to NBTI

Summary

- For polySi gates: “Hard” breakdown is a slow (“progressive”) process:
  - Breakdown criterion is circuit-dependent
  - Circuit failure will be later than initial oxide breakdown
- For metal gates: Progressive breakdown is less apparent
- $V_T$ stability is a concern for oxynitride and new dielectrics/gates
Clock Span

Increasing \( f_{\text{clk}} \) and speed
- Reduced logic span
- Higher electromagnetic coupling: capacitive coupling inductive bounce

Source: Saraswat

Transmission Line

\[
\frac{\partial^2 V}{\partial x^2} = \frac{1}{r} \frac{\partial^2 V}{\partial t^2} + \frac{1}{l c} \frac{\partial V}{\partial t}
\]

The Wave Equation
**Repeaters**

Taking the repeater loading into account

\[
    m_{opt} = L \sqrt{\frac{0.38rc}{0.69R_dC_d(\gamma + 1)}} = \sqrt{\frac{t_{wire(unbuffered)}}{t_{p1}}}
\]

\[
    s_{opt} = \sqrt{\frac{R_dC}{rC_d}}
\]

For a given technology and a given interconnect layer, there exists an optimal length of the wire segments between repeaters. The delay of these wire segments is independent of the routing layer:

\[
    L_{crit} = \frac{L}{m_{opt}} = \sqrt{\frac{t_{p1}}{0.38rc}} \quad t_{p, crit} = \frac{t_{p, min}}{m_{opt}} = 2\left(1 + \sqrt{\frac{0.69}{0.38(1 + \gamma)}}\right) t_{p1}
\]

**Inductance in Supply Lines**

Input rise/fall time: 50 psec

Input rise/fall time: 800 psec
Mitigating Inductive Effects

- Separation of power pins for I/O pads and core
- Multiple power and ground pins
- Careful positioning of the power and ground pins on the package
- Increase the rise and fall times of the off-chip signals to the maximum extent allowable
- Schedule current-consuming transitions
- Improved packaging
- Add decoupling capacitance

SRAM cell Flip Failure Envelope

Minimum voltage of SRAM affected by combination of NBTI (pFET VT shift) and Oxide progressive breakdown

Metal Gate High $\kappa$

- Major issue
  - Mobility degradation
  - Threshold voltage control
    - For high $\kappa$, electron trapping under positive bias (PBTI in nFET) is a new concern