Fabrication of Graphene Field Effect Transistors

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Abstract:

Graphene is an exciting new material because of its two-dimensional nature and interesting mechanical and electrical properties. There is still much room for development in methods for growing graphene, such as chemical vapor deposition (CVD) on copper. Making field effect transistors (FETs) with graphene is a practical way to assess the characteristics of a given sample of graphene and determine if a method for creating graphene is effective. The focus of this project was to fabricate graphene FETs to assess the quality of graphene grown through CVD on copper. This process was broken down into three main steps: (1) the electrochemical transfer of graphene from copper to silicon (Si) wafers, (2) the patterning of electrodes onto the graphene covered wafers, and (3) the electrical testing of resulting devices through four-point-probe and transistor measurements. Graphene was transferred through the application and removal of poly(methyl methacrylate) (PMMA) on copper (Cu). The electrodes were patterned using photolithography and evaporative metal deposition. Four-point-probe and transistor measurements were attempted as a means to assess the sheet resistance, carrier mobility, and carrier density of the graphene.

Introduction:

In the future, graphene may be used in a wide variety of devices, but if these devices are ever going to be produced commercially, there needs to be much improvement in methods for growing high quality graphene. The purpose of this project was to fabricate graphene field effect transistors (FETs) to assess the quality of graphene grown through CVD on Cu and examine problems in the fabrication process.

Experimental Procedure:

The experimental procedure broke down into five main steps: (1) the preparation of the substrate, (2) the transfer of graphene from copper onto the substrate, (3) the patterning of electrodes onto the graphene, (4) the deposition of the back-gate metal, and (5) the characterization of the graphene.

A heavily doped Si wafer (n-type, <100>, 0.01-0.02 Ω-cm) was used as the substrate for the graphene FETs. The wafer had to be oxidized to have an oxide thickness of 90 nm so that the graphene would be visible on top of the oxide [1].

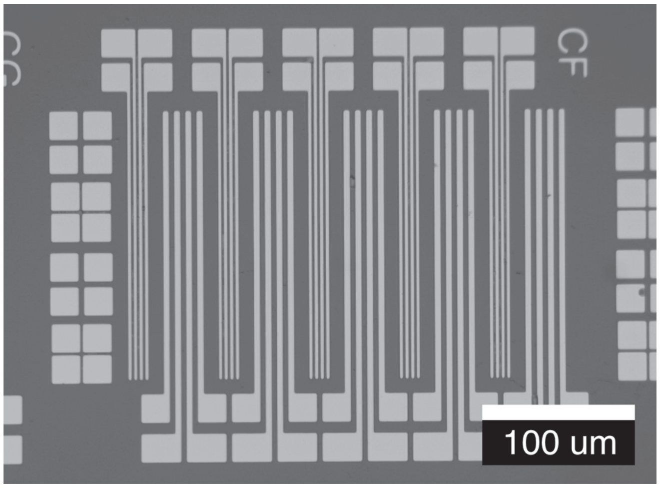

Figure 1: Electrode pattern; small fingers are 2 µm wide and large fingers are 4 µm wide.

Graphene was transferred from copper to the substrate through an electrochemical reaction. Poly(methyl methacrylate) (PMMA) was spun onto the copper sheet before hooking up the copper sheet to function as a cathode in a potassium hydroxide (KOH) bath with a steel electrode serving as the anode. Hydrogen gas forming on the surface of the copper lifted off the PMMA, with the graphene attached to its underside. This sheet of PMMA was then cleaned and scooped up with the substrate.

After removing the PMMA with remover PG and annealing the sample to clean the graphene, electrodes were patterned onto the surface of the graphene in a pattern that can be seen in Figure 1 through photolithography and evaporative metal deposition.

The final fabrication step was the deposition of the back-gate metal. The back-gate metal was deposited after stripping away the backside oxide with buffered oxide etch (BOE).

Characterization was done through use of a probe station and parameter analyzer. The goal was to use four-point-probe and transistor measurements, though in the end, only four-point-probe measurements were conducted.

Results and Conclusions:

Three main problems were encountered during fabrication: (1) the oxide had to have a specific thickness, (2) the transfer process caused the graphene to fold up on itself, as shown in Figures 2 and 3, and (3) the nickel electrodes adhered poorly to the graphene, as shown in Figure 4.

The first problem was addressed through using dry oxidation to make the oxide slightly thicker than desired and then using BOE to fine-tune the thickness of the oxide. The second problem was caused by remover PG attacking photoresist residue under the graphene during the PMMA removal step. This problem was addressed by changing the order of fabrication steps to allow for nanostrip cleaning directly before transfer to ensure that the surface of the substrate was clean. Given the limited amount of time for the research project, the third problem was not addressed although possible solutions have been formulated.

Due to the problems with fabrication, data was only successfully collected from a single device as the electrodes proved difficult to probe. The four-point-probe measurement suggested a sheet resistance of 7700 Ω/sq with very high probe contact resistances of 200 Ω per contact, and a nickel-graphene contact resistance of 5.38×10^{-4} Ω-cm^2. The measured sheet resistance was 20 times higher than expected, likely because of uneven contact between the nickel and graphene and discontinuities within the graphene sheet.

Three main ideas have been put forward to address the nickel-graphene adhesion problem in the future. First, the mask should be redesigned to have larger probe pads to make probing the devices easier. Second, new metals, such as platinum, should be experimented with as possible nickel substitutes. Finally, a reactive ion etching step might be done to etch the graphene into strips before patterning electrodes onto the surface so that contact pads can remain on the oxide with only fingers on the graphene. After this problem is addressed, more characterization needs to be done.

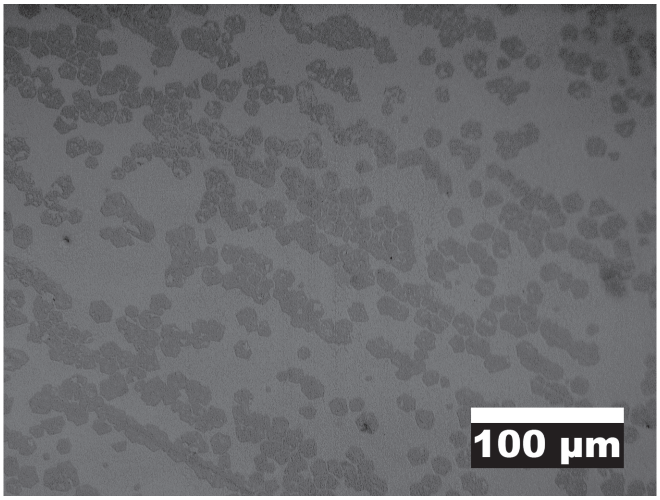

Figure 2: Graphene prior to PMMA removal.

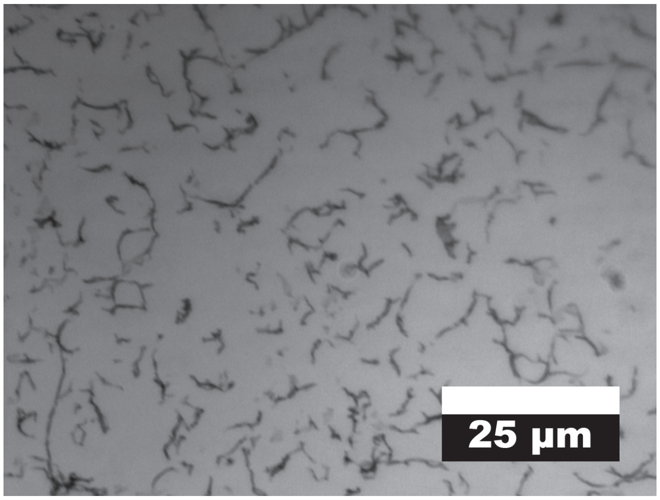

Figure 3: Graphene after PMMA removal.

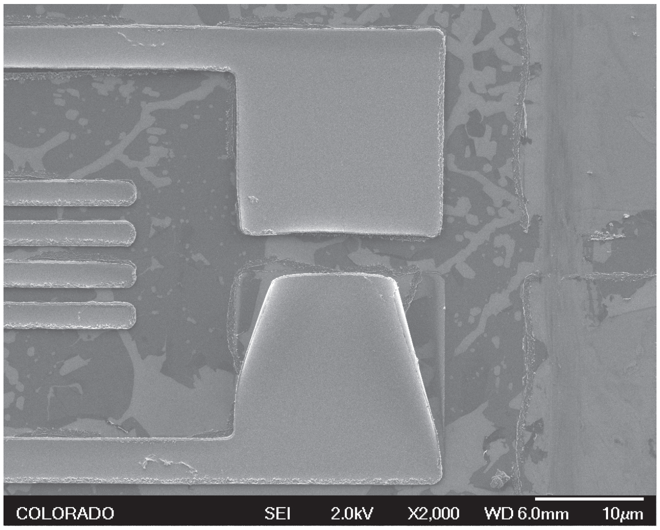

Figure 4: Nickel electrodes over graphene.

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References:

[1] P. Blake, et al., "Making Graphene Visible," Applied Physics Letters, 91, 063124, 2007.