# Characterization of Si-Nanowires for Biosensor Applications

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## Abstract and Introduction:

Silicon nanowire field effect transistors (Si NW FETs) are promising structures for the development of new biosensors due to their ability to directly translate interactions with target molecules into readable signals [1]. They are highly sensitive and selective and capable of real-time response and label-free detection. However there are challenges with stability and reproducibility in the development of such sensors due to the property changes over time of the thin gate dielectric when exposed to an electrolyte, low signal to noise ratio due to the small size of the NWs, and an increased role of surface effects.

In order to develop and to find the optimal dielectric passivation for Si NW sensors this project is focused on the investigation of the influence of an electrolyte liquid gate on the physical and electrical properties of the NW FETs covered with a thin silicon dioxide ($SiO_2$) passivation layer. Noise spectroscopy was employed to characterize the performance of the devices in the electrolyte and without it. This technique provides a number of advantages. Noise measurements allow for the determination of various kinetic parameters from experimental data gathered without time-varying external excitation.

In addition, data extracted from noise spectra contains information about structure performance, and quality of the samples, making noise spectroscopy a powerful tool for monitoring device state. Noise spectra were measured and analyzed for Si NW FETs of 500 nm width and a variety of lengths (2-16 $\mu$m) with a thin $SiO_2$ passivation layer (10 nm thickness) in air and phosphate buffered saline (PBS) at different liquid gate and back-gate voltages. Parameters of interest include the effects on threshold voltage and charging time of the device gate dielectric.

## Methods:

Drain voltage spectral density was measured for samples of varying nanowire length (2-16 $\mu$m) over a range of different applied back-gate voltages; first in air, then in PBS. A constant source-drain voltage of 100 mV was applied to the samples to ensure linear regime of operation. The noise spectra of the device were registered using a HP Spectra Analyzer after the output signal from the sample was passed through a low-noise

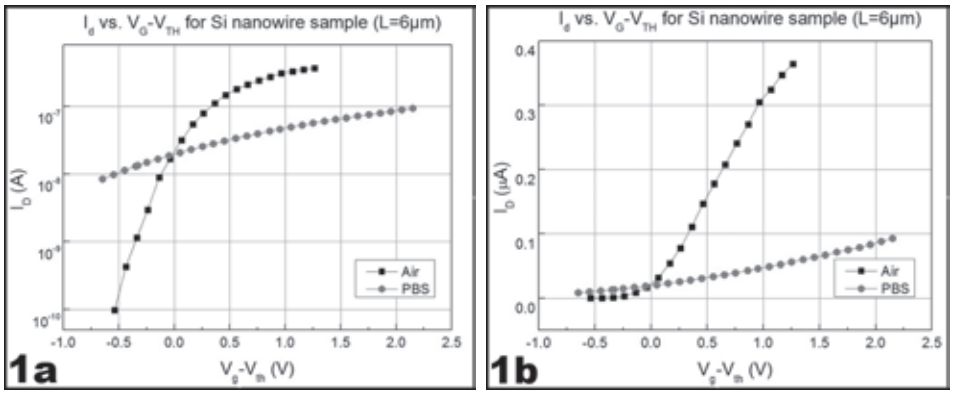


*Figure 1: Drain Current vs. $V_{GATE}$-$V_{THRESHOLD}$ for a 6 μm sample shown in (A) semi-log and (B) linear scale.*

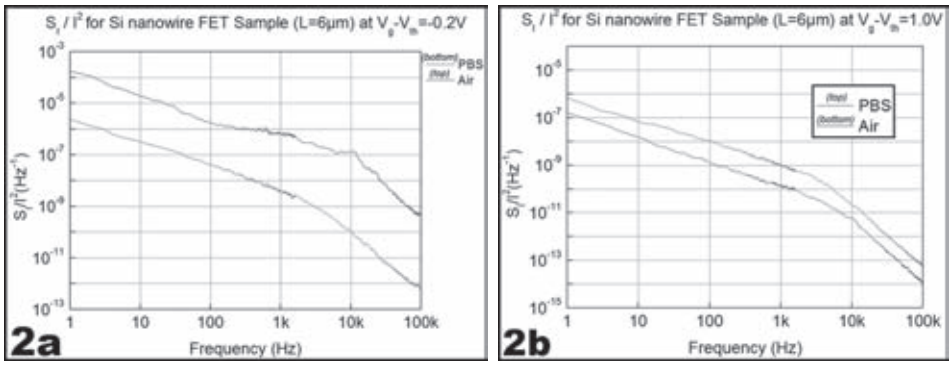


*Figure 2: Normalized Current Noise Spectral Density measured for a 6 μm sample in (A) the sub-threshold region and (B) above threshold voltage region.*

homemade amplifier with gain 100 dB. A custom program was designed to measure the drain current and spectra data. This data was then analyzed using OriginLab software to determine the effects of PBS on threshold voltage and the noise spectra. The current spectral density, $S_I$, was calculated using the measured voltage spectral density and the equivalent resistance of the measurement scheme.

## Results and Discussion:

The first parameter of interest of our device was the effects that PBS had on the samples' threshold voltages. Drain current in the samples was measured over a range of backgate voltages, and the transfer characteristics of the FETs were then plotted. Threshold voltage was calculated by applying a best fit approximation to the linear region of the curves. Figure 1 shows typical transfer characteristics measured for a sample of length 6 $\mu$m in (A) semi-log and (B) linear scales. From Figure 1A, it can be seen that the addition of PBS affects the sub-threshold current of the sample, and thus facilitates exchange between interface traps of the top dielectric with the channel of the Si NW FET in the sub-threshold region. Therefore, the interaction of the electrolyte with the nanowire FET structures results in changes of the state of the interface traps. Also, an increase in threshold voltage is registered when the sample is exposed to PBS, indicating a change in surface charge of the NW transistor.

Figure 2 shows normalized current spectral density, $S_I / I^2$, at (A) sub-threshold backgate voltage, $V_{bg} - V_{TH} = -0.2V$ and (B) above threshold voltage, $V_{bg} - V_{TH} = 1.0V$, measured in air and PBS. In the sub-threshold region, the normalized current spectral density of fluctuations in the device decreased when PBS was introduced to the sample. This decrease can be explained by the changing of the surface charge due to PBS and thus the charge state of traps in the sample's top dielectric and partly by increases in the sub-threshold current without a corresponding increase of the noise (Figure 1A).

Above the threshold voltage, submerging the sample in PBS appears to increase the amount of fluctuations in the sample. The lower value of the current at $V_{bg} - V_{TH} = 1.0V$ in PBS (see Figure 1B) only partially explains this behavior. If change in the number of charge carriers was the only cause, then the ratio of currents in air to PBS and the ratio of $S_I / I^2$ in PBS to air would be similar.

Figure 1B shows that the current in air is three times higher than the current in PBS at this voltage. However, $S_I / I^2$ at 100 Hz, is ten times greater in PBS than in air. Thus, the change in number of carriers is not the only factor influencing the change in noise level. We suggest that another component of this variation is a change in the mobility of the charge carriers due to a change in the behavior of the traps at the interface between the semiconductor and the top dielectric caused by the PBS.

## Conclusions and Future Directions:

It was shown that the exposing the nanowire samples to PBS not only affects the number of charge carriers, but also most likely results in a change in mobility of charge carriers. Further experiments need to be done to determine what other factors affect the stability and reliability of the samples working with the liquid gate. The next step will be to compare the properties of the Si NW FET samples passivated with different thin film dielectric layers in air and in PBS. Measurements will also be performed after exposing the samples to cell media for the development of neuron-nanowire FET hybrid structures.

## Acknowledgements:

I would like to thank Dr. Svetlana Vitusevich, Sergii Pud, and the rest of the Vitusevich lab for hosting me. Also, thank you to the NNIN iREU Program and the National Science Foundation for funding this experience.

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[1] "Silicon nanowire field-effect transistor-based biosensors for bio-medical diagnosis and cellular recording investigation"; Chen, K; Li, B; Chen, Y; Nanotoday (2011) 6, 131-154.

# Production of Solid State Spin Qubits

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## Introduction:

The focus of this project was to design and create an electron irradiation setup at The University of California, Santa Barbara (UCSB) to produce solid state spin quantum bits (qubits) in diamond and silicon carbide. Unlike the conventional bit, which is either 0 or 1, a qubit can be 0, 1, or any superposition of the two states. Quantum computing takes advantage of this property to perform some tasks, such as factoring and searching, much faster than conventional computers can. The setup designed during this project will allow efficient qubit engineering under precisely controlled conditions.

## The Qubits:

Solid state spin qubits have several advantages over current qubit technologies: they have long coherence times (~ 2 ms) at room temperature, are optically readable, are scalable as a system, and certain polytypes of silicon carbide can be integrated easily into silicon devices.

A solid state spin qubit consists of a crystal vacancy complex containing a localized electron density. The spin state of this density can be manipulated with microwave frequency magnetic field and the state is read out optically. In diamond, the qubit structure consists of an atomic vacancy adjacent to a substitutional nitrogen atom. In silicon carbide there are six qubit structures. Four of them are known to be divacancies in varying orientations. Figure 1 shows each qubit structure.

The preferred method for creating these atomic vacancies is electron irradiation. Electron irradiation gives even distribution of qubits and a relatively low level of unwanted crystal damage, but creation is inefficient. Only 0.1% of the nitrogen atoms in diamond samples become part of viable qubits, and every extra nitrogen atom interferes with qubit coherence. Currently, samples must be sent to third parties for processing where we have minimal control over irradiation conditions. By creating a facility to manufacture qubits ourselves, we hope to improve creation efficiency and engineer samples with controlled qubit densities, and higher qubit densities than have been made before.

## The Project:

To create these qubits, an irradiation setup was designed to interface with the UCSB free electron laser (FEL). The FEL's 5 MeV electron beam is diverted through the sample irradiation setup and into a beam dump. To protect the electron accelerator and eliminate scattering, the entire path of the beam must be under ultra-high vacuum conditions (UHV = $10^{-9}$ Torr). Because many materials outgas under

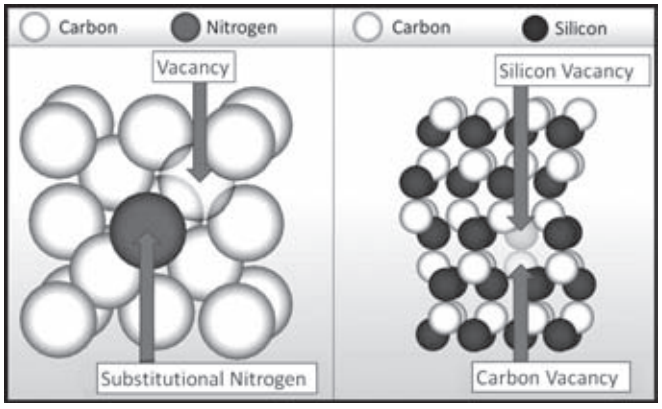


*Figure 1: Nitrogen vacancy center in diamond (left) and silicon carbide divacancy (right).*

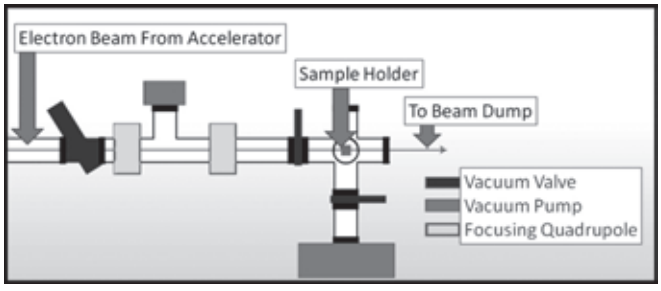


*Figure 2: The irradiation addition layout.*

UHV conditions, all parts in the vacuum, including sealing gaskets, must be metal. An estimated 9 W will be absorbed by the sample during irradiation so all parts of the system must withstand or dissipate this heat.

## The Design:

The final design met all of the challenges of the high energy beam, UHV environment, and more. For the safety of the electron accelerator, the irradiation addition was automatically isolated from the rest of the beamline in the event of a leak, and could be manually isolated in multiple sections for access and pumping. For efficiency, the addition used standard vacuum parts with the exception of the sample holder, and a small volume to pump down. Figure 2 shows the irradiation addition to the FEL facility. The sample holder was a 20 × 16 × 75 mm block of copper with five insets for samples on the front face. The holder was threaded onto a high-power ¾″ copper feedthrough that was attached to a linear-shift bellows mechanism to offer a 50 mm movement range.

The sample holder and beam were aligned using a 6 mm diameter calibration hole at the bottom of the holder while maximizing the current at the beam dump. When the system was aligned, the 7 mm spacing between samples allowed us to move between all five samples without breaking the vacuum. The calibration process also provided an electron flux measurement that could be used to calculate irradiation dose when the sample was in the beam. For heat conduction out of both faces of the samples, each was secured in its inset by a 4 mm thick copper faceplate and two bolts. Heat was drawn from the sample holder via the feedthrough which was water cooled outside the chamber for vacuum safety.

To reduce unnecessary heating there was a free path for the beam through the center of each faceplate and through the holder behind each inset. The first sample holder accommodated two 2.3 × 2.3 mm samples and three 3 × 3 mm samples, but the threaded attachment made installing other sample holders for future experiments simple.

Figure 3 shows the elements of the irradiation assembly and Figure 4 shows the finished sample holder.

## Conclusion and Future Work:

At this point the irradiation addition to the FEL is under construction. Several components required for the protection of the accelerator are being ordered. When completed, the setup will be used to study how different irradiation conditions affect resulting qubit quality.

## Acknowledgements:

This project would not have been possible without input and support from many individuals. The Awschalom Group provided tremendous feedback and assistance throughout the project. Engineer David Enyeart and Research Scientist Gerald Ramian, of the UCSB FEL staff, provided regular consultation on construction, acquiring parts, and interfacing to the beam. Professor Christopher Palmstrom provided input on the construction of UHV systems and considerations for the optimal design. And the NSF, NNIN REU Program, UCSB, DARPA, and the Air Force provided funding and facilities.

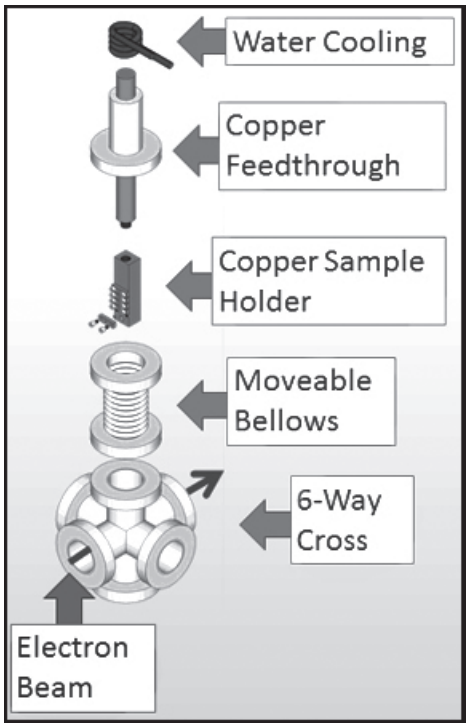


*Figure 3: The irradiation assembly.*

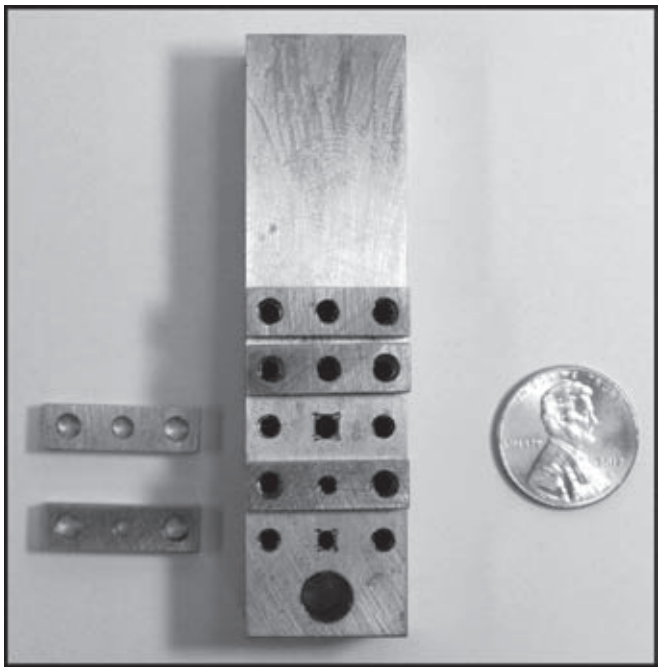

*Figure 4: The completed sample holder.*

# Fractal Electrodes

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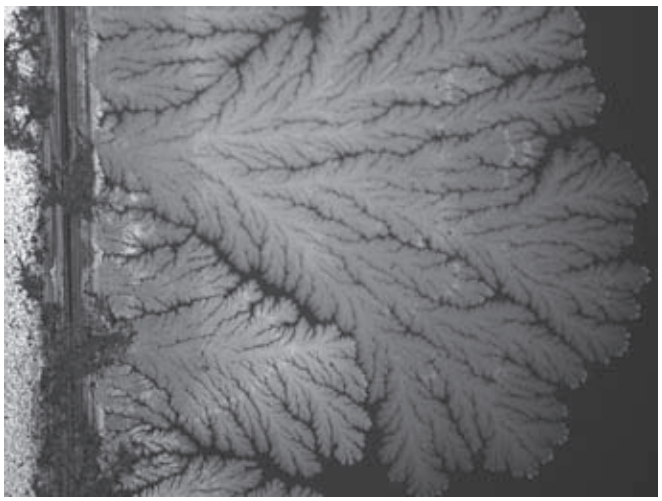

*Figure 1: A sample cathode. Dendrites are growing to the left as more silver ions reach the cathode. There are multiple layers of dendrites visible.*

## Abstract:

Fractal electrodes (dendrites) provide an opportunity to improve many electrical and optical areas including solar cells, sensors, and in the future, retinal replacements. They offer a unique ability to carry either information or charge with minimal resistance, while only covering a small fraction of surface area. These electrodes can be easily made by applying an electric field between an anode and cathode which causes the dendritic metal electrodeposit to form. One key characteristic of the fractal electrodes is the fractal dimension, which is used to describe non-Euclidean geometries. The purpose of this project was to determine the level of control that can be obtained through use of constant current and constant voltage during electrodeposit growth. Thin films of silver were deposited on slides via thermal evaporation. The mask used provided channels between the silver electrodes in which the dendrites could grow. The dendrites, as seen in Figure 1, were then imaged and processed to determine their fractal dimension. It was found that the fractal dimension decreases with an increase in field, in both constant current and voltage trials. The data confirms that a stronger field leads to more one dimensional growth.

## Experimental Procedure:

Silver (Ag) deposition was carried out using thermal vapor deposition. The chamber of the Cressington was vacuumed down to $3 \times 10^{-6}$ mbar. Between 47 and 50 nm of Ag was deposited on the glass slide. Channels to carry out the electrodeposition were created with a mask of Mylar tape. Each channel was probed using an Agilent 4155C semiconductor parameter analyzer. Either constant voltage or constant current were applied across the channel for various amounts of time to produce the dendrites. Once the dendrites were grown, an Axiophot microscope was used to produce the images. Three images were taken for each dendrite. The fractal dimension was calculated in MatLab using a box counting approximation. Results were then averaged for the three images to calculate the fractal dimension for the trial. Experiments at 2 volts and 25 $\mu$A were tested from two minutes to ten minutes every minute. For 5 volts, 35 $\mu$A, and 50 $\mu$A trials, the times tested went from 90 seconds to 240 seconds every 30 seconds. And the higher field trials, 10 volts and 75 $\mu$A, were tested from 30 seconds to 60 seconds in ten second intervals.

## Results and Conclusions:

As seen in Figure 2, the higher the voltage, the lower the fractal dimension tended to be. Similarly, when the current was held constant, higher currents lead to lower fractal dimensions. For the constant voltage trials, Figure 2, the data was not scattered, with the exception of one outlier. The constant current data was much more varied, as seen in Figure 3.

There are many possible areas of error, especially during the probing. One example is how far the probes were from the channel. This varied from sample to sample. Another potential reason could be the contact of the probe to the deposited silver. If the probe was pressing too hard, it could scrape off the silver, which would increase the resistance. On the other hand, if the probe was not pressed hard enough, then the probe would not be making good contact with the silver. For more exact data, these problems would need to be addressed, but a strong negative trend was found.

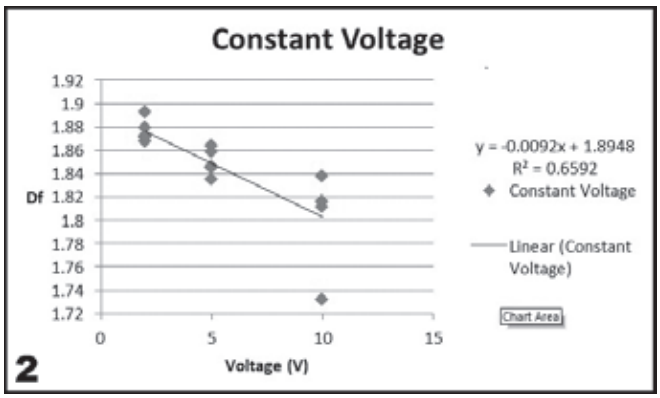


*Figure 2: Fractal dimension for each constant voltage trial. The plot points to a strong downward trend.*

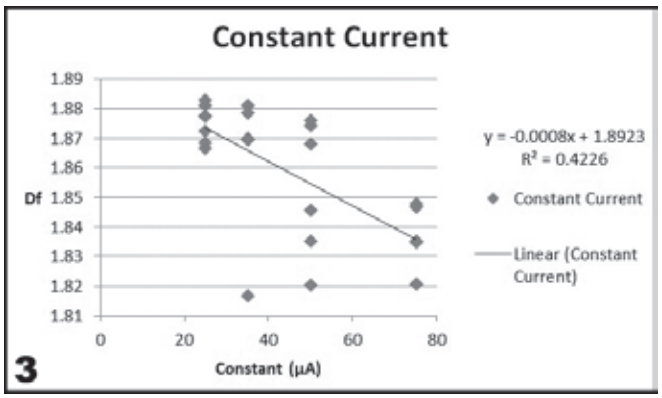


*Figure 3: Fractal dimension for each constant current trial. While data is more scattered than the constant voltage trials, the same trend is prominent.*

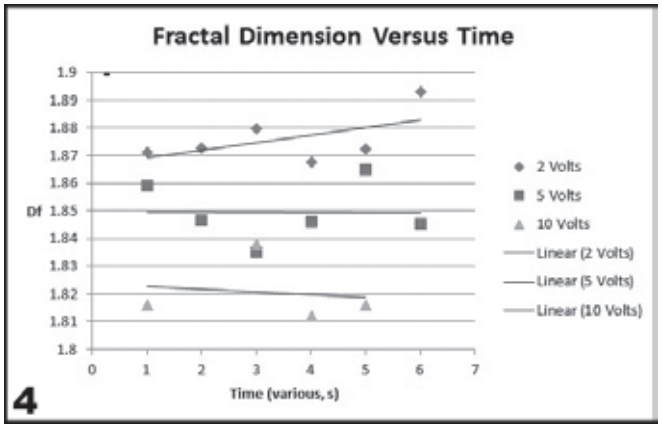


*Figure 4: Fractal dimension versus time. The time scales vary depending on the voltage. For 2 volts, the times tested were every minute, for 5 volts every 30 seconds, and 10 volts was every 10 sec.*

For each voltage and current tested, the fractal dimension to time relationship was tested. Figure 4 shows this relationship for the constant voltage trials only. It was obvious that no clear trend existed with respect to time. The dendrites were not growing far enough to cause any difference compared to the randomness of the sampling. If more exact methods were used, it would make sense for the fractal dimension to have a slight decrease with respect to time.

## Future Work:

The data gotten from the above experimental procedure is useful for silver electrodeposits grown in de-ionized water at room temperature. However, if any of these constraints change, more testing will need to be done. The effect of temperature on dendrite growth would also seem to be a more sensitive way of controlling the formation.

## Acknowledgments:

I would like acknowledge my principal investigator, Dr. Michael Kozicki, and my mentor, Ankitha Chandran, for their time and for everything they taught me. Thanks also to my site director, Dr. Trevor Thornton. Finally, thank you to the National Nanotechnology Infrastructure Network Research Experience for Undergraduates Program, the National Science Foundation, and the Center for Solid State Electronics Research at Arizona State University for providing the opportunity and funding for this amazing experience.

# Improving Superconducting Resonators for use in Quantum Computing

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## Abstract:

Superconducting coplanar waveguides (CPWs) are essential elements in building quantum computers [1] and in single photon detectors for astrophysics [2]. Reducing energy loss in these waveguides is critical to improving their performance. One source of energy loss in coplanar waveguides arises from parasitic coupling to unwanted electromagnetic modes that occur where there are asymmetries or discontinuities in the circuit layout. The effect of these asymmetries and discontinuities can be minimized by adding additional wiring ("crossovers") to the waveguide geometry. However, the dielectric materials that serve as structural supports for the crossovers add additional loss through different mechanisms. We will discuss a method of fabricating crossover wiring in the form of freestanding air bridges, which will still suppress unwanted modes, but will not use a lossy dielectric for structural support.

## Background:

Quantum computation relies on bits of information being stored as excitations in a quantum mechanical object. Unfortunately, these excitations decay as the object losses energy to its environment. This may be represented as a classical "bit" of information spontaneously changing from a "1" to a "0". The loss of energy/information is one of the biggest obstacles facing all of the proposed quantum computation architectures. Thus, reducing sources of energy loss is vital to building a quantum computer.

Energy loss occurs when moving and storing information in a superconducting circuit. A coplanar waveguide is a type of microwave transmission line that is used to move information in a quantum circuit, similar to how wires move information in an integrated circuit. A waveguide with boundary conditions such as electrical opens or shorts on both of its ends will resonate at a fundamental frequency that is defined by the length of the CPW. These resonators are used to store information for later retrieval as well as to aid in both the communication and isolation of qubits.

The CPW consists of a conducting plane lying on a dielectric substrate. The conducting plane is divided into three sections consisting of a center conductor surrounded on either side by ground planes (Figure 1). This geometry supports several electromagnetic modes, two of which are the desired even mode and the parasitic odd mode. The odd mode is a source of energy loss for the even mode, but it can be suppressed using a superconducting strip to force the ground planes to the same electrical potential. Currently the superconducting strip is supported by a dielectric, hydrogen terminated amorphous silicon. While this crossover method suppresses the odd mode, the supporting dielectric introduces a different source of loss not described here.

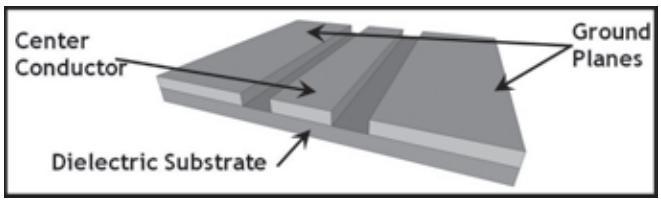


*Figure 1: Coplanar Waveguide (CPW).*

## Methods:

A research group in the Netherlands has developed freestanding air bridges (Figure 2). First, they spin a 3 $\mu$m layer of positive photoresist over a CPW. A lithography step leaves behind a rectangular bar of resist covering the CPW.

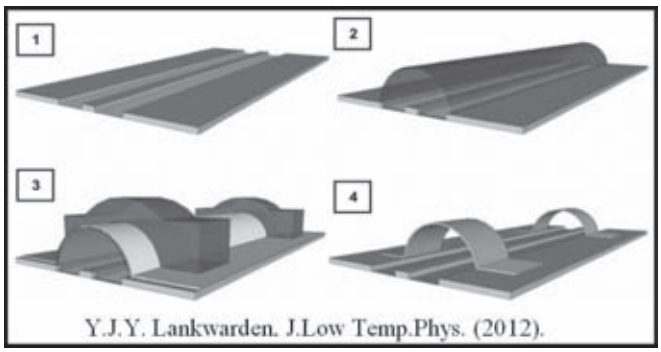


*Figure 2: Air bridge fabrication process.*

Heating the bar of resist above its glass transition temperature results in an arched shape, which serves as scaffolding for the air bridges. A thin layer of aluminum is deposited, followed by another layer of resist. A second lithography step covers the aluminum at the bridge locations. An etching step removes excess aluminum, and all of the remaining scaffolding resist is removed leaving behind freestanding air bridges.

This method could prove less lossy than the current crossover method, because it does not require a dielectric for support. The air bridge method also reduces the number of fabrication steps, which should improve device performance. Since the qubits used in these circuits are temperature sensitive devices, it is imperative that the resist have a low reflow temperature, and can be spun on at ~ 3 $\mu$m to set the height of the air bridges. SPR220-3.0 photoresist can be spun on at 3 $\mu$m, but its reflow temperatures are not known, so separate samples of SPR220-3.0 were baked at temperatures in the range 115°C-155°C for three minutes each. The reflowed resist was analyzed using profilometery and atomic force microscopy (AFM).

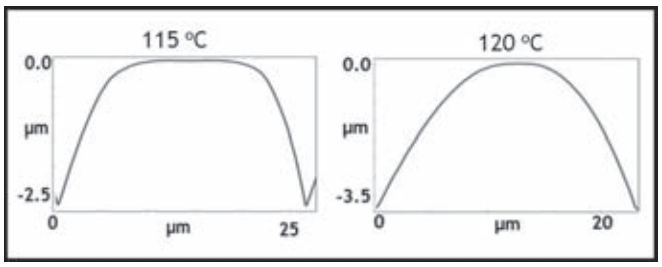


*Figure 3: SPR220-3.0 photoresist baked at the indicated temperature for three minutes.*

## Results and Conclusions:

The results show edge rounding at all temperatures (Figure 3), however at 120°C, a clear semi cylindrical shape appeared. Temperature data was taken up to 155°C, but after 120°C, there was no significant change in the shape of the photoresist. Since the profilometer has a relatively large 12 $\mu$m tip radius, we verified the above results using AFM images (not shown) of before and after reflow.

We have discussed a method of suppressing the odd CPW mode that does not rely on a lossy dielectric for support. The reflow characteristics of SPR220-3.0 photoresist were characterized, and the reflow temperature of SPR220-3.0 was determined to be 120°C. This low reflow temperature should save our sensitive devices from thermal degradation.

After fabricating the air bridges, resonators will be used to compare the losses between air bridges and crossovers. This will improve the quality of our CPW circuit and add robustness to the architecture of superconducting quantum computers.

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# The Effects of Surface Passivation on Trap Levels in Silicon Nanocrystals

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## Introduction:

Silicon nanocrystals (Si-NC) systems have a wide variety of applications due to their optical properties, and their growth can be easily incorporated into Si fabrication methods already established in industry, making Si-NCs an attractive alternative to bulk Si. Recent developments have allowed for the synthesis of Si-NCs that are resistant to oxidation through surface passivation [1]. However, the effects of surface passivation on the electronic properties of Si-NCs remain unknown. With this in mind, our research focused on the investigation of trap levels in Si-NCs and the effects of passivation on these traps.

## Experimental Details:

The Si-NCs were created using non-thermal plasma synthesis with both $SiH_4$ and $SF_6$ gas in order to produce H and F terminated Si-NCs. Details on Si-NCs and passivated Si-NCs growth are described by Pi, et al. [2], and Liptak, et al. [1], respectively. Metal-oxide-semiconductor (MOS) capacitors were fabricated by annealing RTA cleaned n-type Si <100> in a $O_2$ ambient in order to create a thin $SiO_2$ interface, followed by the deposition of Si-NCs on the $SiO_2$ layer.

In order to optimize our measurements, we then utilized atomic layer depostion (ALD) to deposit a high-κ dielectric ($HfO_2$) layer on top of the Si-NCs, and finished by evaporating aluminum back and gate contacts. We fabricated devices with no Si-NCs (for control), a 30-second deposition Si-NCs layer, and a one-minute deposition Si-NCs layer for both bare Si-NCs and surface passivated Si-NCs samples. A topological overview of the device structure can be seen in Figure 1.

The trap centers of our fabricated MOS structures were then investigated using capacitance-voltage (C-V) profiling and deep level transient spectroscopy (DLTS) in order to confirm the presence of traps as well as to characterize the energy level and trap cross-section of these trap centers. The C-V profiles were acquired at different frequencies of 200, 50, and 10 kHz and the DLTS data was acquired using a temperature range of 35K-420K and a rate window of approximately 16 $s^{-1}$.

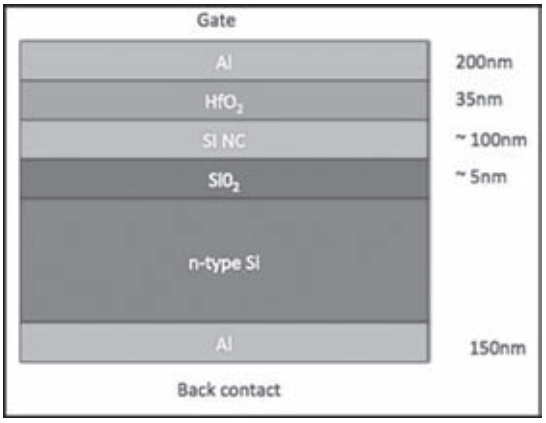


*Figure 1: Cross-sectional side view of the fabricated MOS-capacitors with embedded Si-NCs. The approximate thickness of each layer is shown at the right of the corresponding layer.*

## Results:

The C-V profiles of the samples (not shown), suggest the presence of trap levels in a number of ways: (1) The decrease in accumulation in both the bare and passivated Si-NCs samples indicated the presence of majority traps; (2) Stretchout indicated a greater number of trap levels in the bare and passivated Si-NCs samples; (3) The decrease in depletion in both the bare and passivated Si-NCs samples suggested a higher concentration of interface and majority trap levels; and (4) A greater change in the depletion capacitance was observed for the bare and passivated Si-NCs samples than for the control sample, indicating an increase in interface state density. It is also worth noting that the change in depletion capacitance was greater in the passivated samples.

The C-V measurements also demonstrated hysteresis in all samples for all profiling frequencies, as can be seen in Figure 2. The negative shift of approximately 0.5 V in the down trace of all the measurements is consistent with previously observed values by Kwon, et al., and this memory effect confirms the presence of Si-NCs in the samples [3].

The DLTS measurements are shown in Figure 3 and the trap levels found are summarized in Table 1. These results show that the trap levels found in

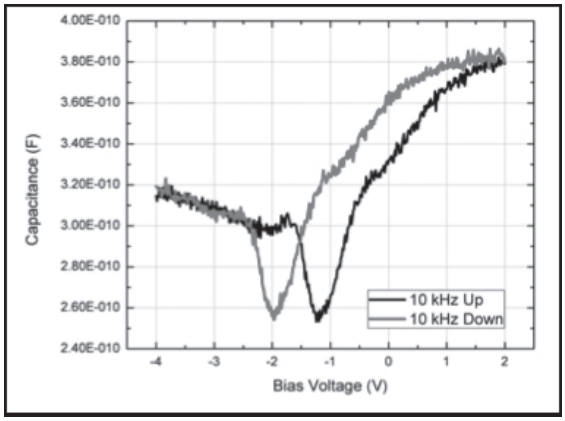


*Figure 2, above left: C-V profile shows the hysteresis profile for a 10 kHz scan of the passivated sample.*

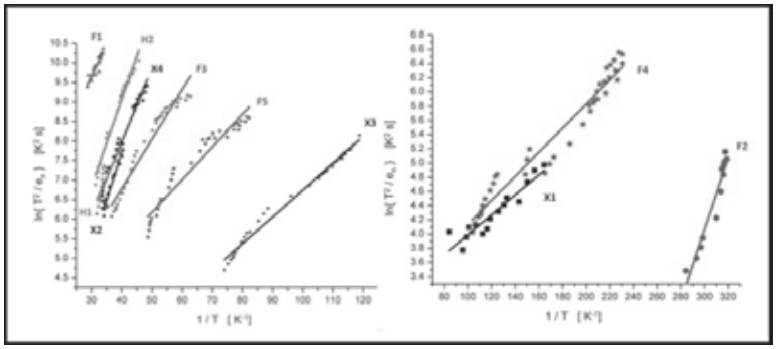

*Figure 3, above right: Arrhenius plots of our DLTS measurements show the presence of multiple traps levels. Each trap is labeled and more information can be found in Table 1.*

*Table 1, at right: List of the corresponding activation energy, capture cross-sections and temperature peaks for the trap levels found.*

| Control | | | |
|---|---|---|---|
| Trap | E (ev) | σ (cm²) | Peak (K) |
| X1 | 0.01 | $4.1x10^{-21}$ | 60 |
| X2 | 0.39 | $7.4x10^{-18}$ | 270 |
| X3 | 0.07 | $3.5x10^{-22}$ | 100 |
| X4 | 0.19 | $4.5x10^{-22}$ | 270 |

| Bare Si-NCs | | | |
|---|---|---|---|
| Trap | E (ev) | σ (cm²) | Peak (K) |
| H1 | -0.53 | $1.7x10^{-17}$ | 270 |
| H2 | 0.22 | $4.4x10^{-22}$ | 290 |

| Passivated Si-NCs | | | |
|---|---|---|---|
| Trap | E (ev) | σ (cm²) | Peak (K) |
| F1 | -0.16 | $4.0x10^{-20}$ | 350 |
| F2 | 0.05 | $2.1x10^{-17}$ | 40 |
| F3 | 0.13 | $1.6x10^{-21}$ | 230 |
| F4 | 0.02 | $3.5x10^{-22}$ | 60 |
| F5 | -0.08 | $2.3x10^{-21}$ | 170 |

our bare Si-NCs samples are not consistent with previously reported values by Souifi, et al. [4] and Kwon, et al. [3], which can be attributed to different Si-NCs growing methods. The traps found also have capture cross-section orders of magnitude smaller than expected, which has been previously observed and attributed to charge tunneling into the Si-NCs and a lower density of states at the Si-NCs by Antonova, et al. [5].

Overall, surface passivation appears to remove deep level traps in Si-NCs while creating shallow level traps for both majority and minority carriers. Considering than an F-terminated Si surface oxidizes much faster than an H-terminated Si surface [6], the removal of deep level traps in Si-NCs by surface passivation supports proposed theories that deep level traps in Si-NCs are caused by hydrogen dangling bonds [7]. However, not enough data has been collected to make any serious assessment and further research is needed to; (1) confirm the validity of the observed trap levels, and (2) correlate growth parameters with observed trap levels.

## Acknowledgements:

A special thanks to Prof. Stephen Campbell and Dr. Richard Liptak for their continued mentorship and support. This research opportunity would have also been impossible without funding from the NSF and National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, the help of Prof. Douglas Ernie, and the facilities of the Electrical and Computer Engineering Department, University of Minnesota.

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# Self-Organized Nanostructural Pattern Formation under Ion Beam Irradiation

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## Abstract:

Ion bombardment is a diverse laboratory technique with many applications including reactive ion etching, focused ion beam milling, ion implantation, sputter deposition, and ion beam characterization techniques such as Rutherford backscattering spectrometry (RBS). Of particular interest are the nano-topologies that form under the presence of ion irradiation. Periodic nanoscale ripples, dots, and high-aspect ratio structures can self-organize under ion bombardment. However, the relative importance of various mechanisms that underlie the self-organization process are poorly understood.

This project aimed to investigate the importance of ion beam-injected stress as a mechanism influencing the dynamics of nanoscale ripples. It has previously been observed that ripples will propagate along the surface of certain materials during ion bombardment, and a recently-developed theory attributes this phenomenon to beam-injected stress. Our study aimed to test this theory by quantitatively measuring ripple propagation velocity at a variety of incidence angles for comparison with the functional form of velocity vs. angle predicted by theory. A 30 keV $Ga^+$ focused ion beam was used to irradiate Si <001>. *In situ* scanning electron microscopy (SEM) was used to directly record the ripple dynamics.

Additionally, a methodology for measuring the propagation of ripples with respect to fluence (ions•$cm^{-2}$) was developed and preliminary measurements were taken.

## Introduction:

There has been much attention granted to self-organized nanostructures that propagate under the presence of ion bombardment [1]. Nanoscale features at and below 100 nm have been shown to form under both focused and unfocused ion beams, a process known as "sputter patterning." In a recent study, a regular array of nanodots with diameters as small as 7 nm were fabricated [2]. However, there is little understanding on how to control the ion induced self-organization process. A cohesive theory by which we can understand the governing mechanisms of ion induced self-organization could lead to a high level of control and manipulation of nano-pattern formation.

In this work, we investigated the propagation velocity at which nano-ripples propagated along the surface of Si <001> under the raster of a focused ion beam. Parallel mode ripples were observed to propagate in a direction anti-parallel to the incoming gallium ions.

Note, the term "propagation velocity" used in this report does not refer to the traditional concept of velocity. Rather, "propagation velocity" was measured in $^{nm}/_{fluence}$, i.e. how far a ripple would propagate under a given amount of ion impingement.

## Experimental Procedure:

A 30 keV beam of focused $Ga^+$ ions was produced using an NVision 40 Dual Beam focused ion beam (FIB) outfitted for *in situ* SEM. FIB and SEM guns were fixed at an angle $\Theta = 54°$ from each other, while the specimen stage had the freedom to tilt. The angle between the specimen stage and the FIB gun is denoted $\Theta_{FIB}$ and was held constant at 30°. Although we were ultimately interested in varying the angles of incidence, $\Theta_{FIB}$ was held constant while beam current, dwell time and other tool specific parameters were optimized. Beam currents of 80 pA and 150 pA were utilized to expose a 100 $\mu m^2$ area of p-type Si <001>. We minimized dwell time, set pixel overlap to 53%, and passed the ion beam over the exposed area many times, thereby approximating uniform radiation. This was done to ensure ripples were not directly written by the FIB.

Real-time Fast Fourier Transform was used to observe the evolution of periodicity while post-mortem Fast Fourier Transform was used to ascertain final periodicity of the ripples. In order to measure propagation velocity, measurements were made on how long it took for the Raith FIB software to execute one exposure loop. Using this metric, we correlated the amount of ions impinging on the surface between SEM frames.

## Results and Conclusions:

Figure 1 exhibits the relevance of dwell time. At sub-microsecond dwell times (1a), nanoscale ripples were apparent. As we increased dwell time, the ion beam was able to mill deeper into the surface, thereby directly writing nano-topologies. Dwell time should therefore be minimized in order to ensure that features are not directly written onto the surface.

*In situ* SEM was employed to record the evolution of ripples shown in Figure 2. We incrementally increased the total fluence, measuring the time to deliver the total fluence. Using this trend, we correlated the amount of ions impinging the surface between video frames and obtained a preliminary propagation velocity of 35.8 nm/$10^{17}$ ions•$cm^{-2}$ anti-parallel to the beam direction. This falls within an order of magnitude reported by [3] earlier this year.

It has been observed that there are inconsistencies in the functioning of the Raith software, and so further characterization of the ion flux is required to ensure repeatability of the metric.

## Future Work:

Obtaining the measure for propagation velocity requires further characterization. Once fully characterized, measurements will be used in comparison to what theory predicts. With the aid of a verified theory, we hope to research more complex material systems and nanostructures.


## Acknowledgements:

Prof. Michael J. Aziz, Joy C. Perkinson, Nicholas Antoniou, National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, National Science Foundation.


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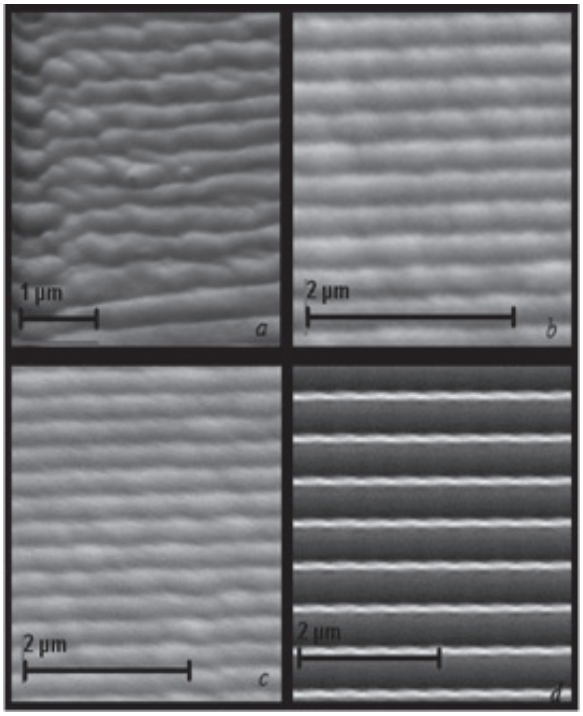


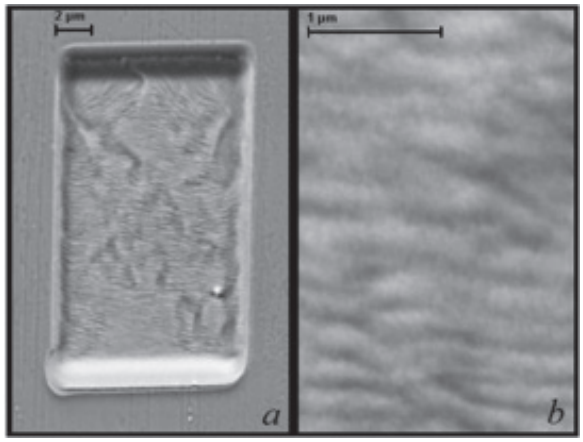


*Figure 1, top: Dwell Time varied: 0.1 µs (a), 6.4 µs (b), 12.8 µs (c), 25.6 µs (d). Scale bar index: 1 µm (a), 2 µm (b), 2 µm (c), 2 µm (d).*

*Figure 2, bottom: Post-ion bombardement: a. 11.12 µm × 19.49 µm milled area, magnification 2.03 kx. b. High magnification (15.05 kx) of nanoscale ripples. Scale bar index: 2 µm (a), 1 µm (b).*

# Cryoelectronic Characterization of Organic Molecules

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**Abstract:**

The temperature dependence of electronic properties of conducting and semi-conducting materials is a well-studied phenomenon, with many interesting effects in low temperature ranges. This project sought to develop a method by which the temperature dependence of capacitance of gold on glass or sapphire inter-digitated capacitors could be characterized, in addition to their inherent frequency dependence. The purpose of this was to establish a reference capacitance for each substrate, such that the capacitance of subsequently deposited or grown organic monolayers could be calculated independently of inherent capacitance via subtraction of the coated samples' values from the reference values. This is especially pertinent in the lower temperature ranges (sub 100K) as unusual effects have been observed previously, especially with ferroelectric materials. The capacitors were first fabricated via photolithography, gold deposition, and liftoff processes in the cleanroom. Afterwards, their capacitance was measured across a wide range of temperature and frequency, from 50K to 300K and 20 Hz to 2 MHz respectively.

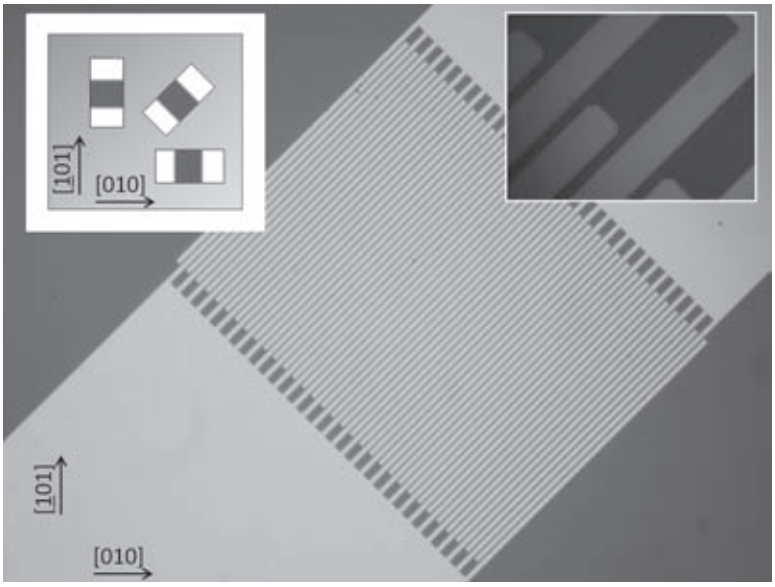


*Figure 1: Structure of the interdigitated capacitors and the three orientations.*

With referencing complete, the samples underwent oxygen plasma cleaning, followed by silinization in an inert atmosphere with octyltrichlorosilane under various pressures and concentrations of the reagent to yield organic monolayers on the substrate surface. The presence of monolayers was verified via contact angle measurements. Finally, the capacitances of the newly coated substrates were measured in the same fashion as the references and their results compared. For octyltrichlorosilane, no noticeable difference in capacitance was measured.

## Experimental Procedure:

Interdigitated capacitors of three orientations made of gold were initially fabricated in the cleanroom. The capacitors were patterned onto glass and sapphire substrates and exposed by contact lithography for 4.7 seconds. The metal was then sputtered onto the samples under reduced pressure. The purpose of the three orientations was to determine the best position for perpendicular deposition. Liftoff was performed outside the cleanroom in acetone under sonication. Each "finger" of the capacitor was approximately 10 $\mu$m wide and separated by 5 $\mu$m. Afterwards, one orientation of the capacitor was bonded to a probe and the capacitance was measured under varying temperature and frequency; 50K-300K and 20 Hz to 2 MHz. This was repeated for the other two orientations.

After a reference capacitance had been established for the capacitors, they underwent oxygen plasma cleaning in order to provide a clean surface for subsequent silinization. The silinization process entailed leaving the substrate in an enclosed system with liquid octyltrichlorosilane under reduced pressure for one hour. Contact angle measurements were performed before and after silinization to verify deposition on the substrate surface. Measured values before silinization were approximately 0 to 5°, and post silinization values ranged from 90 to 110°, suggesting deposition of mono and bi layers. The capacitance for the newly silinized samples was measured in the same manner as the reference samples.

The results were compared and no noticeable difference was observed between the silinized and reference sample.

## Results and Discussion:

As stated previously, this project sought to develop a process by which the electrical properties, the dielectric constant specifically, of various organic molecules could be measured and calculated. Several issues had to be addressed in order to optimize the process, namely fabrication defects, short circuits, and adhesion problems. Despite the relatively large scale of the structures, the samples demonstrated extraordinary sensitivity to fabrication parameters such as exposure and development times. Even the best samples were still prone to developing defects during the liftoff stage, where a small amount of residual gold could result in a short circuit in the capacitor. Finally, bonding certain samples to the probe was problematic due to the poor adhesion between the bonding wire and the metal. This issue was resolved through creative positioning of the bonding wire and the use of conducting paint as a glue to assist bonding. The final remaining issue is whether or not this process is sensitive enough to detect differences between reference and silinized samples. Due to time limitations, only octyltrichlorosilane was measured, and more alkylated silane derivatives need to be tested before a conclusive result can be obtained.

## Acknowledgements:

The author would like to thank Professor Roger Wördenweber, Tino Ehlig, Thomas Grellmann, Eugen Hollmann, and Kirill Greben for their assistance and kindness both in and out of lab. Additionally, this project would not have been possible without the National Nanotechnology Infrastructure Network International Research Experience for Undergraduates (NNIN iREU) Program and the generosity of the National Science Foundation.

# Construction of a Modulated Potential Superlattice

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## Abstract:

A superlattice is a periodic structure composed of at least two different materials and may be used to change the band structure of a semiconductor. We studied the construction of a periodically modulated potential superlattice (with a 60-200 nm period) that we predicted would allow microscale manipulation of electron transport properties in graphene. Using electron beam lithography and reactive ion etching followed by metal deposition, we constructed complete 200 nm and 140 nm period superlattices. We also pushed the size limitations of our process to lay ground work for 100 nm and 60 nm period superlattices.

## Introduction:

The study of graphene's electrical properties has been and continues to be a popular field of research. Our particular interest was in the prediction that by applying the correct periodic potential, electrons could be made to move freely in graphene without scattering. We investigated the parameters necessary to produce such a potential.

Because the mean free path of electrons in graphene is on the order of tens to hundreds of nanometers, the periodicity of the potential must be around a few tens of nanometers to affect the movement of electrons. The way we chose to attempt to create this potential was by constructing a superlattice (see Figure 1). This superlattice alternated gold with silicon oxide. Applying a voltage to the gold created a potential and the spaces of insolating silicon oxide limited the size of the potential. We chose to pursue this process by using a top down approach.

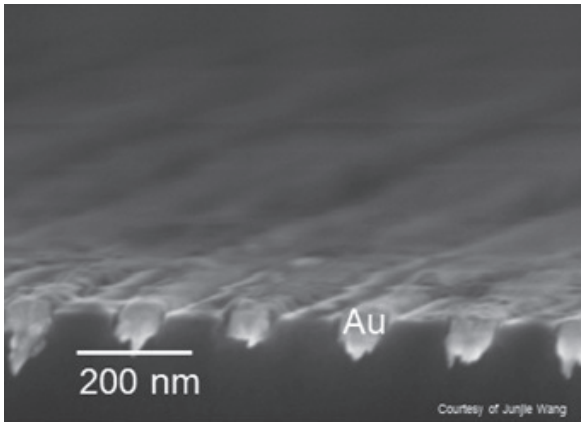


*Figure 1: Superlattice.*

## Methods:

We began with a typical silicon wafer covered in 290 nm of thermally grown silicon oxide. We needed to etch the surface to create a space that would be filled with gold. The patterning of the surface prior to etching was done using electron beam lithography. We chose the resist Zep 520a because of its resistance to etching and its resolution.

One-hundred to about fifty nanometer trenches alternating with same-sized spaces were easily achieved using a Vistec 5200 and a standard develop procedure of 180 seconds in n-amyl acetate, followed by thirty seconds in 8:1 MIBK to IPA, and another thirty seconds in straight IPA to stop the develop process. However, as we approached the 30 nm mark out, the electron beam dose went straight from under-exposed to over-exposed (see Figures 2 and 3). This appeared to be because of proximity effect damage on the adjacent resist walls.

When the electrons were shot at the resist during exposure they broke the polymer chains and at the same time excited secondary electrons. Most of these secondary electrons were much less energetic and, especially at high accelerating voltages (we used 100kV), did not travel far laterally — only a few nanometers. These secondary electrons thus contributed mostly to exposing the pattern in the resist. There were, however, some fast secondary electrons (possibly caused by backscattering) that traveled much further and caused infidelity in the pattern.

This collateral damage became increasingly important as the patterns being written became smaller and closer together. Because of this, as our structures got closer and closer together, the damage to the thin walls of the trenches became catastrophic to the point where our somewhat harsh develop procedure removed not only the parts that we wanted to expose, but also large parts of the adjacent resist that had been damaged by stray electrons.

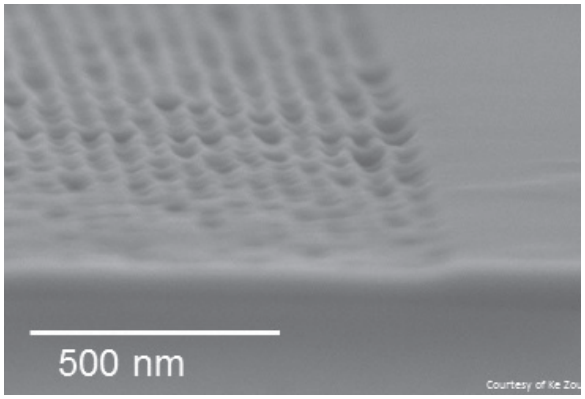


*Figure 2: Underexposed line space pattern.*

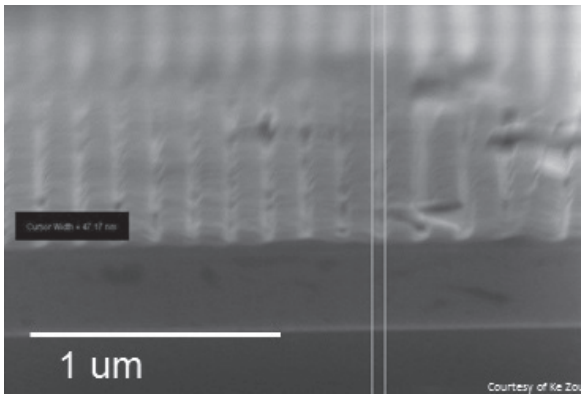


*Figure 3: Overexposed line space pattern.*

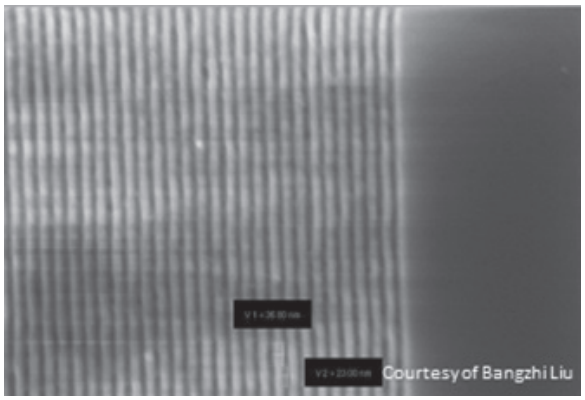


*Figure 4: Cold develop lines.*

In order to make this process work, we needed a develop process that was gentle enough to leave the damaged resist, while still removing the exposed resist. A shorter develop time (thirty seconds to a minute and a half) was attempted, but without success. The shorter develop time had to be combined with a colder develop temperature. Because of the kinetics of the removal process, it was possible to make the developer cool enough (down to ~ 4°C) that it removed the normally exposed resist while leaving intact the damaged/partially exposed sides (see Figure 4). In order to make this work, it was necessary to increase the dose to a much higher level.

Success using a similar technique was achieved by Mr. Frazier Mork, as reported at the 2012 NNIN REU Convocation [1]. Using a cold develop and a 30 nm thick resist, as well as dose correction, his group achieved ~ 20 nm line spacing.

## Conclusions:

Using our process, we believe that it would be difficult to decrease the resist thickness any more than our 140 nm — which we achieved using 1:1 ratio anisole to zep — because the pattern must then survive etching. We etched with a combination of $CF_4$ and $CHF_3$. Metal deposition may be done with regular electron beam evaporation, and finally for lift off, we used warm remover PG with sonication. (Acetone would also work though it is less aggressive.) We achieved a successful superlattice (see Figure 1) that was too large for experimentation, although it did demonstrate the method. Using the cold develop method, we demonstrated the technique's viability for use in smaller structures.

## Acknowledgements:

Thanks to Professor Jun Zhu for letting me work in her lab as well as Ke Zou and Jing Li for working with me. I would also like to thank Junjie Wang for his help and advice, and the Nanofab staff at Penn State for entertaining my numerous questions. Finally, thanks to the NNIN REU Program and the NSF for funding and making this research possible.

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# Optical Characterization and Solar Cell Application of GaAs/$Al_{0.8}Ga_{0.2}As$ Quantum Wells

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## Abstract:

The theoretical efficiency limit of current single p-n junction solar cells is ~ 33%. Intermediate energy states in the solar cell's band gap allow low energy photons to induce carrier excitations, increasing efficiency [1]. Quantum well solar cells contain such states, but carriers excited in the barrier often relax into the wells where they become trapped and recombine, reducing efficiency. Because of a large momentum difference, the use of an indirect material may suppress carrier trapping and recombination, resulting in greater solar cell efficiency. Using GaAs/$Al_{0.8}Ga_{0.2}As$ quantum well structures, we find that carriers trapped in our quantum wells cannot easily escape, and current measurements show no significant recombination among carriers generated in the indirect barrier region. Our data suggest that the trapping of these carriers may indeed be suppressed, but further investigation is necessary.

## Introduction:

Solar cells (SCs) convert solar energy to electricity. Current SCs only utilize part of the solar spectrum, so room for improvement remains. Intermediate band (IB) SCs are a possible solution because they allow low energy photons (< SC's band gap) to excite carriers from the valence band (VB) to the conduction band (CB) [1]. Quantum well (QW) IB SCs are easy-to-fabricate layers of different band gap materials, leading to finite potential wells in the VB and CB, each having discrete hole and electron states [2]. Unfortunately, barrier-excited carriers often relax into the well, become trapped, and recombine. The SC's efficiency is reduced because these carriers do not contribute to the current.

Indirect barrier QW structures are expected to suppress the trapping of barrier-excited carriers. Unlike a direct barrier, the Γ-state of indirect $Al_xGa_{1-x}As$ ($x > 0.45$) has the greatest energy, and the X-state has the least. Indirect barrier-excited carriers were expected to thermally relax to the X-state. Then, conservation of momentum and narrow QW width would increase probability of carrier contribution to the current. Since the lattice constant is not dependent on Al composition, GaAs/$Al_{0.8}Ga_{0.2}As$ QWs were grown to study the possible application of indirect barrier QWs as SCs and were characterized using photoluminescence (PL), photocurrent (PC), and voltage dependent current (I vs. V) experiments.

## Fabrication:

Two sets of samples were fabricated.

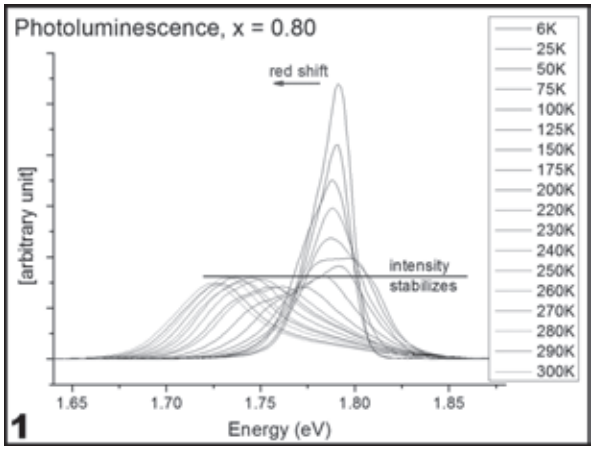
First, two undoped, ~ 3 nm wide, 10-QW structures were grown with molecular beam expitaxy (MBE) for PL measurements. A low Al content x = 0.3 sample served as a traditional, direct barrier reference sample for a high Al content x = 0.80 sample. Second, two high Al content (x = 0.80), doped SCs were grown using MBE. A 0-QW sample served as a reference for a ~ 3 nm wide, 10-QW sample. Photolithography and sputtering were used to create devices for PC and I vs. V measurements.

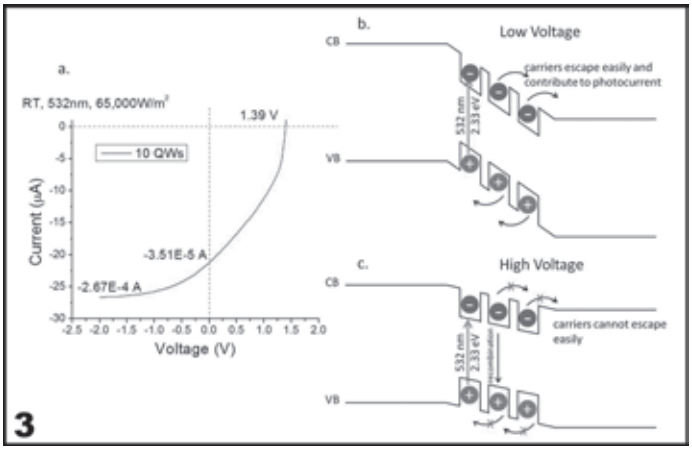
## Results and Discussion:

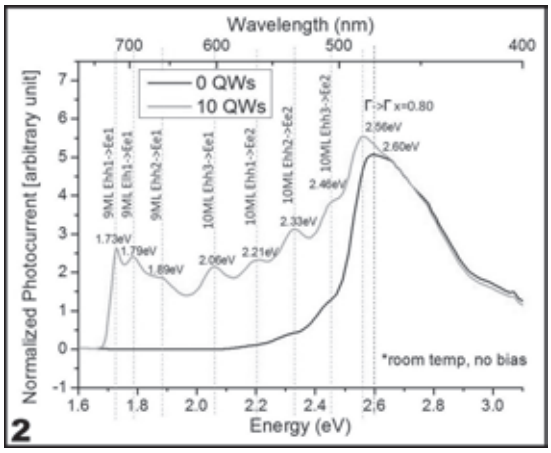
PL occurs when excited carriers recombine and emit a photon [3]. After excitation with a 532 nm laser, the spectrum emitted is observed with a charge-coupled device detector. For the reference sample, temperature increase showed a red shift in peak energy and a decrease in intensity [4]. Quantitative analysis showed that direct sample carriers "see" the lowest energy Γ-state as barrier. Indirect barrier PL stabilized at 125 K as seen in Figure 1. Carrier recombination still occurred, and qualitative analysis predicted high AE. Indirect sample carriers likely "see" the highest energy Γ-state as barrier. Since carriers were not likely to escape to the X-state, they were less likely to relax into the well from the X-state.

PC collected across the visible light spectrum showed carrier excitation energies, including below the band gap. This information was used to determine the exact Al composition and well thickness as labeled in Figure 2 [5].

I vs. V measured from reverse to forward bias with photons above and below the $Al_{0.8}Ga_{0.2}As$ Γ-state band gap of 2.56 eV show carrier trapping and recombination effects. At low voltage, a steep band profile contributed to easy well-



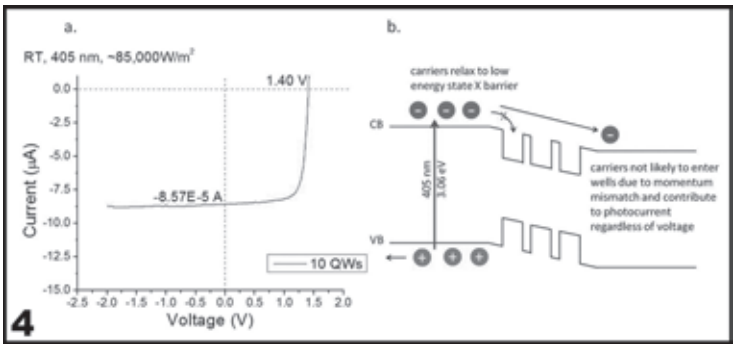




*Figure 1, top: Temp. dependent photoluminescence.*

*Figure 2, bottom: Photocurrent spectra.*

*Figure 3, top: I vs. V with well-excited carriers.*

*Figure 4, bottom: I vs. V with barrier-excited carriers. No significant voltage dependence was observed.*

generated carrier escape, and current was high as seen in Figure 3. A higher voltage yielded a flatter band profile, so carriers could not escape and contribute to the current. This voltage dependence agreed with high AE. Figure 4 shows that barrier-excited carriers were not likely to relax into the wells, and contribution to the current regardless of voltage was expected. No voltage dependence was observed, which is consistent with expectations, but further study is required to prove that carrier trapping is suppressed.

## Summary:

PL showed high confinement and AE in high Al content, 10-QW sample. I vs. V confirmed this high confinement for well-excited carriers and suggested that the trapping of barrier-excited carriers may be suppressed. Further investigation includes measuring PC at different voltage biases and I vs. V at low temperature. A 1-QW sample will also be to more purely study carrier trapping and escape.

## Acknowledgements:

Special thanks to Dr. Takeshi Noda, Prof. Hiroyuki Sakaki, Martin Elborg, Dr. Masafumi Jo, Dr. Takaaki Mano, Dr. Takuya Kawazu, Kumiko Higuchi, the National Institute for Materials Science, the National Nanotechnology Infrastructure Network International Research Experience for Undergraduates (NNIN iREU) Program, and the National Science Foundation.

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# Oxidation of CVD Grown Carbon Nanotubes for Applying Magnetic Complexes for Spin Transport Measurements

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## Abstract and Introduction:

Due to their high aspect ratio and few nuclear spins, carbon nanotubes (CNTs) can be used as one-dimensional models to observe fundamental spin transport. Polarizing electron spins have been done on CNTs by attaching individual magnetic complexes. Different magnetic complexes and attachment mechanisms have been used [1], but the one of interest here are tetramanganese (II) complexes with manganese as the metal [2, 3]. Regardless of the complex however, functional groups need to be introduced to the CNTs in order to chemically attach the complexes.

For this aim, the CNT networks were oxidized at 420ºC in air, pure $O_2$, and an ~ 50/50 mix of $N_2/O_2$ to control the oxidation rate. To measure the degree of oxidation, Raman spectroscopy and resistance measurements across CNT networks were done. An increase in oxidation was expected to show a decrease in resistance and an increase in defects in the CNT network. At 420ºC, the results showed that there were no significant effects on the tubes. Although at 450ºC, results from previous experiments showed an increase in defects from the Raman spectroscopy [4].

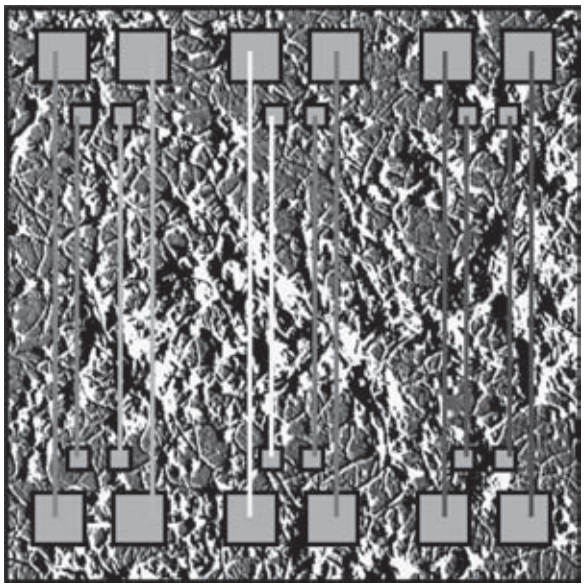

*Figure 1: The contacts were arranged on the substrate with the contacts represented by the grey squares. A "large vertical" configuration is shown with the large lines being current and the short lines are voltage measurement. The sets of colors show that we can perform six measurements across the sample. The 10-micron by 10-micron AFM image underneath shows the networks on the substrate (not to scale compared to the substrate).*

## Methods:

CNTs were grown in a tube furnace at 860ºC on a one-$cm^2$ quartz substrate using a Fe/Mo catalyst. Using this procedure, networks of CNTs were grown on the substrate and then Ti/Pt (3/70 nm) contacts were deposited on the pristine networks. Figure 1 shows how these square contacts were distributed on the quartz substrate along with an atomic force microscope (AFM) image of the networks. The tubes were oxidized in air, pure $O_2$, and an $O_2/N_2$ mixture. In air, the tubes were oxidized in a muffle oven. Pure $O_2$ and $O_2/N_2$ oxidations were performed in a tube furnace. The gasses bubbled through water before going into the oven because COOH groups are needed for a latter functionalization [2].

The CNTs were characterized by a Bruker RAMII spectrometer with Fourier-transformed Raman measurements at an excitation wavelength of 1064 nm. Figure 2 displays an example of a Raman spectrum data with the D and G peak labeled. The ratio of the area underneath the D and G peak was sensitive to the number of defects created and was obtained by using a numerical approach. The peaks were subtracted from a linear background and then a trapezoidal rule was performed to get the areas and ratios.

The resistance across the CNT network was also measured using two probe and four probe measurements. Using the contacts, a current was swept through the network and the voltage drop was measured at each oxidation step to obtain the resistance. Since the samples were not homogenous, different combination of contacts were tried across the sample. Figure 1 represents how a four probe measurement "large vertical" configuration was done.

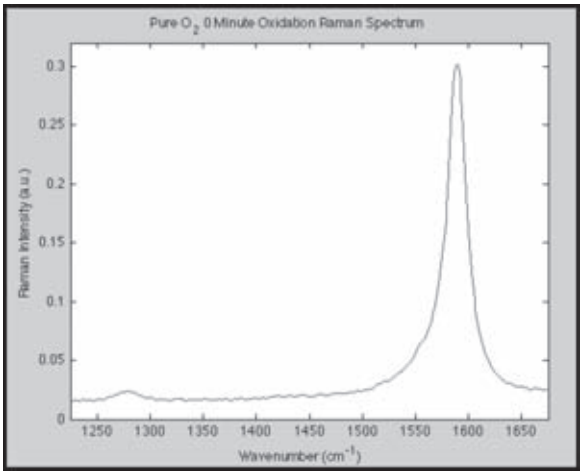


*Figure 2: Pure $O_2$ zero minute Raman spectrum to show the D and G peak shown as the left and right peak, respectively.*

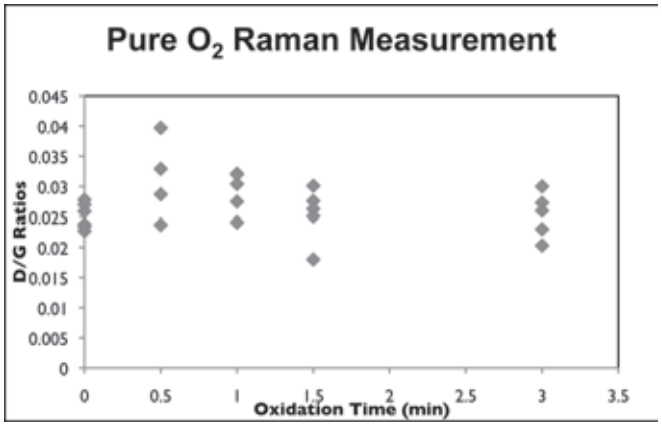


*Figure 3: D/G Ratios from pure $O_2$ measurements. As shown the ratios stay constant within the error of the measurements.*

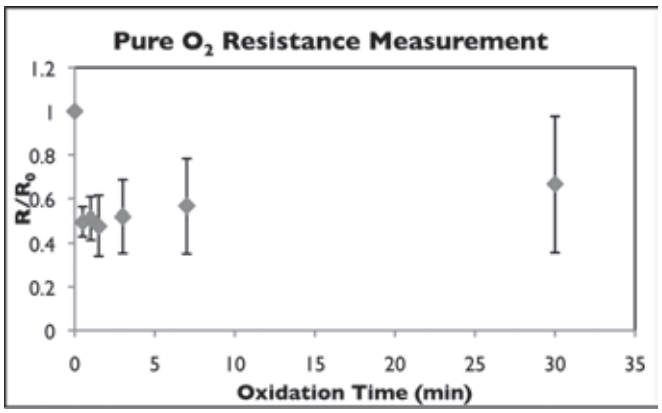


*Figure 4: Resistance measurement of the pure $O_2$ sample from the large vertical configuration shown in Figure 1.*

## Results and Discussion:

The ratio between the area under the D peak and the area under the G peak stayed constant throughout the oxidation, as shown by Figure 3. The resistance across the channels for all three conditions went down sharply after an initial oxidation of thirty seconds to a minute and then stayed constant within the errors of the measurements until oxidation was stopped after 30 minutes. Figure 4 displays the results of the resistance measurements of pure $O_2$ with the "large vertical" configuration.

The D/G plots didn't seem to show strong evidence for defect formation on the CNTs. This was likely due to the fact that 420ºC was not hot enough for significant amount of defect formation. With the resistance, the initial drastic drop can be attributed to the CNTs crosslinking, which would create stronger paths for the current to flow through. Afterwards, the resistance stays constant within the errors of the measurements. This agrees with the little to no defects formed on the CNTs. At 450°C, on the contrary, oxidation definitely takes place; the D/G ratio saturates to twice of its original value and resistance decreases until 12 min [4].

## Conclusions:

CNTs were grown in a tube furnace in a network on top of a quartz substrate. The CNTs were oxidized in three different manners, pure $O_2$, $N_2/O_2$ mix, and air, all at 420ºC. These tubes were analyzed using Raman spectroscopy and resistance measurements. The Raman measurements did not show any change in the D/G ratio, but the resistance decreased. The constant D/G ratio was most likely due to the fact that 420ºC was not hot enough to create defects on the tubes. The sharp drop in resistance after initial oxidation can be explained by CNTs crosslinking.

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# Monolayer Molybdenum Diselenide

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## Abstract:

We fabricated a device based on few-layer molybdenum diselenide ($MoSe_2$), a unique two-dimensional (2D) semiconducting material in the family of transition metal dichalcogenides. Unlike its sister material, molybdenum disulfide ($MoS_2$), monolayer $MoSe_2$ is largely unexplored [1]. Here, we employed the same exfoliation technique developed by the winners of the 2010 Nobel Prize in Physics for their work with graphene [2]. In this method, scotch tape is used to exfoliate $MoSe_2$ crystals. These crystals are then deposited on the surface of a silicon dioxide/silicon chip. Using an optical microscope, few-layer $MoSe_2$ pieces are identified. A precise measurement of the thickness of each $MoSe_2$ piece is determined using atomic force microscopy. By combining these methods with electron-beam lithography to create a transistor, we can ultimately examine the unexplored optical and electronic properties of monolayer $MoSe_2$.

## Introduction:

In recent years 2D semiconducting materials have been produced that exhibit interesting electrical and optical properties. In monolayer materials, electrons behave differently than in bulk materials. As electrons move through monolayer materials, they are confined to two dimensions, thus resulting in different properties. Graphene is a 2D material that has been greatly explored. One interesting property of graphene is that it has a very high electron mobility of 200,000 cm2 $V^{-1}s^{-1}$ [3]. However, graphene does not have a naturally existing band gap and its on/off current ratio of five is very low [4]. Due to this lack of a naturally existing band gap, graphene is not an ideal material for making transistors. For the fabrication of 2D transistors, it is essential to find new 2D semiconducting materials. Recently, a family of compounds known as the transition metal dichalcogenides has been of interest in monolayer form. One transition metal dichalcogenide, molybdenum disulfide ($MoS_2$), has been studied widely in monolayer form. This material has a band gap of 1.8 eV, an on/off current ratio of $10^8$, and an electron mobility of 380 $cm^2$ $V^{-1}s^{-1}$ [5].

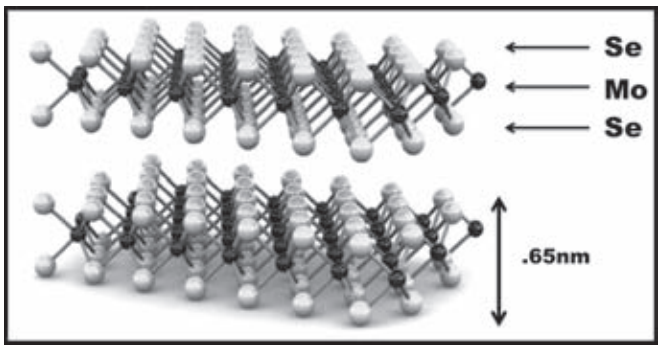


*Figure 1: Structure of $MoSe_2$, after [1].*

We explored another transition metal dichalcogenide, molybdenum diselenide ($MoSe_2$), with the hopes of finding a material with similarly high on/off ratio, but with a lower band gap, and a higher electron mobility.

$MoSe_2$, shown in Figure 1, is an inorganic compound that has been used in bulk form for many years as a dry lubricant. The predicted band gap of a monolayer based on the band structure of a bulk crystal is 1.6 eV. The approximate height of a single layer of $MoSe_2$ is 0.65 nm, as determined from a bulk crystal. Once these layers are exfoliated and isolated, then electrical and optical properties of this unexplored monolayer material may be investigated.

## Experimental Procedure:

First, we deposited $MoSe_2$ crystals on Scotch™ tape and then ripped the tape apart several times until the crystals were very fine. Due to van der Waals interactions, this material's layers could be easily ripped apart. Second, the tape containing the exfoliated $MoSe_2$ crystals was placed on top of a silicon chip with 285 nm of thermally grown $SiO_2$. Then we rubbed the tape against the chip to transfer the exfoliated crystals from the tape onto the chip. Next, an optical microscope was used to scan the chip for possible monolayer, bilayer, and trilayer pieces of $MoSe_2$. This process took advantage of the way that $MoSe_2$ absorbs light to determine if a piece could possibly be one to a few layers thick. Typically, a monolayer to bilayer of $MoSe_2$ appears pink to light purple in color.

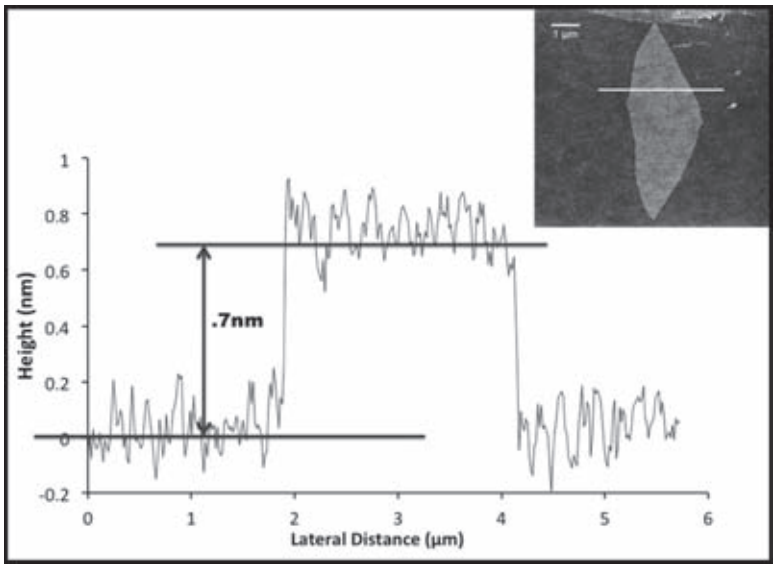


*Figure 2: Cross-sectional plot of a monolayer of $MoSe_2$. The AFM image is in the upper-right corner; the cross-section is indicated by the white line.*

Then an atomic force microscope (AFM) was used to confirm the height of interesting $MoSe_2$ pieces. By looking at a cross-sectional plot of the $MoSe_2$ sample, shown in Figure 2, we were able to measure the height of each piece. Keeping in mind that a single layer of $MoSe_2$ as measured from a bulk crystal is 0.65 nm thick, we used the AFM cross-sections to determine if a given piece was a monolayer, bilayer, or trilayer. Our device fabrication process is illustrated in Figure 3.

Fabrication started with a thin piece of exfoliated $MoSe_2$ on the silicon chip (Figure 3a). Next, the chip was spun with resist. Exposure to the chip via electron-beam lithography and development followed (Figure 3b). Finally, 50 nm of Au were evaporated for electrodes (Figure 3c). The transistor device was completed upon lift-off of the Au (Figure 3d).

Figure 4 shows the fine features one of the several devices that were successfully fabricated.

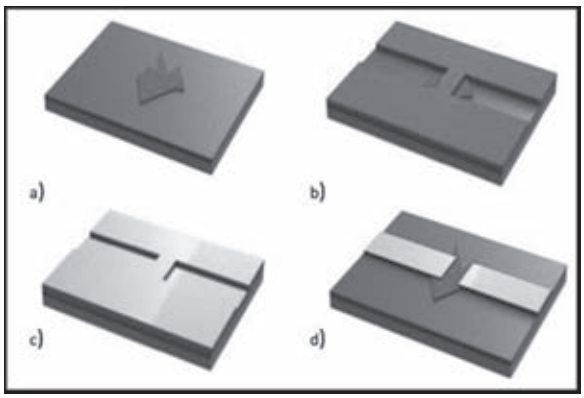


*Figure 3: Device fabrication process.*

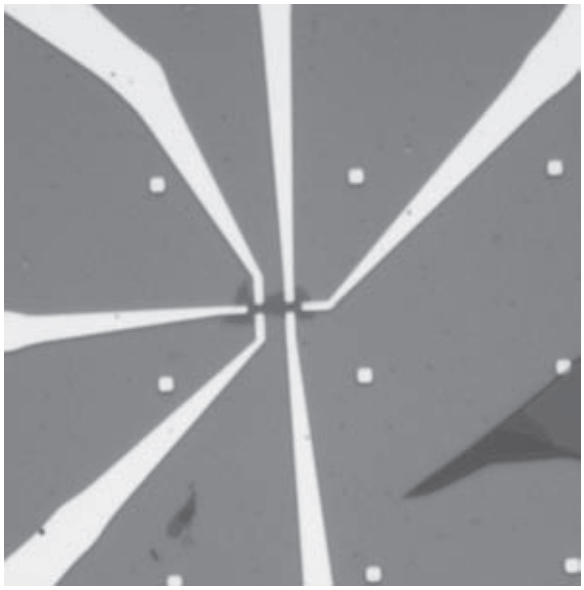

*Figure 4: Completed device made from a trilayer piece of $MoSe_2$.*

## Summary and Future Work:

We successfully exfoliated and isolated few-layer $MoSe_2$. Sixty thin samples of $MoSe_2$ were exfoliated and measured using AFM, and several few-layer $MoSe_2$ devices were successfully fabricated. We are currently working towards measuring the electrical and optical properties of $MoSe_2$. The devices we fabricated will be used specifically to look at the band gap, on/off current ratio, and mobility of monolayer $MoSe_2$.

## Acknowledgements:

We extend our thanks to the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, National Science Foundation, Cornell NanoScale Science and Technology Facility, Rob Ilic, Melanie-Claire Mallison, and to all the CNF Staff.

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# Oxidation Effect in Single Dot Quantum Junctions

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## Abstract:

Three-terminal devices with a monolayer of quantum dots (QD) between nanometer-spaced gold electrodes allows for the study of single electron quantum transport. Indeed, IV measurements for a 50 nm device show characteristic Coulomb staircase under dark condition and with 543 nm and 670 nm light. However, lead selenide (PbSe) devices of various sizes exhibited current fluctuations on the order of nanoAmperes (nA) over time, both under dark condition and with light. Also, a slow relaxation after shining light was observed. With increasing oxidation, the devices stabilized and the relaxation time decreased, which suggests the surface state of the QD governs transport through the device.

## Device Fabrication:

The devices had high aspect ratios: while the width of the devices varied from 10 $\mu$m to 20 nm, the gap between the electrodes was kept at about 6 nm to fit the QD monolayer. In order to achieve this, a layer of chromium (Cr) was evaporated on top of titanium (Ti) adhesion and first gold (Au) electrode layers. The growth of $Cr_xO_y$ led to an overhang over the edges of the first layer. The overhang served as a mask for the second Au electrode layer, producing 6 nm gaps when the Cr and oxide were etched away [1]. A monolayer of PbSe colloidal QD was deposited via the dipcoating method [2]. Ligand substitution, which increases coupling to the electrodes, was performed with 1,2-ethanedithiol (EDT).

## Theory:

Device behavior was modeled on single electron resonant transport, which assumed weak coupling (though coupling may be much stronger because EDT is short). The QD can be considered to have discrete quantum levels (Figure 1).

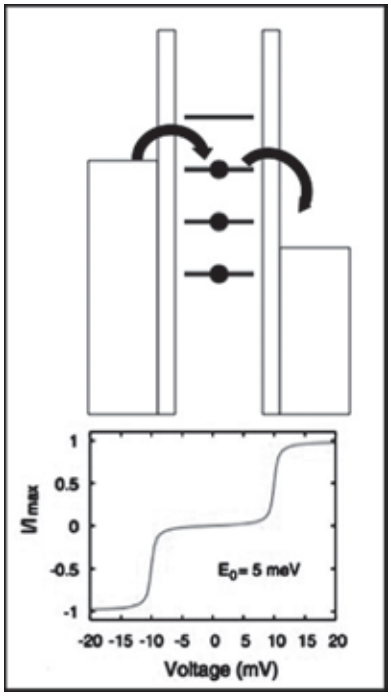


*Figure 1: Schematic of chemical potentials of QD and electrodes; Coulomb staircase.*

Tunnel barriers separated the QD from the electrodes on each side, wherein the electrons obeyed the Fermi-Dirac distribution. To observe quantum behavior, low temperature was required to ensure that the energy difference between quantum levels in the QD (~ 1 meV) and the charging energy of the device ($e^2$/(2C), where C is the capacitance of the device, ~ 25 meV) were greater than the thermal energy of the charge carriers.

In these devices, current was driven by the chemical potential difference between the charged states in the QD and the electrodes. For resonant transport, the chemical potential of the QD charged transition state must lie within the bias window, which is the energy range between the chemical potentials of the electrodes. Electrons with energy resonant with the QD level tunneled from occupied states in the source to the QD, then ended up in empty states in the drain. A sharp increase in current was observed as a step when the bias window enclosed a resonance.

At low bias, current was suppressed as there were no transitions that were within the bias window. For the QD to undergo a charge transition (by adding or removing an electron to or from the QD), a charging energy penalty was required. This region of high differential resistance is known as a Coulomb blockade and is observed as a flat region in the IV curves.

Photoconductance depended on the formation of excitons and extraction of charge carriers to the electrodes. Formation of excitons depended on the absorption rate, which depended on laser power. Photoconductance varied monotonically with the laser power density; therefore, increased current should be observed with increased laser power.

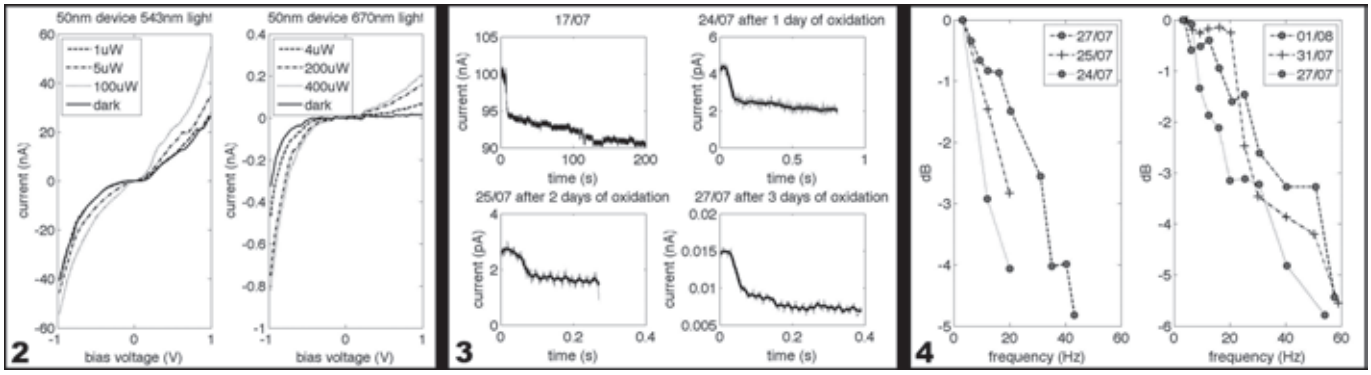


*Figure 2, left: Coulomb staircase in 50 nm device at 10K.*

*Figure 3, middle: Continuous-wave measurement of current decay at room temperature.*

*Figure 4, right: Time-resolved measurement with modulated light intensity at room temperature.*

## Results:

IV measurements were performed from -1V to 1V in vacuum and at cryogenic temperatures. Figure 2 shows a 50 nm device that exhibited step behavior characteristic of single or few QDs. Photoconductance was observed for both 543 nm and 670 nm. The Coulomb blockade region became smaller with increased laser power as well. For the larger devices with more QDs, the IV curves were smoother, indicating that the presence of many QDs smoothed out the staircase behavior of a single QD. However, the reference dark IVs changed by a few nA over days, with no apparent trend for the change in Coulomb blockade region size or magnitude of current. Measurements of current over hours at 0.5V showed fluctuations of order nA as well.

The devices were exposed to air in room temperature one day at a time. After each day of oxidation, continuous-wave and time-resolved measurements were performed. For the continuous-wave measurement, after shining 670 nm 100 $\mu$W light, the devices were then covered and the decay of the current was observed over time. For the other measurements, the intensity of the light was modulated at increasing frequencies in order to observe when the device stopped exhibiting photoresponse. The value of 3dB was a metric for the cutoff of photoresponse.

Figure 3 clearly shows the relaxation time decreased with increased oxidation, especially dramatically after one day. Figure 4 shows that with the frequency for the cutoff of photoresponse increased with increased oxidation. These both indicate that the device showed clearer photoresponse with increased oxidation.

## Future Work:

Oxidation reduces the time dependence of current and the relaxation time in these three-terminal devices. However, the measurements performed were only preliminary measurements and oxidation was not performed in a completely controlled fashion. Future work includes oxidation of different systems in a more controlled manner, with variation of QD type (CdSe, for example) and device width.

## Acknowledgments:

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# A 3D Circuit QED Architecture with Separate Readout and Coupling Cavities

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**Abstract:**

This work presents the development of a three dimensional circuit quantum electrodynamics (3D cQED) architecture with separate cavities for inter-quantum bit (qubit) coupling and for qubit readout. Such a separation allowed for optimization of the cavities for their separate tasks, as opposed to the compromise necessary in single-cavity architectures. The device designed was a 3D analogue of a working multi-resonator, multi-transmon qubit device in standard, planar circuit QED. By switching from coplanar waveguide (CPW) resonators to 3D cavity resonators, we expected to attain significantly higher qubit and resonator coherence times (tens of microseconds), allowing realization of complex quantum computing algorithms, while retaining the virtue of physical scalability. The architecture pursued also included local flux tuning of qubit transition frequencies, necessary for control of qubit-qubit interactions on nanosecond timescales. We present here the design, simulation and initial characterization of the first prototype.

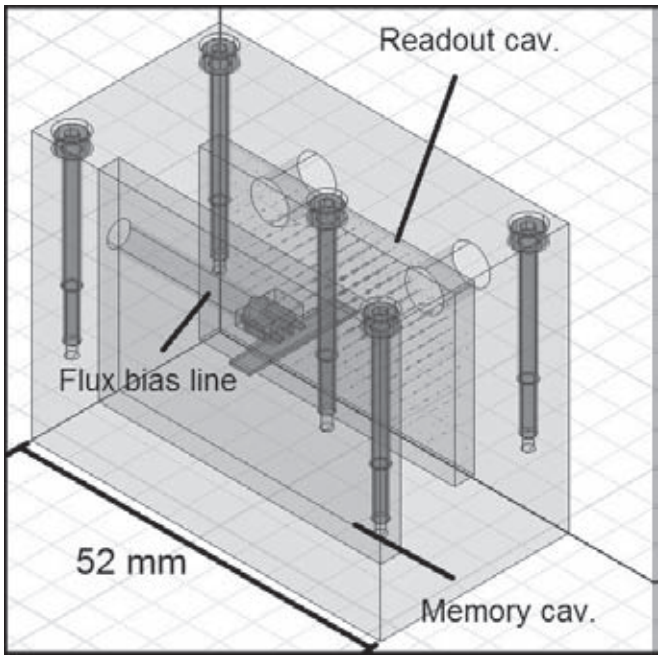


*Figure 1: HFSS model of device geometry. The qubit substrate straddles the two cavities. The fundamental mode of the readout cavity is displayed as a vector plot.*

## Introduction:

The emergence of cQED as a leading paradigm for the solid-state realization of quantum information processing has inspired a slew of refinements on the basic topology, which uses CPW resonator(s) to couple to one or more qubits. One such refinement replaces the CPW resonator(s) with 3D superconducting cavity resonator(s), a change that improves coherence times. Another refinement introduces separate cavities for readout and for memory/coupling. A multi-cavity scheme allows for specialized tuning of qubit-cavity coupling strength, $g$. A high $g$ is desired between the qubit and the dispersively coupled readout cavity in order to increase the distinction between the measurements corresponding to the two qubit states, translating to an increase in readout fidelity. However, such strong coupling between the qubit and the inter-qubit coupling cavity creates residual cross-coupling between qubits. If resonant gates are used, then this coupling can be decreased to mitigate these negative inter-qubit effects while still matching the gate times achieved with dispersive gates.

It was thus straightforward to combine the above two ideas and to conceive of a multi-resonator, multi-qubit 3D cQED architecture. It should be noted that any such architecture should ideally also include the flux bias lines needed to tune the qubit transition frequencies on nanosecond timescales, needed to realize multi-qubit gates. In this work, we made use of a transmon qubit consisting of two super-conducting aluminium islands connected by two Josephson junctions, all on a sapphire substrate.

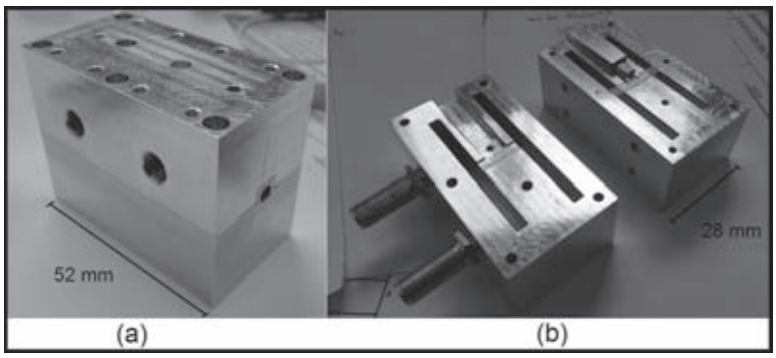


*Figure 2: (a) Fabricated device, fully assembled. (b) Fabricated device in two halves with connector/substrate visible.*

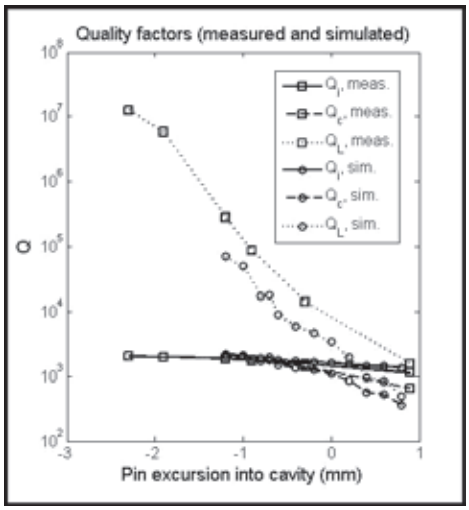


*Figure 3: Loaded, intrinsic, and external quality factors as simulated and as measured. In simulation, zero dielectric loss is assumed, and the cavity is defined with bulk conductivity 3.8 × 10⁷ S/m.*

## Design:

The cavity design was carried out primarily using ANSYS high frequency structure simulator (HFSS), a full wave simulator that allowed modeling of high-frequency electromagnetic behavior in arbitrary geometries. With HFSS, we could determine the geometries that provided the desired resonant frequencies and make predictions concerning the coupling and intrinsic quality factors of the individual cavities. Figure 1 displays the HFSS model for reference.

The qubit design was carried out using ANSYS Maxwell, a simulator geared towards electro- and magneto-static simulations. We employed it to calculate the inter-island capacitance of the qubit structure, a parameter that determines the charging energy of the qubit. Due to the device geometry, however, the physical size of the qubit was nearly a fifth of a wavelength at the highest operating frequency of interest. This implied that the super-conducting islands acted as distributed elements, rather than as lumped elements, casting some uncertainty on the simulation results.

Flux bias was controlled by applying a voltage between a shorted trace and ground, generating a current through the trace that in turn gave rise to a magnetic flux normal to the plane of the trace. The use of very small profile connectors was necessary due to the relatively high (7 GHz) frequencies of operation of the device. We employed a standard miniature subminiature push-on (SMPM) edge launch connector to realize the connection of a coaxial cable to the trace on the substrate.

## Fabricated Device:

The finalized design was sent to a professional rapid CNC prototyping company for manufacture in aluminium 6082-T651. Figure 2 depicts the fabricated device. In actual operation, the qubit and flux bias geometry will be fabricated on the displayed substrate, and the connector will be wirebonded to the flux bias geometry.

## Experimental Results:

At this time, only room temperature measurements of transmission through the readout cavity have been made, varying coupling strength by using coupling pins of different lengths. Good qualitative agreement is seen between HFSS and measured results. Ten resonant modes of the readout cavity were observed and differed from those predicted by simulation by, at most, 150 MHz. The average deviation was 45 MHz, and the median deviation was 20 MHz. The desired resonant frequency for the fundamental mode of the readout cavity was 7 GHz; the observed value was 7.03 GHz. Figure 3 depicts measured and simulated quality factors for the readout cavity.

## Conclusions:

A preliminary two-cavity one-qubit device has been fabricated, and initial characterization does not deviate significantly from predicted behavior. The next step is to characterize the device under superconducting conditions (i.e., low temperatures) and finalize/fabricate a qubit for this device. At this time, a scaled-up three-cavity two-qubit device has been fabricated, and future work will include realization of quantum algorithms with the benefits of this architecture.

## Acknowledgements:

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