Electrochemical Deposition of Polythiophene onto Carbon Nanotube Arrays

Ryan Parry

Mechanical Engineering, North Carolina State University

NNIN REU Site: Nanotechnology Research Center, Georgia Institute of Technology, Atlanta, GA

NNIN REU Principal Investigator: Baratunde Cola, Mechanical Engineering, Georgia Institute of Technology

NNIN REU Mentor: Virendra Singh, Mechanical Engineering, Georgia Institute of Technology

Contact: rjparry@ncsu.edu, cola@gatech.edu, vsingh@gatech.edu

Introduction:

Each new generation of electronic products uses high-speed microchips that squeeze more transistors/power and performance into even smaller packages. This leads to excess heat generation within the semiconductor components, which causes the chip to fail over time. Heat sinks were added to help cool these chips. Heat sinks allow for the heat to dissipate from the chip to the heat sink to a cooler ambient, like air. When the heat sink and microchip were first put together, it was found that the two surfaces formed contact points and air gaps. Contact points are areas where the chip and the sink are connected together and heat can travel successfully from the chip to the sink. Air gaps are all the areas between the contact points where heat has trouble crossing from chip to sink. Since air is an insulator, the heat builds up on the chip at these air gaps and become hot spots, which lead to device failure.

Thermal interface materials (TIMs) were used to eliminate the air gaps within the component and consequently provide a path of heat removal from the component package surface through the heat sink and heat spreader. Therefore, TIMs are integral part of overall electronic product design. An ideal TIM will have both high thermal conductivity and the ability to conform to the surfaces well. These are two major characteristics that determine the total thermal interface resistance of different surfaces. In order to improve the life and performance of electronic devices, TIMs with improved thermal resistance are in urgent need.

Carbon nanotubes (CNTs) are being researched as a favorable TIM because of their high thermal conductivity. CNTs allow for vertically aligned columns to transfer the heat from the chip to the sink [1-4]. However, the poor adhesion of CNTs to the substrate limits their use as TIMs for high power devices. In order to improve the performance of CNT based TIMs, the problem of adhesion has to be addressed.

The goal of this current research was to develop a hybrid material that combined the high thermal conductivity of carbon nanotubes (CNTs) and exceptional mechanical compliance of polythiophene (Pth). We selected Pth as the polymer of choice as it is an electroactive polymer and can be deposited electrochemically. Additionally, Pth is thermally stable up to the device operating temperature.

Experimental Procedure:

In a typical fabrication process, diced 2 × 3 cm silicon wafers were cleaned extensively. Two different catalyst seed layers — 100 nm titanium (Ti) / 10 nm aluminum (Al) / 3 nm iron (Fe), and 40 nm silicon oxide (SiO_2) / 10 nm nickel (Ni) — were deposited using a Denton Explorer e-beam evaporator. We used three minutes of low pressure chemical vapor deposition on the Ti/Al/Fe samples and 15 minutes of plasma-enhanced chemical vapor deposition on the SiO_2/Ni samples to induce CNT growth on the wafers using acetylene as precursor gas in a Black Magic PECVD reactor.

Finally, the CNT arrays were coated with Pth using three electrodes electrochemical deposition. The current was sent from the working electrode, the silicon wafer, to the

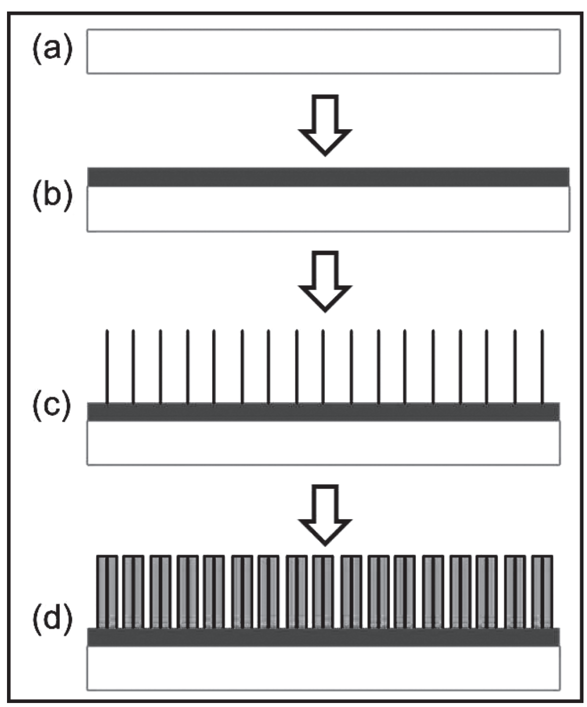

Figure 1: Fabrication process. (a) Silicon wafers. (b) Deposition of catalyst layer. (c) CVD for CNT growth. (d) Pth electrodeposition.

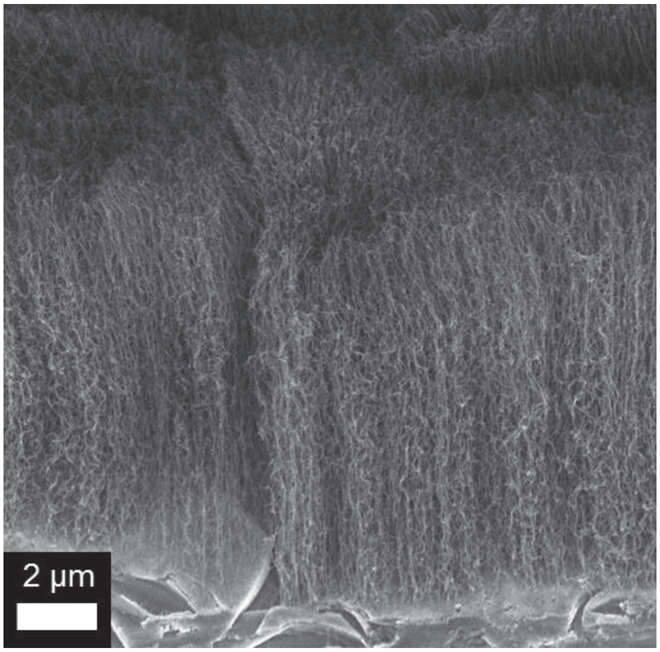

Figure 2: SEM image of Ti/Al/Fe CNT growth.

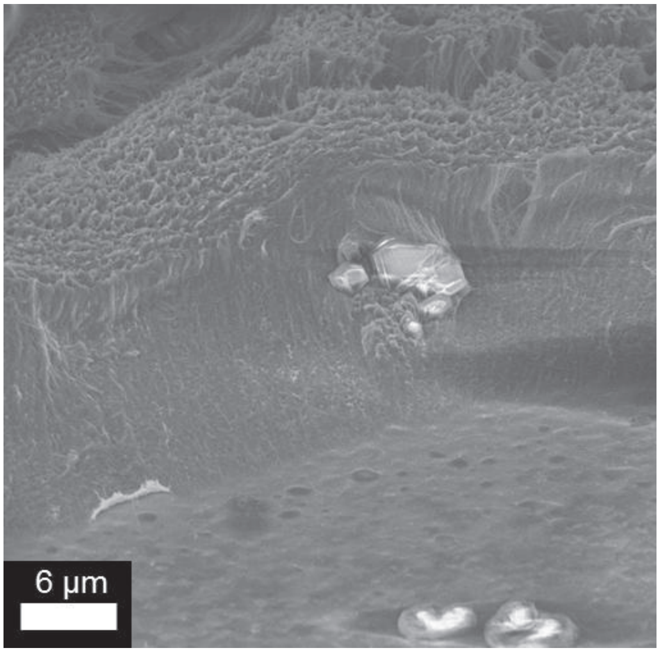

Figure 3: SEM image of Pth coating CNT arrays.

counter electrode, which was immersed in Pth solution, with the reference electrode measuring current. We used cyclic voltammetry to be able to control the amount of Pth coated on the CNTs and ran samples using 5, 10, and 15 cycles.

To evaluate the orientation, thickness, height, and density of the CNTs and Pth coating on CNTs, we used a scanning electron microscope (SEM). A typical fabrication procedure is outlined in Figure 1.

Results and Conclusions:

After CVD, we found that the Ti/Al/Fe catalyst layer produced the desired CNT arrays, and we used this catalyst layer for further experiments. As shown in Figure 2, the vertically aligned arrays measuring about 10-12 μm tall and a density of about 2×10^{-7}cm^2 was obtained in a typical LPCVD recipe with a three minute growth time.

The CNT arrays were successfully coated with Pth through electrochemical deposition using cyclic voltammetery (Figure 3). However, we were only able to coat a thick layer of Pth on top of the CNTs and further modification of electrochemical process is required to achieve a conformable coating.

Future Work:

Future research will involve quantifying how much Pth is deposited per cycle during deposition. This will allow us to control coating with the amount of cycles. In addition, we need to determine how to coat the individual CNTs and not just the whole array. Using a photoacoustic technique, we plan to measure the thermal resistance for our hybrid structures to compare to other TIMs. Additionally, we will run adhesion and electrical/thermal conductivity tests in order to ensure our TIM will adhere to the surfaces as predicted, without affecting the thermal performance. The long-term plan is to develop this material into an effective Thermal Interface Material that can be used in electronics to improve current technology and increase the life-span of electronics.

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