Fabication of GaAs-Based Integrated Circuits by Advanced Nanofabrication Techniques

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Abstract:

Gallium arsenide (GaAs), a III-V semiconductor, has recently gained attention due to promising applications in wireless technologies that include power amplifiers and integration of switches for use of different frequency bands. The relatively high electron mobility, lower high frequency noise, and lower parasitic capacitances of GaAs in comparison to silicon make GaAs a suitable choice for high frequency integrated circuits.

This project focused on the creation of three GaAs integrated circuit (GaAs-IC) devices — specifically the: 1) Metal-semiconductor field effect transistor (MESFET), 2) Logic Inverter, and 3) Ring Oscillator — with each subsequent device employing the previous device as a base component. The Schottky barrier intrinsic to the MESFET made it difficult to achieve the necessary positive threshold voltage for creating a functional ring oscillator. Using industrial level design, fabrication, characterization, and analysis techniques, all three devices were ultimately created and the functional ring oscillator achieved an operating frequency of 19.9 MHz — a value comparable to predicted values.

Approach:

One cycle of the project involved the computer automated design of a new sample (including several devices), followed by fabrication in a cleanroom environment. The devices were then characterized using the manual prober system. Data was analyzed using MATLAB.

Methods:

Preparation of GaAs Substrate. The GaAs substrate used; 1) an n-type GaAs active layer ($N_D = 3 \times 10^{16}$) with an initial thickness of 500 nm on, 2) a semi-insulating GaAs. The GaAs wafer was first cut to the appropriate size. Thinner active layers correspond to higher threshold voltages, so the sample was then etched with $H_3PO_4 : H_2O_2 : H_2O = 1 : 1 : 50$ to achieve a depth ranging from 100 nm to 500 nm.

Mesa Fabrication. The sample was coated with primer (HMDS), then photoresist (AZP4620 : PGMEA = 3 : 1). Samples were exposed to the Mesa pattern using the DL-1000 laser lithography system and hand developed in 2.38% tetramethylammonium hydroxide (TMAH). A postbake at 140°C prepared the sample for a second etching process that electrically isolated the samples. The photoresist was removed with N-methyl-2-pyrrolidone (NMP).

Source and Drain Electrode Fabrication. The sample was coated with primer (HMDS), then two photoresists (PGMI and TSMR8800). Samples were then exposed and developed. Au-Ge/Ni/Au = 1500A/100A/1500A was deposited by the R-DEC e-gun evaporation system. The resist and excess metal was lifted off with NMP. The sample was then annealed at 400°C to prepare the sample for a second etching process that electrically isolated the samples. The photoresist was removed with N-methyl-2-pyrrolidone (NMP).

Gate Electrode Fabrication. The sample was coated with primer (HMDS), then two photoresists (LOR5A and AZ5214E). Samples were then exposed and developed. Ti/Au = 2000A/2000A was deposited by the ULVAC jsputter sputtering system. The resist and excess metal was lifted off with NMP.

A completed ring oscillator device is shown in Figure 1.

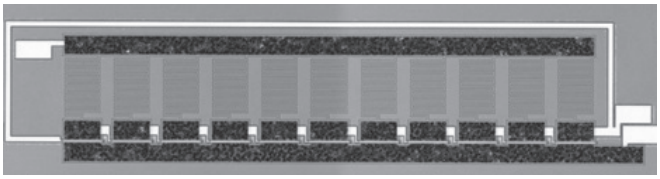

Figure 1: Completed ring oscillator device.

Results:

Positive Gate Threshold Voltage Achieved Through T-Gate Design. An active layer thickness of below 174 nm is needed to achieve a positive threshold voltage. However, functional devices with this thickness are difficult to create due to increased defects at the interface of the active layer and semi-insulating GaAs; effective mobility is determined to drop significantly as active layer thickness is decreased. Initial MESFET fabrication resulted in a maximum threshold

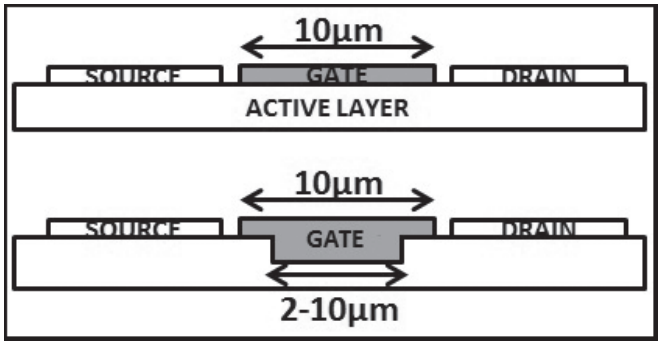

Figure 2: Schematic of T-gate (bottom) with original gate for reference (top).

voltage of -0.22V determined from drain current as a function of gate voltage data measured using a manual prober system for each device.

The T-gate design (Figure 2) involved using the gate width of 10 μm employed in earlier designs while etching a portion of the active layer ranging in width from 2 μm to 10 μm centered below the gate metal. By etching the active layer at only this area to 141.3 nm and 172.4 nm, positive threshold voltages of 0.15V and 0.3V were achieved, respectively (Figure 3). The most successful T-gate variation had a 2 μm base width.

MESFET and Inverter Performance. Devices across MESFET and inverter samples were found to be consistent. Strong gate dependences were observed and inverter devices exhibited sensitive input and full-scale output.

Ring Oscillator Performance. Functional ring oscillators were fabricated using the T-gate design on the 174.2 nm active layer sample. Oscillation frequencies of 19.9 MHz were observed for load resistances of 3.2 kΩ and 1.7 kΩ corresponding to applied voltages of 1.3V and 0.9V, respectively.

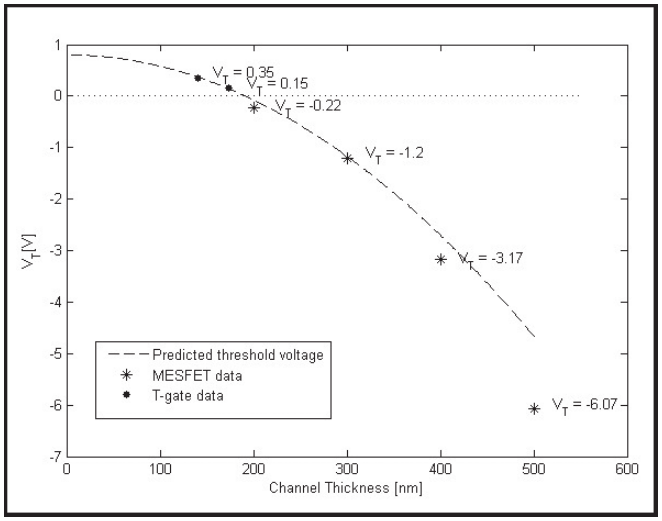

Figure 3: Average threshold voltage as a function of active layer thickness. Values for thicknesses over 200 nm correspond to MESFET data while values for thicknesses below 200 nm correspond to T-gate data.

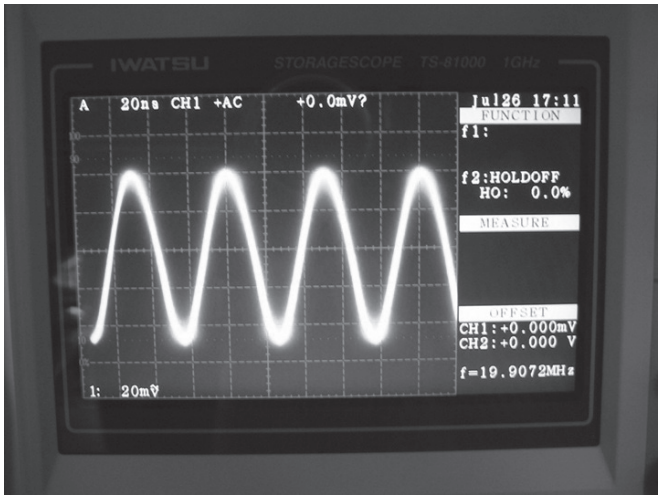

Figure 4: Functional ring oscillator output for R = 3.2 kΩ and V_{DD} = 1.3V.

Conclusions and Future Work:

The importance of achieving a positive threshold voltage was realized during early iterations. The resulting design and fabrication of the T-gate overcame the decrease in effective mobility for thinner active layers and contributed to the successful fabrication of all three target devices. The ring oscillator output oscillation frequencies of 19.9 MHz were comparable to calculated values.

However, the ring oscillator design can be improved in future iterations. A T-gate base width below 2 μm may increase effective mobility and produce stronger inverting characteristics at lower load resistances, producing higher oscillation frequencies. In addition, it has been observed that full sized 200 μm by 200 μm source/drain electrodes have a higher effective mobility and corresponding drain current than the compacted 100 μm by 200 μm electrodes used for later samples. Use of full sized versions in future designs may yield similar performance improvements.

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References:

[1] Sze, S; "Physics of Semiconductor Devices" (2006).