Inkjet Printed Interconnects for Multilayer Flexible Electronics

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Abstract:

We have developed a method to fabricate fully interconnected flexible multilayer circuits at a high rate using inkjet printing. Ink containing silver nanoparticles was used for the conducting layers, and SU-8 2002 photopolymer was used for the insulating layers. During fabrication, vias with diameters between 65 μm 0and 100 μm were printed consistently, and the measured resistance of the multilayer interconnects differed little from that of single layer circuits. Bend tests revealed a slight increase in resistance, which stabilized with repeated bending.

Introduction:

Inkjet printing is emerging as an efficient and versatile method for the mass production of flexible electronic devices, such as organic light-emitting diode (OLED) displays, phased-array antennae and radio-frequency identification (RFID) tags. Many such devices require complex circuitry, which can take up considerable space. Thus, there is need for a method to create multilayer circuits in order to make the devices more efficiently utilize the available real estate.

The main objective of this project was to develop a method to reliably create multilayer interconnections for printed electronics at a high rate. The aim was to consistently create via holes that had a diameter of 100 μm or less. In addition, the process needed to be completely additive and able to be implemented using a high speed roll-to-roll printer for high throughput manufacturing.

Experimental Procedure:

The printing process involved printing a bottom conducting layer on a flexible Kapton® substrate, followed by a middle insulating layer containing via holes, and finally a top conducting layer, which connected to the bottom layer through the vias. Silver nanoparticle ink was used for the conducting layers and SU-8-2002 photopolymer was used for the insulating layer. These materials were chosen because they were readily available; however, this technique can be implemented using any printable material ink.

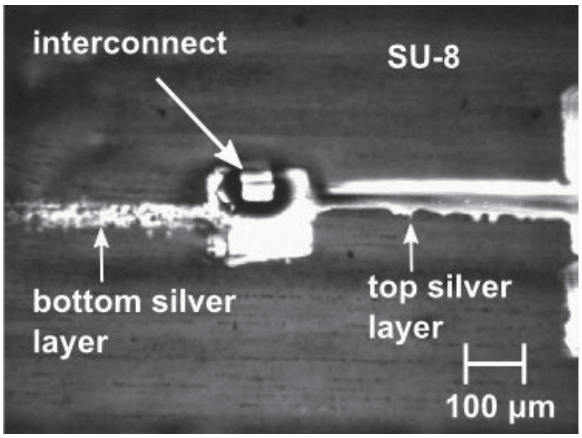
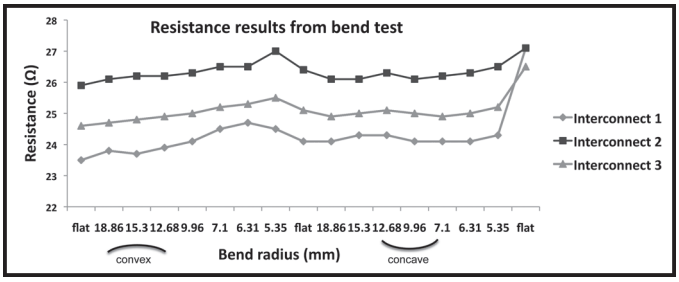


Figure 1: Optical image of multilayer interconnect.

The circuit elements were designed using AutoCAD and printed using a Fujifilm Dimatix Materials Printer, DMP 2800. The layers were aligned using ink-jet printed silver alignment marks on the flexible substrate and the printer's fiducial camera. The bottom silver layer was printed on the substrate and annealed at 150°C for permanency and conductivity. The SU-8 layer containing via holes was then printed on top of the bottom silver layer and cured using heat and ultraviolet radiation. The SU-8 was treated with oxygen plasma to increase its wettability. The entire structure was heated at 150°C to prepare the SU-8 surface for the top silver layer. The top silver layer was printed and annealed on the SU-8 with interconnects to the bottom layer through the vias (Figure 1).

In order to determine the minimum printable via hole size, we printed holes with sizes ranging from 20 μm to 180 μm using SU-8, (100 holes of each size), and determined how many were left open after printing. The minimum printable hole diameter was 120 μm in the design file, but the printed diameter was between 65 μm and 100 μm due to the viscosity of the SU-8. Ninety-nine percent of the holes of this size were open.

A test structure was printed with one via hole in the insulating layer connecting a top conductor to a bottom conductor.



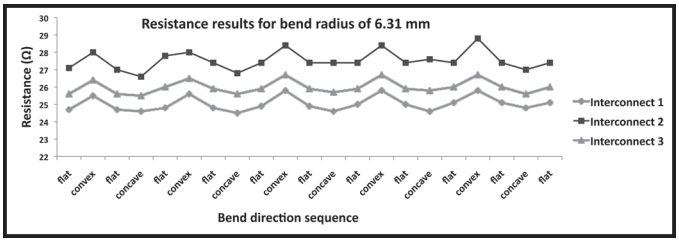


Figure 2, top: Resistance of test structure during first bend test sequence.

Figure 3, bottom: Resistance of test structure during second bend test sequence.

A digital multimeter was used to measure the resistance of the test structure. The structure was then wrapped around cylindrical rods of different radius, and a multimeter was used to measure the resistance at each bend radius.

Finally, a multilayer daisy-chain test structure was constructed to demonstrate continuity through multiple interconnects, and insulation between unconnected conductors.

Results:

The measured resistance of the test structure was 34.33 Ω. Assuming an average thickness of 0.4 μm [1] we calculated the resistivity to be 4.08×10^{-8} Ω.m and the sheet resistance to be 0.10 Ω/square. These values are both well within the range of published specifications for silver ink [1], however, they can be further improved by optimizing the annealing conditions.

Resistance of the test structure increased with decreasing convex bend radius, as expected, with slight decreases for concave bending (Figure 2). A large increase in resistance was observed in the flat state after concave bending. The increases in resistance were due to silver particles in the via being stretched apart, and the decrease in resistance for concave bending was due to the particles being compressed and forming a stronger contact [2].

An additional bend test was performed using a single bend radius of 6.31 mm in order to determine whether resistance would stabilize or continue to increase with repeated bending. Small fluctuations in resistance in the bent positions were observed, but resistance in the flat position stabilized for the last three to five measurements (Figure 3).

The daisy-chain structure successfully demonstrated continuity between interconnected conductors with acceptable resistance, and insulation between unconnected conducting layers.

Conclusions:

Our goal of developing a fully inkjet printed interconnection process for flexible electronics was successfully achieved. The via hole size was small enough to fit our constraints and the resistance of the interconnects proved to be stable with repeated bending. Unlike current interconnection methods, this process is completely additive and no chemicals are needed to remove material. This process can be implemented using a high speed roll-to-roll printer for high throughput manufacturing in the future.

Acknowledgments:

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References:

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[2] Pham, et al., "Self-aligned carbon nanotube thin-film transistors on flexible substrates with novel source-drain contact and multi-layer interconnection," IEEE Trans. Nanotechnol. vol 11, no. 1, pp 44-50, 2012.