

MOSFET: Fabrication Process and Performance Analysis

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Abstract:

The focus of this project was to determine the optimal gate region wet etch time, using the trench method, for the metal-oxide semiconductor field-effect transistor (MOSFET) fabrication process. The gate region, or trench, etching was time-dependent because too little time resulted in short-circuiting devices, while too much time resulted in lower-performing devices. The semiconductor parameter analyzer (SPA) examined the transistors' efficiency by generating current-voltage (I-V) graphs. No devices were successfully produced, but the optimal etching time range was found to exist between 15 and 25 seconds for this project's sample composition.

Introduction:

Scaled MOSFETs enable electronics to be made smaller and consume less power. Nanotechnology researchers solve problems that arise during the attempt to scale down the transistors, decreasing transistors' threshold voltages V_{TH} . With lower V_{TH} , devices have the capability to consume lower amounts of power, resulting in greater device efficiency. The most significant problem associated with this project was the etch stop thickness. Effective etch stops are at least 5 nm thick,

preventing etchants from penetrating through the surface. Since the samples' layer was 2 nm thick, the mordant etched through the indium gallium arsenide (InGaAs) and the indium phosphide (InP) of the gate region. Caution was taken to ensure that the etching removed the etch stop, without penetrating into the channel region. By alternating the trench etch time with multiple samples, an optimal gate region etch time was attempted to be found and employed for future processes.

Experimental Procedure:

The trench method consisted of four photolithography stages: isolation, gate region definition, gate metal deposition, and source/drain metal deposition. During each photolithography step, masks containing prints for a set of devices were used to expose the same print multiple times on the samples. Each print was designed for approximately 100 devices, and the total transistor count for each sample varied depending on the wafer size. The isolation process involved dry etching into the hard mask and wet etching the sample, using substance ratios of one part phosphoric acid (H_3PO_4): one part hydrogen peroxide (H_2O_2): 25 parts water (H_2O), until the etch level was in the barrier. This defined the active area of each device and varied the channel widths (5-25 μm). The gate region definition stage consisted of dry etching into the hard mask, and wet etching, using the same mordant from isolation, into the contact and etch stop layers of the exposed devices. This etching phase determined the channel lengths (0.3-1.0 μm); the etching was controlled by time, due to the thin etch stop layer.

The third photolithography step occurred after the hard mask removal, approximately 4 nm hafnium oxide (HfO_2) deposition, and 15 minute annealing at 400°C with forming gas purging. Following the oxide annealing, gate metal — nickel (Ni) — was deposited above the trench region, including the sides along the device for functioning and measurement purposes. The excess Ni was lifted-off and the last photolithography step protected areas where the source/drain metals were not supposed to cover. Hydrofluoric acid (HF) was used to remove some oxide in order to establish contact sites for the source/drain metals.

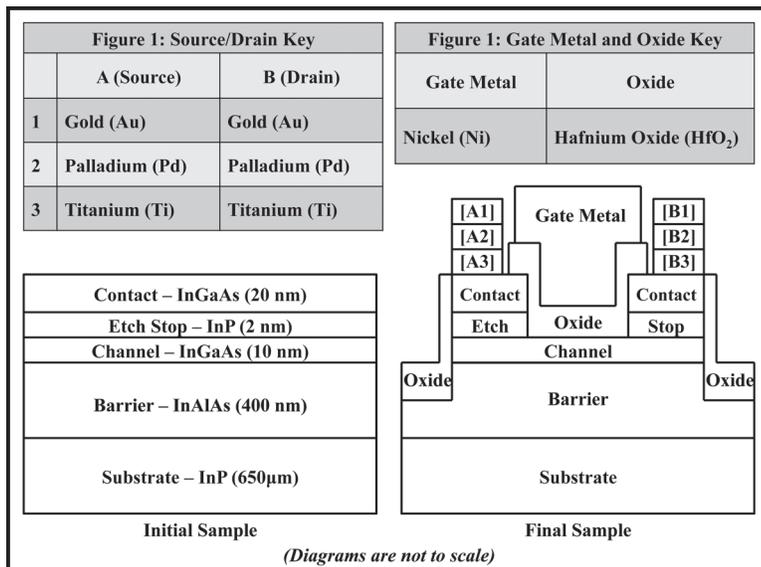


Figure 1: Initial and final stages of the MOSFET fabrication process.

Etch Time and Deposition Summary					
	Gate Region Etch Time	Oxide Deposition	Gate Metal Deposition	Source/Drain Metal Deposition	Measured by SPA?
Sample 1	10 seconds	3.5 nm HfO ₂	64 nm Ni	25 nm Ti/ 30 nm Pd/ 50 nm Au	Yes
Sample 2	15 seconds	3.5 nm HfO ₂	64 nm Ni	25 nm Ti/ 30 nm Pd/ 50 nm Au	Yes
Sample 3	25 seconds	3.5 nm HfO ₂	75 nm Ni	N/A	No
Sample 4	25 seconds	4.5 nm HfO ₂	95 nm Ni/ 75 nm Au	N/A	No

Figure 2: Summary of the samples' etching times and deposition thicknesses.

The source/drain metals — titanium (Ti), palladium (Pd), and gold (Au) — were deposited onto the sample, and the final lift-off removed the excess metal. Ti was deposited for its n⁺ contact properties, Pd for its ability to prevent gold diffusion into the semiconductor [1], and Au for its non-oxidizing properties (Figure 2).

Results:

A total of four samples were fabricated during this research project. The first process consisted of two samples that experienced gate region etch times of 10 and 15 seconds. These wafers were tested with no gate voltage and their I-V graphs suggested resistor-like behaviors (see Figure 3). These results led to another process, consisting of a sample with 25 seconds of trench etching. Following gate metal deposition, the sample was examined under the scanning electron microscope (SEM): the gate metal along the sides of the devices did not connect to the Ni above the channel (see Figure 4); voltage could not be applied to the gate without potentially damaging the metal. The last sample also underwent 25 seconds of trench etching, but the gate metal and source/drain photoresist was lifted off during the oxide etching with HF. This unexpected result may have been due to poor photoresist development.

Conclusions:

Although no working transistors were produced, the experimental results obtained will help future researchers. The optimal gate region wet etch time was found to exist between 15 and 25 seconds after attempting to fabricate four samples. The maximum time was observed because the 15-second sample underwent another procedure: the HfO₂ was removed and the devices were wet etched for 10 additional seconds. No current was conducted through the devices when no gate voltage was applied.

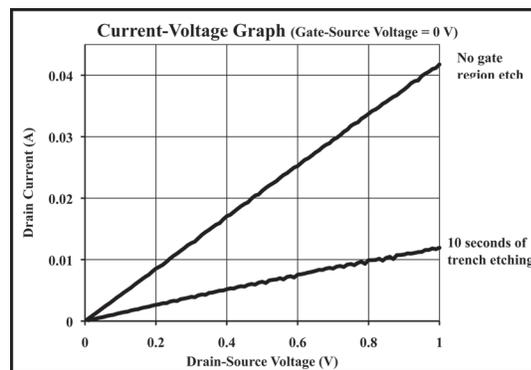


Figure 3: Performance comparison between a trenchless device and a 10-second etched device.

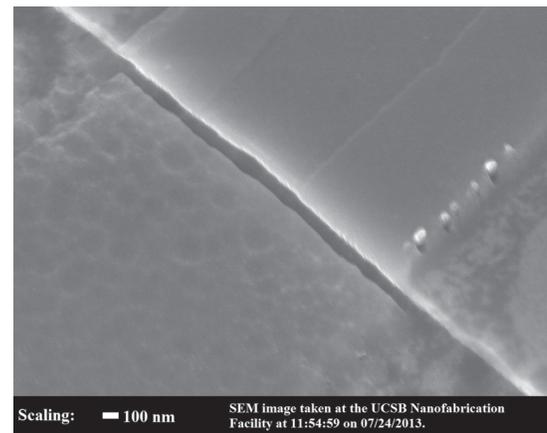


Figure 4: SEM of the third sample's gate metal discontinuity.

Scientific investigators can continue to construct MOSFETs, knowing they can achieve functioning devices with 25 seconds of etching, or they can alter the etch time parameter to define the most optimal trench etch time. Despite the knowledge this research provides, these results do not guarantee perfect-working devices; rather, this information improves the chances of fabricating more efficient MOSFETs.

Acknowledgements:

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- [1] Brown, D.. "Pd Plating (electroplating) - Palladium per Mil-P-45209." Palladium Plating. Professional Plating, 2008. Web. 19 Aug. 2013.