Studying the Effect of Materials and Processing on the Electrical Properties of Bilayer Al / Amorphous CoTiN Metal Gates for Advanced Nanoelectronic Devices

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ELEC

Abstract:

Amorphous metal gate stacks present several advantages over traditional polysilicon gate stacks, including lower electrical resistivity and the elimination of polysilicon depletion and boron penetration effects. Recent use of amorphous metal gates in complementary metal oxide semiconductor (CMOS) integrated circuits have been shown to enhance their electrical properties by reducing work function and threshold voltage variability [1]. Additionally, amorphous metal gates are expected to exhibit enhanced diffusion barrier properties, which would stabilize the work function by preventing metal interdiffusion. However, amorphous gate mechanics have yet to be fully investigated. Understanding the effect of structure, materials, and processing on the electrical properties of transistors as well as optimizing the gate stack remain a challenge. The goal of this project was to study such effects in a bilayer metal gate structure consisting of aluminum (Al) as an upper layer and either polycrystalline titanium nitride (TiN) or partially amorphous cobalt titanium nitride (CoTiN) as a bottom layer. This would be done by comparing the diffusion barrier properties of the CoTiN gates to those of the TiN gates by measuring capacitance-voltage characteristics with varying thickness and annealing temperature. The extracted work function could then be used to determine if the amorphous gates effectively resist Al diffusion and prevent threshold voltage fluctuation, properties essential to increasing operational speed and efficiency in industrial nanoelectronic devices.

Experimental Procedure:

Several bilayer metal gate stacks consisting of a 50 nm Al upper layer and a polycrystalline TiN or amorphous CoTiN layer underneath with varying thickness (1-50 nm) were fabricated. The metals were deposited via sputter deposition onto a step-etched HfO_2/SiO_2 dielectric (with 2 nm of atomic layer deposited hafnium dioxide, HfO_2, and 5-20 nm of thermally grown silicon dioxide, SiO_2) on a Si substrate.

Following deposition, the structures were etched and patterned into 200 μm diameter capacitors using standard lithography techniques. The wafers were coated with 1.6 μm of machine-spun Shipley 3612 positive photoresist, masked and patterned under high-intensity UV light, and then developed to strip away the weakened photoresist. The exposed Al was etched away using Al etchant, and the TiN or CoTiN metal underneath was dry etched with $CHCIF_2$ (Freon 22) plasma. The remaining photoresist was then removed using a PRS3000 wet etch. Following the lithography procedure, hydrofluoric acid was used to remove the back oxide, thus improving the wafer back contact.

Inspection by optical microscope revealed that most samples sustained damage during etching and lithography procedures, possibly related to gas contamination or gas leakage in the system as observed from the plasma color differences during etching. Damages incurred by the capacitors included over-etched capacitor boundaries as well as thread-like projections from inner and outer rings, both of which could have degraded capacitor functionality.

Fortunately, one sample of Al on 6 nm of CoTiN remained unaffected by the etching and lithography problems. This sample was used to measure the change in work function as a function of annealing temperature. Figure 1 shows the undamaged and completed sample.

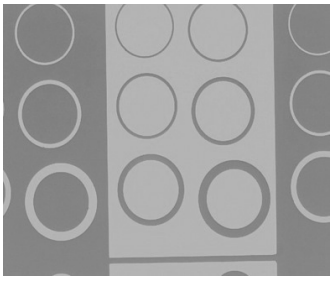

Figure 1: Salvageable Al / CoTiN (6 nm) capacitors as-deposited.

The capacitance-voltage (CV) characteristics of this sample were then measured using a bipolar bias sweep from 4V to -2.5V and back. These characteristics were used to determine several device parameters such as flatband voltage and equivalent oxide thickness, which can be used to calculate the work function as described in Reference 2.

CV characteristics for each oxide thickness of the sample were measured as-deposited and again after 300°C, 400°C, and 500°C anneals in forming gas for 20 min. Measurements were taken at 10 kHz, 100 kHz, and 1 MHz to confirm consistent device operation. Figure 2 represents CV measurements obtained from the sample after a 300°C anneal.

Flatband voltage is the voltage corresponding to the flatband capacitance; equivalent oxide thickness was derived from the maximum capacitance. Figure 3 represents a plot of flatband voltage as a function of equivalent oxide thickness.

By the equation used to calculate the metal work function, extrapolating a linear regression of flatband voltage versus equivalent oxide thickness gives the work function difference between the metal and the semiconductor. Adding the calculated work function of the semiconductor to this value yields the CoTiN work function for a particular anneal condition. Following this method, the CoTiN work function was extracted for each anneal condition and plotted with respect to annealing temperature in Figure 4.

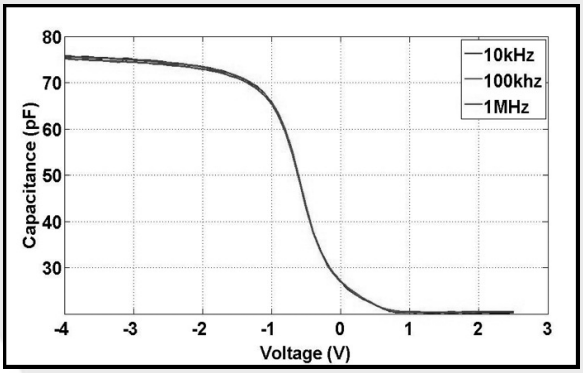

Figure 2: Capacitance-voltage characteristics of the Al / CoTiN (6 nm) sample.

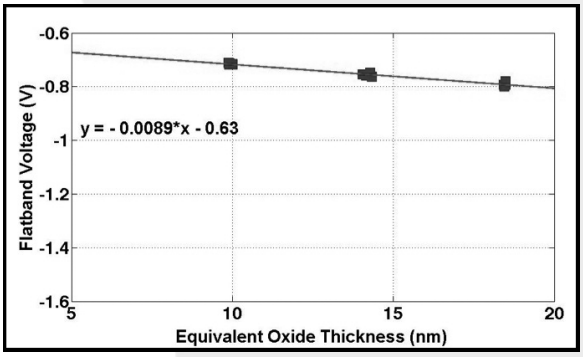

Figure 3: Plotting flatband voltage against equivalent oxide thickness is used to calculate the CoTiN work function.

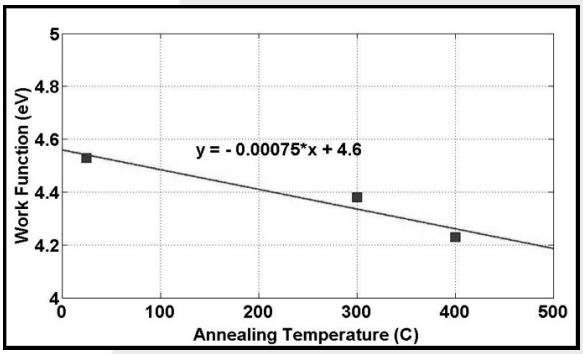

Figure 4: CoTiN work function plotted against annealing temperature shows a decrease with increasing temperature.

Results and Conclusions:

The obtained results illustrate that the CoTiN metal work function nominally decreases with an increase in annealing temperature. Possible explanations include:

- Ineffective Al diffusion prevention,
- Annealing of interface defects,
- Structural changes in CoTiN during the annealing process, and,
- Interaction between dielectric and CoTiN interface.

The effectiveness of CoTiN as a diffusion barrier remains unclear. While results do indicate a change in work function of approximately 0.3 eV, this difference is relatively small compared to silicon's band gap and could be affected by any combination of the reasons cited. Further experimentation on the effects of thickness on the CoTiN work function as well as comparison to polycrystalline metals are needed to establish amorphous CoTiN barrier properties and its use as a gate material for industrial applications.

Acknowledgements:

Metal Gate Research Group: Prof. Bruce Clemens, Prof. Yoshio Nishi, Dr. Michael Deal, Dr. Jim McVittie, Ranida Wongpiya, Joanie Ouyang. REU Program Administrators: Dr. Michael Deal, Maureen Baran. Stanford Initiative for Nanoscale Materials and Processes. Stanford Center for Integrated Systems. National Science Foundation. National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program.

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Optimization of Hybrid Fuel Cell Designs and Materials

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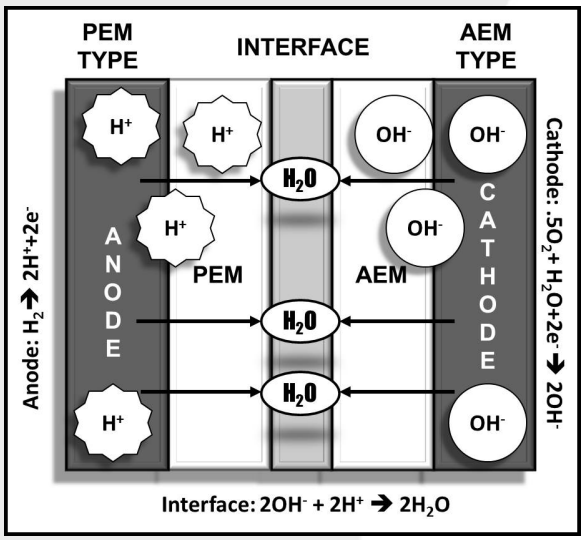

Figure 1: The membrane electrode assembly and hybrid fuel cell electrochemical reactions are shown.

Introduction:

A hybrid fuel cell (HFC) produces electricity by means of an electrochemical reaction. The membrane electrode assembly (MEA) and electrochemical reactions are shown in Figure 1. The hybrid fuel cells studied combine elements from a proton exchange membrane (PEM), which only conducts protons, and an anion exchange membrane (AEM), which only conducts hydroxides. HFCs have the potential to provide quiet, efficient, and zero emissions energy without the need for a water management system. Some problems with HFCs are expensive components such as platinum catalysts, low performance values, and AEMs that are not durable.

The main focus of this research was on the interface material that is positioned between the PEM and AEM in the fuel cell. This region is important because it provides the adhesion between the AEM and PEM, and water is created at this interface when the hydrogen and hydroxide ions combine. Two hybrid fuel cells were assembled with different interface materials. The interface material in HFC 1 was a polymer that interacts with hydrogen and hydroxide ions. The interface material in HFC 2 was a hydroxide conductive ionic liquid. Voltammetry, impedance spectroscopy, and chronoamperometry were the electrochemical analyses performed on both cells to determine which interface material works better.

Experimental Procedure:

The cathodes and anodes were made using the recipe described in the literature, except the AEM cathode was made with toluene instead of dimethylformamide [1]. The material used as the PEM was Nafion® 117 and the material used for the AEM was Tokuyama a201. To assemble the MEA for HFC 1, the electrodes were sprayed with ionomer solution. The PEM was sprayed with neutral epoxy, ionomer interface material, which was made of polynorbornene, Nafion ionomer, and trimethylolpropane triglycidyl ether. The electrodes, PEM, and AEM were then stacked on top of each other in the order shown in Figure 1 and put into the hot press for 10 minutes at 2 MPa and 212°C to bond the layers together.

The same procedure was used to make the MEA of HFC 2 except the PEM was sprayed with ionic [bmim][OH] interface material. During the electrochemical analysis, each fuel cell was connected to a FCT 150S test station and a PARSTAT 2773, which is a combined potentiostat and galvanostat. The fuel cell test station and FC Lab V5.22 software were used to control the fuel cell temperature, relative humidity, and gas flow. The potentiostat was used to perform the voltammetry, impedance spectroscopy, and chronoamperometry. All of the electrochemical analyses were performed at 100% R.H and 55°C. At the anode, hydrogen flowed in at 10 mL/min. At the cathode, oxygen flowed in at a rate of 25 mL/min.

Results:

The voltammetry results for the HFCs are shown in Figure 2. The max current density for HFC 1 was 28 mA/cm^2. The max current density for HFC 2 was 38 mA/cm^2. HFC 1 produced 3.9 mW/cm^2 and HFC 2 generated 5.1 mW/cm^2. The power density indicates how many watts are produced per square centimeter of MEA. Chronoamperometry was performed on each HFC for five hours. The results are shown in Figure 3. HFC 1 produced a steady 0.05 A. HFC 2 produced an initial 0.13 A, then dropped to a steady 0.11 A.

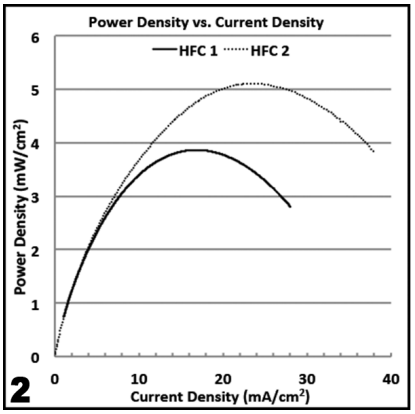

Figure 2: The results of the voltammetry experiment for HFC 1 and 2 are shown.

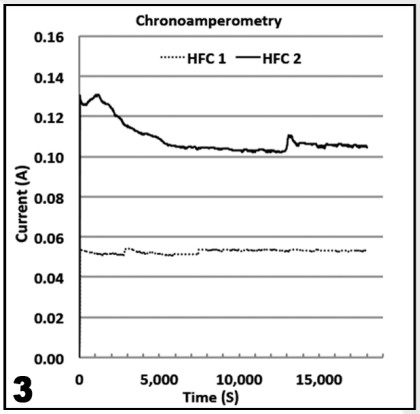

Figure 3: The chronoamperometry results of both HFCs are shown in the graph. The experiment was run for five hours.

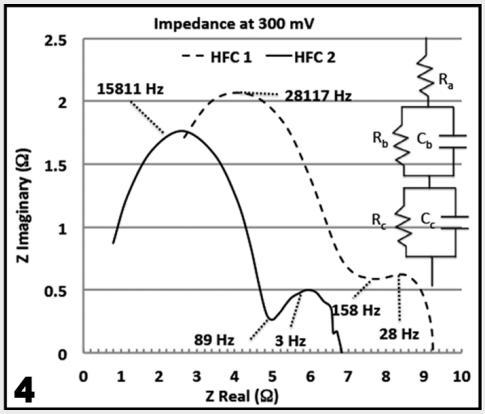

Figure 4: The chart shows the impedance spectroscopy results for both of the HFCs. The HFCs were tested at the same frequencies 0.05 Hz – 88913 Hz. Both HFCs have the same equivalent circuit shown in the graph.

It is believed that HFC 2 generated a large current because it had less resistance than HFC 1. HFC 2's low resistance can be attributed to the conductivity of the [bmim][OH].

Impedance spectroscopy measurements were taken at 300 mV from 0.05 Hz - 88914 Hz. The impedance data is shown in Figure 4. The impedance data shows the membrane, anode, and cathode resistance. The length between the first data point and the y-axis is the membrane resistance in ohms. The radius of the first peak is the anode resistance. The radius of the first valley is the cathode resistance. Both of the HFCs had the same equivalent circuit that is shown in Figure 4. An equivalent circuit may have resistors, capacitors, and inductors, but low testing frequencies eliminated the need for inductors [2]. The equivalent circuit was refined until it produced impedance values that were similar to the experimental values. The equivalent circuit and the impedance data show that HFC 2 has less resistance, which means there is less power loss to resistance.

Conclusions:

Both of the HFCs performed better than previous designs without an interface material. The ionic [bmim][OH] interface material in HFC 2 performed better than the neutral epoxy and ionomer interface material in HFC 1 in all the electrochemical analyses. The impedance spectroscopy data indicates the [bmim][OH] decreases resistance in a HFC. It is believed the [bmim][OH] decreases resistance by conducting the incoming hydroxide ions better than a neutral interface material. The large steady current values and high power density of HFC 2 is a result of less resistance in the interface material.

In the future, it is likely that an HFC with a proton conducting interface material will be tested.

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Interlayer Dielectric and Interconnect for Heterointegration

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Introduction:

In order to vertically integrate heterogeneous electrical devices, compatible processes for interlayer dielectrics and metal interconnects are needed. The focus of this project was to study silicon dioxide (SiO_2) as an interlayer dielectric for heterointegration of two process technologies. The first step of this project was to develop and characterize a deposition process for high quality plasma enhanced chemical vapor deposition (PECVD) SiO_2 film by fabricating capacitors and testing film electrical characteristics. Once the dielectric was assessed to be viable, via etch hole and metal interconnect technologies were developed and characterized. Test structures were made to verify the electrical connection between the top contact of the bottom device and the bottom electrode of the top device. These test samples were followed by fabrication of the heterogeneously integrated devices. The ability to reliably integrate heterogeneous devices will enable new applications.

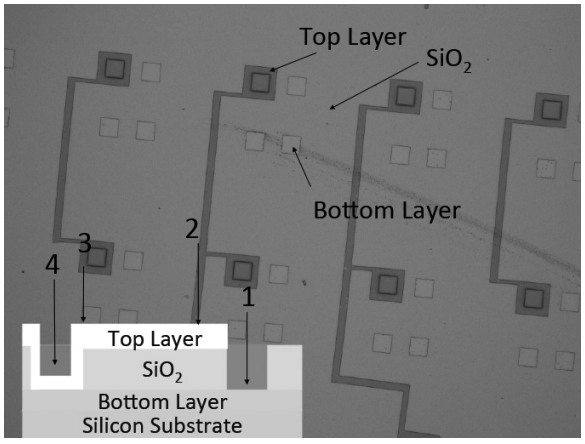

Figure 1: Structures for testing side wall coating of top metal. Numbers on the inset cross-section indicate test probe points for current-voltage measurements of Figure 3.

Experimental Procedure:

First metal-insulator-metal (MIM) capacitors were fabricated to identify a suitable dielectric film and to develop a deposition technique that would have a limited effect on previously fabricated devices existing on the substrate. Using PECVD, four different films were deposited on four 100 mm silicon wafers. Two were deposited at 200°C with thicknesses of 200 nm and 500 nm. These thicknesses were also deposited at 380°C. Tungsten was deposited using the LAB 18-02 PVD sputter tool and a shadow mask to form the top capacitor plates. Capacitance-voltage (C-V) and current-voltage (I-V) measurements were taken to determine film properties.

Once the 380°C film was determined to be a suitable dielectric, the etch rate of the film was characterized. The LAM 9400 was used for reactive ion etching (RIE) of SiO_2 with a power of 500W and gas flows of 8 sccm of SF_6, 50 sccm of C_4F_8, 50 sccm of He, and 50 sccm of Ar.

Next, test samples were fabricated to test the metal interconnects. A 100 nm film of aluminum (Al) was deposited on glass substrates followed by deposition of 1 μm SiO_2. The SiO_2 was etched to create vias to the Al layer. These etch holes were covered with top metal pads as shown in Figure 1. I-V measurements were performed to determine the resistance of the metal interconnect. Finally, the optimized SiO_2 film was used as a passivation layer between two sets of transistors.

Results:

From the C-V data measured on the MIM capacitors, the experimental dielectric constants of the SiO_2 films were calculated. Its value for the 380°C film was very close to the ideal value of 3.9 [1]. This indicated that the film was dense and of a fairly high quality. I-V measurements of leakage current

were also taken, and are shown in Figure 2. The 380°C film maintained a low leakage current throughout the sweep, indicating its functionality as an insulator, while the 200°C film had significantly higher leakage current. While the 200°C oxide would be preferred for low temperature processing, the low leakage of the 380°C film makes it a better choice for heterointegration [2].

As shown in Figure 3, the resistance present between the metal pad and the side of the etch hole was approximately 23.3Ω. The resistance between the top metal pad and the bottom of the etch hole was 87.9Ω — meaning that the resistance of the side wall was about 65Ω. This large increase in resistance was due to the method used to cover the side walls of the etch holes. The sputtered metal was thin relative to the dielectric layer and thus only a very thin coating was present on the side walls.

The resistance between the top metal pad and the bottom aluminum surface was measured to be 117Ω. Thus the resistance added by the contact between the two metals was only about 20Ω. This indicates both that there was a good connection between the two metals and that there was no SiO_2 at the bottom of the etch holes. Both of these are important requirements for heterointegration of two devices.

Using the SiO_2 passivation layer, two layers of functioning transistors were fabricated. Devices in the first layer maintained their functionality even after top device fabrication, and the top devices displayed switching behavior. Figure 4 displays the results of I-V sweeps on both a bottom and a top layer transistor.

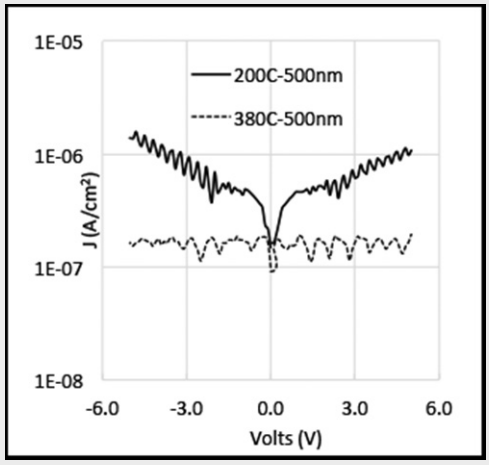

Figure 2: Average leakage current vs. voltage of 0.003 cm² SiO_2 MIM capacitors.

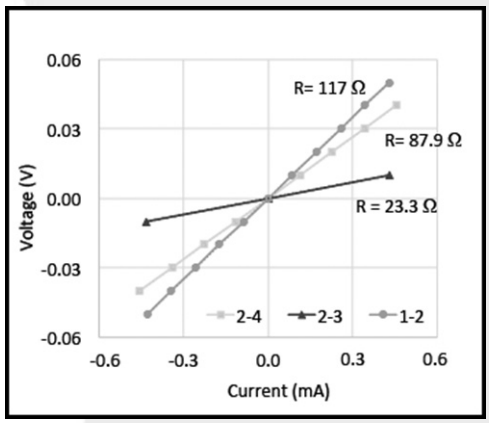

Figure 3: Resistance of metal interconnect test structures used to determine the quality of the metal vias.

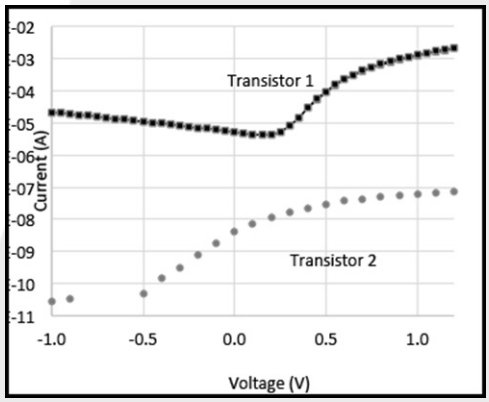

Figure 4: Measured drain current vs. gate voltage for one top layer and one bottom layer transistor. Both devices show field-effect behavior, indicating the successful heterointegration.

Conclusion and Future Work:

This experiment showed that SiO_2 is a suitable interlayer dielectric for the integration of two process technologies. A plasma etch was used to create openings in the SiO_2 down to the metal interconnect of the bottom device. Test samples showed that a thin metal layer could establish a reliable electrical connection through these etch holes to provide suitable vias for integrating top devices. Future work could be done to further improve the sidewall coverage and reduce via resistance. Two layers of functioning transistors were fabricated using a SiO_2 interlayer dielectric.

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Aluminum Oxide for Surface Passivation in Photovoltaics

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Abstract:

In order to study the influence of temperature and carrier injection on the surface passivation quality of p- and n-type silicon substrates, aluminum oxide thin films were deposited after cleaning as the surface passivation layer using atomic layer deposition. The minority carrier lifetime in each instance was then measured using a photoconductance lifetime tester with a variable temperature stage, both before and after annealing the samples. The results show a relationship between the increase in temperature and the increase in lifetime.

ELEC

Introduction:

Conversion efficiency within silicon solar cells is limited by recombination at the surface and recombination within the bulk defects, which together limit the amount of effective carriers in the cell and therefore the current and voltage output. Reducing surface recombination is especially important as wafers become thinner in order to reduce production costs. As the thickness decreases, the surface area to volume ratio greatly increases, and surface recombination becomes a leading limiting factor in efficiency.

The equation for effective lifetime is given by Equation 1, in which the first three terms on the right of the equation represent recombination within the bulk of the material. The last term represents the effect of the surface, where $S_{front/back}$ is defined as the surface recombination velocity (SRV) in cm/s and W is the wafer thickness. As thickness decreases, this last term becomes larger and to counteract this, the SRV must be increased through surface passivation.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} + \frac{S_{front/back}}{W}$$

Eq (1)

Experimental Procedure:

To start, 2-inch as-cut silicon wafers were cleaned using a piranha solution (sulfuric acid + hydrogen peroxide) followed by a saw-damage removal etch—both acid and alkaline chemistries were tried. The acid-based solution was a mixture of hydrofluoric acid, nitric acid, and acetic acid, and the alkaline-based solution was potassium hydroxide. Afterwards, RCA-b was used to remove any inorganic or metal contaminants on the surface. Finally, a hydrofluoric acid solution (BOE), was used to conclude the process. A BOE dip was repeated before any deposition was done in order to remove any surface oxides that may have formed.

After cleaning, atomic layer deposition (ALD) was performed using trimethyl aluminum as a precursor. This technique allowed for the controlled and conformal deposition of single monolayers on the surface of the silicon wafer. After depositing approximately 30 nm of aluminum oxide on both sides, the samples were annealed in a box furnace with a nitrogen atmosphere for 30 minutes at 425°C [1]. Minority carrier lifetime was measured by photoconductance decay using a WCT-120TS lifetime tester over a temperature range of 50°C to 230°C and an injection level 1×10^{14} to 1×10^{17} cm^{-3}.

Results and Conclusions:

Lifetime measurements were performed for both p-type and n-type Si wafers. Figures 1 and 2 show the variation of lifetime (y-axis) with injection level (x-axis) and temperature. In both graphs, the lifetime is seen to increase parabolically as minority carrier concentration increases, with maximums around 10^{15} cm^{-3}. Lifetime is also seen to increase with temperature despite the wafer type involved. These results are consistent with previous observations from other authors [2-4]. The trend with increasing temperature is expected since the additional energy imparted to the samples in the form of heat helps to fill empty levels in the band gap, therefore reducing the amount of possible recombination.

The n-type wafer was analyzed in further detail, with lifetime values reaching as high as 500 μs. The relationship between the inverse of effective lifetime and the inverse of wafer thickness taken for various wafer thicknesses at 200°C is shown in Figure 3. As depicted by Eq (1), this plot puts in evidence the

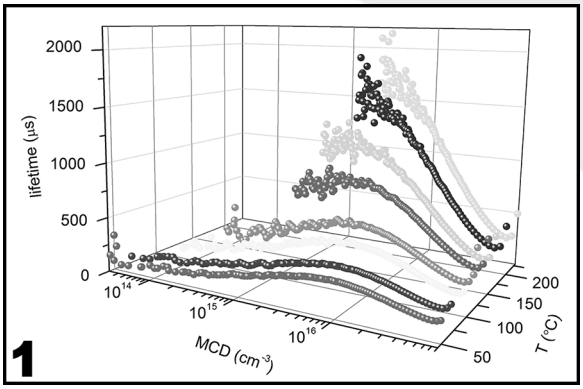

Figure 1: Lifetime versus temperature and injection level for a p-type c-Si wafer with an ALD Al_2O_3 layer. (See full color version on page xxxvi.)

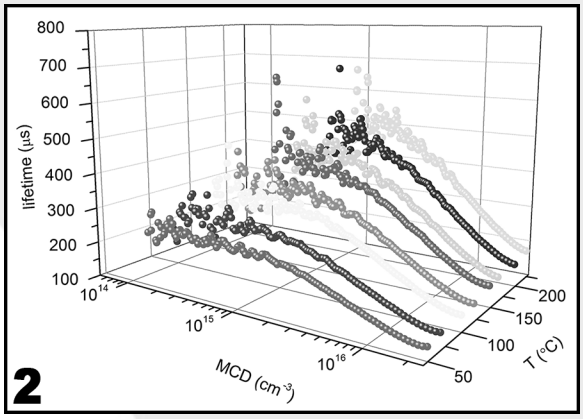

Figure 2: Lifetime versus temperature and injection level for an n-type c-Si wafer with an ALD Al_2O_3 layer. (See full color version on page xxxvi.)

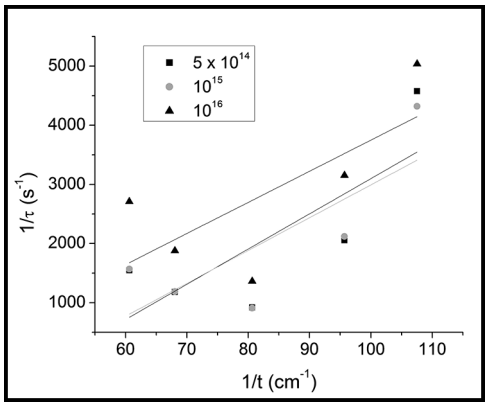

Figure 3: Inverse of lifetime versus inverse of wafer thickness measured at 200°C for n-type c-Si deposited with Al_2O_3 as wafer thickness was reduced. The slope represents the SRV.

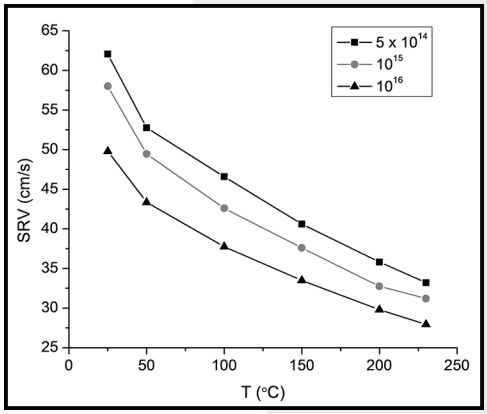

Figure 4: SRV versus temperature for n-type c-Si deposited with Al_2O_3.

SRV achieved with this passivation layer. The temperature was then plotted against the various SRV, found for 10° intervals over the measured temperature range, shown in Figure 4. From this graph, the dependence of SRV with temperature is clear and will be the base for future modeling efforts.

Future Work:

Initially, the type of passivation (chemical or field effect) must be studied. These results will then be used to develop a model for the relationship between SRV and temperature for various passivation layers (Al_2O_3, SiN_x, SiO_2). This will enable the subtraction of the surface effects from the effective lifetime, which ultimately will help characterize the high quality bulk silicon underneath.

Acknowledgements:

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Fabrication of Five-Terminal Laterally-Actuated Nano-Electro-Mechanical (NEM) Relays

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Abstract:

Nano-electro-mechanical (NEM) relays offer reliable alternative switches with low leakage current compared to MOSFETs. In a NEM relay, applying voltage to a gate electrode causes electrostatic force to mechanically actuate a beam, which makes contact between source and drain electrodes, allowing current to flow. One of the present drawbacks of NEM relays is that the pull-in voltage at which the switch actuates is extremely high (~20V). This project focused on a laterally-actuated (in the plane) cantilevered relay and investigated how parameters at different fabrication steps affected the relay's pull-in voltage. The body and electrodes of the relay were fabricated by first growing silicon dioxide on a silicon wafer, depositing polysilicon, and defining the physical features with electron-beam lithography. A layer of titanium nitride was then deposited and etched. Finally, the beam was released from the surface of the wafer by etching with hydrofluoric acid. Parameters such as deposition temperatures and etch times were varied in an effort to produce a durable, lower pull-in voltage relay. Lower pull-in voltages in NEM relays would be a step towards integrating the devices into ultra-low-power applications such as computing.

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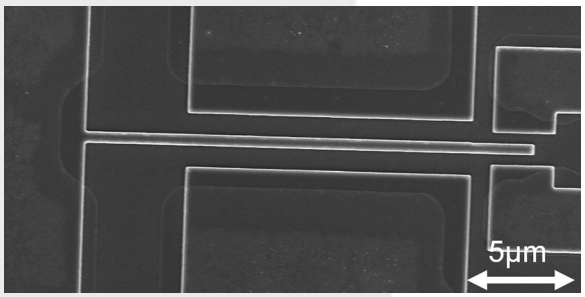

Figure 1: SEM image of a completed NEM relay. At the left is the device source, to which the beam is attached. Gates are in the middle top and bottom, and drains are at the right. Beam-to-gate gaps are 1000 nm and beam-to-drain gaps are 500 nm.

Introduction:

The most common form of logic switch today is metal-oxide-semiconductor field-effect transistors (MOSFETs). As MOSFETs are scaled down for faster computing, leakage current will flow through the device even in its "off" state. Nano-electro-mechanical (NEM) relays promise no leakage current and faster switching behavior than MOSFETs [1]. Similar to MOSFETs, a basic NEM relay requires three terminals: source, drain, and gate. Applying a sufficiently high pull-in voltage to the gate generates enough electrostatic force to move a beam, connected to the source, to contact the drain, allowing current to flow through the device. One of the present drawbacks of NEM relays is an extremely high pull-in voltage, approximately 20V in literature [2].

In this project, we demonstrated a five-terminal NEM relay with two drains and two gates. A finished device is shown in Figure 1. The laterally-actuated beam moved in the plane of the wafer on which the device was fabricated. The goal of this project was to investigate the effects of varying certain processing steps to create a device with a lower pull-in voltage and other properties favorable for ultra-low-power application.

Procedure:

Fabrication began by growing 400 nm of silicon dioxide (SiO_2) and depositing 400 nm of polycrystalline silicon (polysilicon). The polysilicon was then patterned using electron-beam lithography (EBL) and etched anisotropically with plasma. Next, 20 nm of titanium nitride (TiN) was deposited using atomic layer deposition (ALD). The TiN was patterned with another round of EBL and etched anisotropically with plasma. This anisotropic etch removed TiN from horizontal surfaces, exposing the underlying SiO_2, but left TiN on vertical sidewalls intact. Because we needed to determine a suitable etch recipe for TiN, we etched four separate samples for 60s, 90s, 120s, and 150s. Finally, the device was finished by etching the now-exposed oxide using 20:1 buffered oxide etch

(BOE) and drying the samples in a critical point dryer, releasing the beam. Finished devices were tested using a three-point probe measurement, with source voltage grounded, drain voltage held at 0.5V, and gate voltage varied between 0 and 25V. Devices were also imaged under a scanning electron microscope (SEM) after several fabrication steps. After examining and testing the four samples, an additional sample was prepared, with TiN etched for 150s.

Results and Discussion:

From SEM images, the 60s TiN etching samples seemed best etched, as shown in Figure 1. In contrast, the 90s, 120s, and 150s TiN etching samples (Figure 2) had unetched TiN remaining between the gates and drains. As seen in the tilted SEM image in Figure 3, underetching was apparent from tilted SEM images, but it was unclear whether the beams were fully suspended during HF etching. Measurements on the samples with 60s TiN etching revealed that current would always flow through the device. Our conclusion was that 60s was too short of an etch time, leaving a conductive layer of TiN all over the device. Measurements on the samples with 150s TiN etching were also inconclusive, as the leftover TiN between the gates and drains created a short circuit that left us unable to measure the current flowing between the source and drain. We concluded that the samples with 150s, 120s, and 90s TiN etching were unsuccessful due to problems in the TiN etching. Oddly, the second 150s TiN etch sample did not have leftover TiN for reasons yet undetermined.

Future Work:

Further investigation is needed to improve the TiN etching. Once working samples have been completed, we then need to measure pull-in voltages using the three-point probe measurement described above. Moving forward, we will further explore fabrication techniques to further decrease the pull-in voltage of these laterally-actuated NEM relays, such as varying device geometries (e.g., gaps between features, beam shape) and integrating with other technologies.

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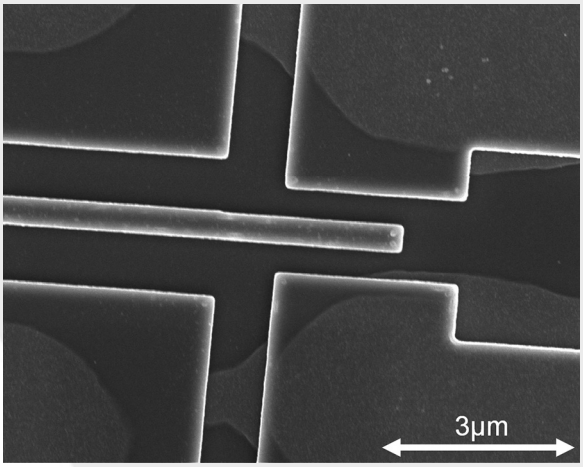

Figure 2: SEM image of a 120s TiN etching sample. TiN is visible in the lighter regions and on the reflective sidewalls. TiN remains on the surface between drains and gates.

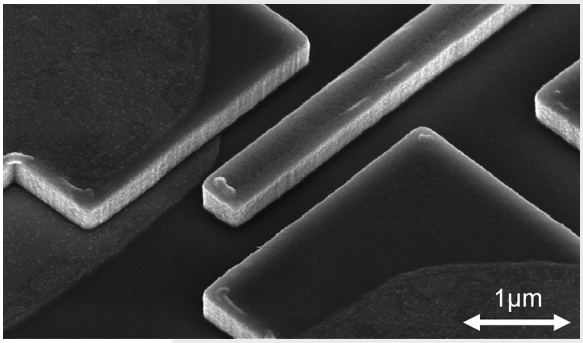

Figure 3: SEM of a 90s TiN etching sample, tilted 38°. Dark shadows under the features indicate some etching by HF.