The Effect of Low Temperature Growth and Annealing on the $Al_2O_3/In_{0.53}Ga_{0.47}As$ Interface

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Abstract:

This work summarizes the characterization of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface grown and annealed at low temperature. Samples were pretreated using atomic layer deposition (ALD) cycles of N*/TMA, then ~ 3-6 nm of Al_2O_3 were grown using ALD and furnace annealed to passivate the interface. Varying the annealing process found that a 250°C forming gas anneal, nearly independent of time, gave the best interface. Additionally nine cycles of N*/TMA was found as the optimum pretreatment giving a maximum midgap D_{it} of $6.85 \pm 0.37 \times 10^{12}$ $cm^{-2}eV^{-1}$. Though a better quality Al_2O_3 film and aluminum oxide/indium gallium arsenide (Al_2O_3/InGaAs) interface are achieved at higher temperature, these results show acceptable D_{it} and C-V behavior for use when low temperature processing is necessary.

Introduction:

$In_{0.53}Ga_{0.47}As$ is the leading candidate for post-Si n-channel technology partially due to its low effective electron mass. Additionally, high-κ dielectrics, like Al_2O_3, grown by atomic layer deposition (ALD) are being explored as gate oxides to prevent current leakage while maintaining high capacitances. However, high surface and interface defect concentrations lead to a high interface trap density (midgap D_{it}) at the Al_2O_3/InGaAs interface. Previous work has shown that *in situ* surface pretreatments using alternating cycles of nitrogen plasma and trimethylaluminum (N*/TMA) can successfully passivate the interface for a 300°C growth and 400°C furnace anneal [1]. However, material limits make it desirable to modify this passivation technique for low temperature processing, working with growth temperatures near 115°C and a maximum annealing temperature of 250°C.

Experiment:

InGaAs/InP samples were initially cleaned using a three minute buffered HF dip in order to remove any surface contaminants. An ALD reactor (Oxford Instrument FlexAl) was used for an *in situ* surface pretreatment and Al_2O_3 growth. The surface was pretreated using N*/TMA cycles, five to nine times, at 115°C. This pretreatment allows for the removal of native oxides and the initial passivation of the InGaAs surface. Immediately following the pretreatment, ~ 3-6 nm of Al_2O_3 was grown using cycles of TMA and water vapor. Al_2O_3/InGaAs samples were then post annealed in either a forming gas or N_2 environment for different times and temperatures below 250°C. Ni contacts (80 nm thick) were then deposited by thermal evaporation using a shadow mask. A Cr/Au contact (20/100 nm) was deposited on the back of the InP substrate in order to form the metal-oxide-semiconductor capacitors (MOSCAPs) used for electrical measurements. The MOSCAPs were tested using a two-point probe measurement to determine capacitance density and conductance as a function of gate voltage between 1 kHz and 1 MHz.

Results and Discussion:

Conductance and capacitance data was use to analyze the quality of the Al_2O_3/InGaAs interface. The optimum pretreatment and annealing conditions can be found by minimizing the frequency dispersion, but more importantly the midgap D_{it} response. The frequency dispersion is the difference in capacitance between 1 kHz and 1 MHz. This should be minimized both in the accumulation (high bias) and transition regions as seen in Figure 1. A high frequency dispersion can be a sign of a film with high trap densities, currently leakage, and channel resistance, which limit device speed and cause break down at high bias [2]. In addition to this, we want to minimize the midgap D_{it}, which is the quantitative estimate of the interface trap density in the InGaAs midgap. The "conductance" method described in Reference 3 uses the measured capacitance and conductance to calculate the D_{it} at 1 kHz.

Figure 2 shows the frequency dispersion as a function of annealing conditions. The lowest frequency dispersion of 2.5 $\times 10^{-8}$ F/cm^2 for the transition and 1×10^{-7} F/cm^2 for accumulation is found for a 15 minute, 200°C furnace anneal in a forming gas environment. However, the D_{it} response (Figure 3) is high for the 200°C case at about $1.1.10^{13}$ cm^{-2}/eV.

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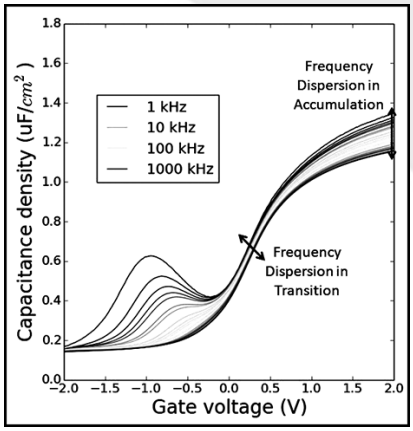

Figure 1: Example C-V curve for Al_2O_3/InGaAs MOSCAP. Frequency dispersion should be minimized in transition and accumulation regions. (See full color version on page xxxvi.)

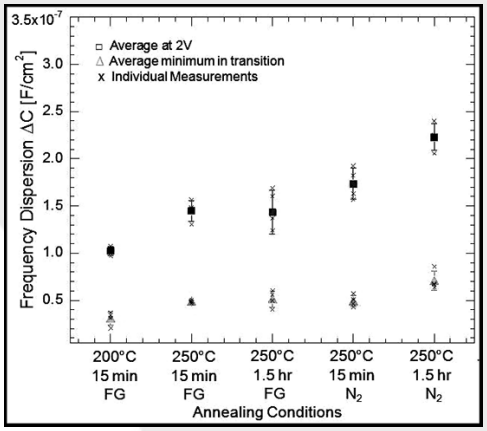

Figure 2: Frequency dispersion in accumulation and in transition versus annealing conditions. Samples were furnace annealed between 200°C and 250°C for 15 to 90 min in either a forming gas (5% H_2/95% O_2) or N_2 environment.

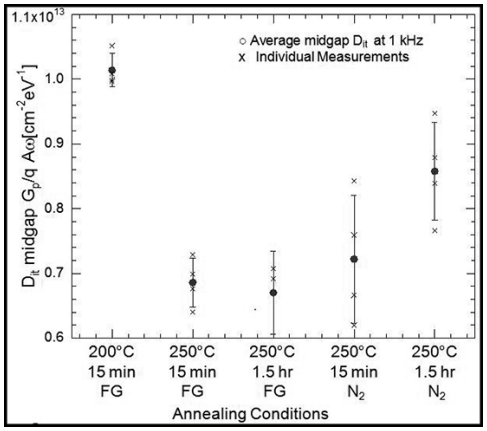

Figure 3: Midgap D_{it} response (estimate of interface trap density) versus annealing conditions.

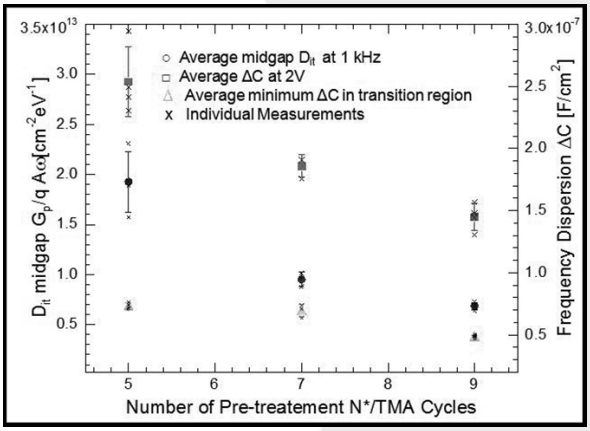

Figure 4: Midgap D_{it} response, frequency dispersion in accumulation, and frequency dispersion in transition versus number of N/TMA* in situ *pretreatment cycles.*

A 250°C forming gas anneal gives the lowest D_{it} response with little time dependence.

The frequency dispersion and midgap D_{it} response were also compared to find the optimum number of pretreatment cycles. Figure 4 shows that nine cycles N*/TMA is clearly the best condition for surface cleaning. It is possible that greater than nine cycles could give slightly better D_{it} results, but it is more likely that additional plasma exposure would damage the InGaAs surface.

Conclusions and Future Work:

It has been shown that it is possible to grow quality Al_2O_3 by ALD even at 115°C. C-V data show reasonable behavior with acceptable levels of current leakage. Additionally, a midgap D_{it} of 6.85 ± 0.37 × 10^{12} $cm^{-2}eV^{-1}$ has been achieved for a 250°C forming gas anneal with nine cycles of a N*/TMA *in situ* pretreatment. High temperature processing has reported midgap D_{it} values around 2 × 10^{12} $cm^{-2}eV^{-1}$ after optimization, but this result is still acceptable when low temperature processing is desired [1].

In the future, work may be done to further optimize this recipe by varying the plasma conditions during pretreatment. Additionally, further surface imaging has been started using AFM and SEM to better understand the film morphology and the affect of annealing time.

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References:

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