Aluminum Oxide for Surface Passivation in Photovoltaics

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Abstract:

In order to study the influence of temperature and carrier injection on the surface passivation quality of p- and n-type silicon substrates, aluminum oxide thin films were deposited after cleaning as the surface passivation layer using atomic layer deposition. The minority carrier lifetime in each instance was then measured using a photoconductance lifetime tester with a variable temperature stage, both before and after annealing the samples. The results show a relationship between the increase in temperature and the increase in lifetime.

Introduction:

Conversion efficiency within silicon solar cells is limited by recombination at the surface and recombination within the bulk defects, which together limit the amount of effective carriers in the cell and therefore the current and voltage output. Reducing surface recombination is especially important as wafers become thinner in order to reduce production costs. As the thickness decreases, the surface area to volume ratio greatly increases, and surface recombination becomes a leading limiting factor in efficiency.

The equation for effective lifetime is given by Equation 1, in which the first three terms on the right of the equation represent recombination within the bulk of the material. The last term represents the effect of the surface, where $S_{front/back}$ is defined as the surface recombination velocity (SRV) in cm/s and W is the wafer thickness. As thickness decreases, this last term becomes larger and to counteract this, the SRV must be increased through surface passivation.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{Rad}} + \frac{1}{\tau_{SRH}} + \frac{S_{front/back}}{W}$$

Eq (1)

Experimental Procedure:

To start, 2-inch as-cut silicon wafers were cleaned using a piranha solution (sulfuric acid + hydrogen peroxide) followed by a saw-damage removal etch—both acid and alkaline chemistries were tried. The acid-based solution was a mixture of hydrofluoric acid, nitric acid, and acetic acid, and the alkaline-based solution was potassium hydroxide. Afterwards, RCA-b was used to remove any inorganic or metal contaminants on the surface. Finally, a hydrofluoric acid solution (BOE), was used to conclude the process. A BOE dip was repeated before any deposition was done in order to remove any surface oxides that may have formed.

After cleaning, atomic layer deposition (ALD) was performed using trimethyl aluminum as a precursor. This technique allowed for the controlled and conformal deposition of single monolayers on the surface of the silicon wafer. After depositing approximately 30 nm of aluminum oxide on both sides, the samples were annealed in a box furnace with a nitrogen atmosphere for 30 minutes at 425°C [1]. Minority carrier lifetime was measured by photoconductance decay using a WCT-120TS lifetime tester over a temperature range of 50°C to 230°C and an injection level 1×10^{14} to 1×10^{17} cm^{-3}.

Results and Conclusions:

Lifetime measurements were performed for both p-type and n-type Si wafers. Figures 1 and 2 show the variation of lifetime (y-axis) with injection level (x-axis) and temperature. In both graphs, the lifetime is seen to increase parabolically as minority carrier concentration increases, with maximums around 10^{15} cm^{-3}. Lifetime is also seen to increase with temperature despite the wafer type involved. These results are consistent with previous observations from other authors [2-4]. The trend with increasing temperature is expected since the additional energy imparted to the samples in the form of heat helps to fill empty levels in the band gap, therefore reducing the amount of possible recombination.

The n-type wafer was analyzed in further detail, with lifetime values reaching as high as 500 μs. The relationship between the inverse of effective lifetime and the inverse of wafer thickness taken for various wafer thicknesses at 200°C is shown in Figure 3. As depicted by Eq (1), this plot puts in evidence the

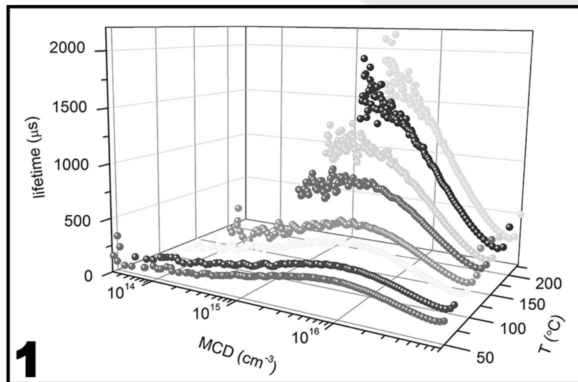

Figure 1: Lifetime versus temperature and injection level for a p-type c-Si wafer with an ALD Al_2O_3 layer. (See full color version on page xxxvi.)

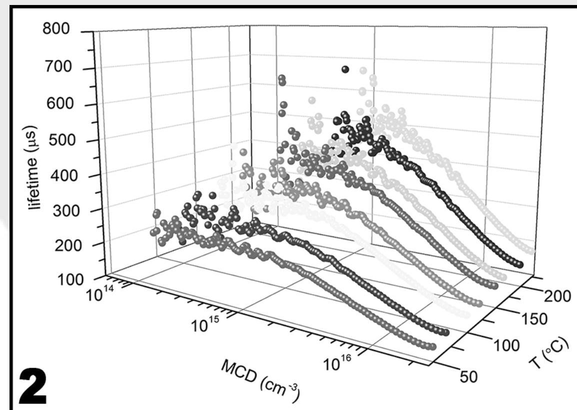

Figure 2: Lifetime versus temperature and injection level for an n-type c-Si wafer with an ALD Al_2O_3 layer. (See full color version on page xxxvi.)

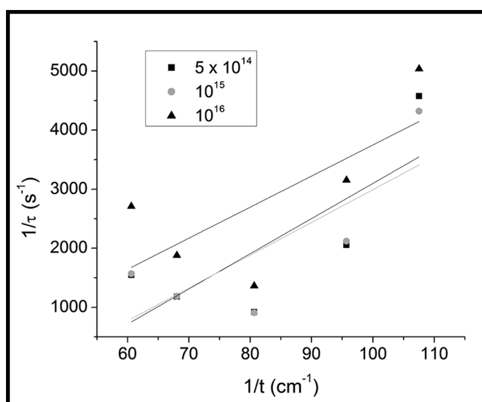

Figure 3: Inverse of lifetime versus inverse of wafer thickness measured at 200°C for n-type c-Si deposited with Al_2O_3 as wafer thickness was reduced. The slope represents the SRV.

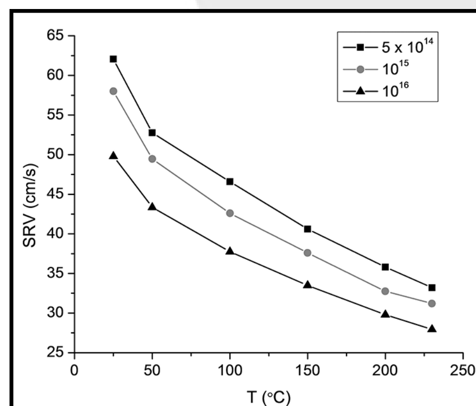

Figure 4: SRV versus temperature for n-type c-Si deposited with Al_2O_3.

SRV achieved with this passivation layer. The temperature was then plotted against the various SRV, found for 10° intervals over the measured temperature range, shown in Figure 4. From this graph, the dependence of SRV with temperature is clear and will be the base for future modeling efforts.

Future Work:

Initially, the type of passivation (chemical or field effect) must be studied. These results will then be used to develop a model for the relationship between SRV and temperature for various passivation layers (Al_2O_3, SiN_x, SiO_2). This will enable the subtraction of the surface effects from the effective lifetime, which ultimately will help characterize the high quality bulk silicon underneath.

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