Device Integration of Lithium Niobate Microring Resonators Patterned with a Silicon Hard Mask

Nicolás Andrade
Electrical Engineering, Virginia Commonwealth University

NNIN REU Site: Center for Nanoscale Systems, Harvard University, Cambridge, MA
NNIN REU Principal Investigator: Dr. Marko Lončar, School of Engineering and Applied Sciences, Harvard University
NNIN REU Mentor: Cheng Wang, School of Engineering and Applied Sciences, Harvard University
Contact: andradenm@vcu.edu, loncar@seas.harvard.edu, chengwang@seas.harvard.edu

Introduction:

Nonlinear optical devices are powerful tools for controlling the propagation, phase, and polarization of light. Lithium niobate (LN) is a promising candidate for integrated optical devices due to its combination of strong electro-optical and nonlinear optical properties. Ring resonators made of LN with reduced device size allow for nonlinear applications such as optical storage, second harmonic generation, telecommunication, and sensors. In order for these devices to function, the ring resonator needs to have a sufficiently high quality factor (Q-factor) so as to achieve high gain at its resonant frequency. There have been numerous attempts to fabricate high Q-factor LN optical resonators by utilizing advanced manufacturing techniques including photolithography, ion-beam enhanced etching, and reactive ion etching using either chromium or nickel masks deposited on the device [1].

There are numerous advantages to the techniques listed above; nevertheless, these usually result in rough sidewall profiles, high surface roughness, reduced etch depth, and non-ideal sidewall angles. These process non-uniformities, especially surface roughness, scatter light leading to poor confinement in the waveguides and resonators.

This project highlights work done to address two significant issues, the first part seeks to improve fabrication process non-uniformities and roughness by using a silicon hard mask, and the second part of the project deals with device integration with SU-8 waveguides. The device coupling efficiency, which is essential in nonlinear optics experiments, may be enhanced by improving the coupling between the waveguide and fiber by overlaying and polishing SU-8 waveguides. These methods make the fabrication and optical test of LN devices more robust and increase the device performance by improving modal confinement and tunability.

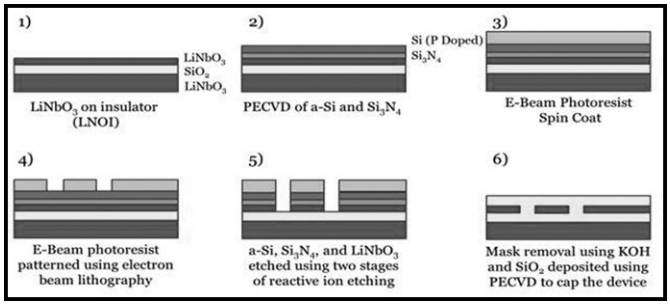

Figure 1: The fabrication process using a Si mask.

Methods:

The current process uses a FOX-16, hyrdrogen silsequioxane (HSQ) electron-beam resist, as an etch mask. However, HSQ is not crystalline and is physically soft; therefore, selectivity to LN is low, approximately 0.5, which leads to non-uniform lateral etching. To address the poor selectivity of the FOX-16 process, we tested a silicon mask, as shown in Figure 1, patterned by HSQ e-beam resist and a standard silicon (Si) dry etch process. The key points of this process were the testing of different thicknesses of amorphous silicon and e-beam resist, and the patterning of LN by a physical argon (25 sccm Ar^+) etch in a NEXX reactive ion etch (RIE) tool with an RF power of 250W and a pressure of 5 mTorr.

For the device integration portion, prior to a silicon dioxide (SiO_2) cap, SU-8 waveguides were overlaid on the sample and attached to existing waveguides to act as coupling pads for a lensed fiber. The key process was the cleaved sample polish using an Allied Polisher with 30 μm, 6 μm, 1 μm, 0.3 μm, and 0.05 μm lapping films; the first three pads were diamond and the remaining aluminum oxide.

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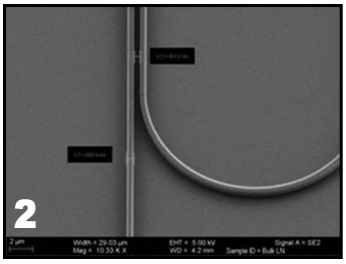

Figure 2: FESEM image of an Si mask demonstrating low surface roughness.

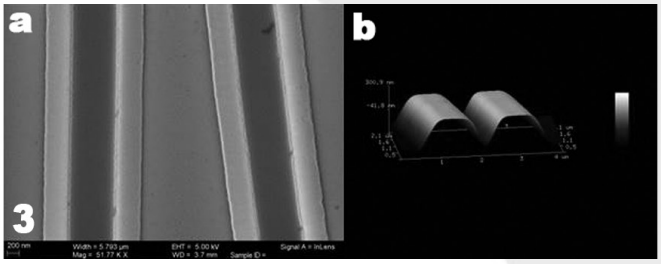

Figure 3: a) SEM image after silicon mask removal of a waveguide and ring resonator with noticeably low surface roughness and sidewall profile. b) AFM 3D image of the waveguide.

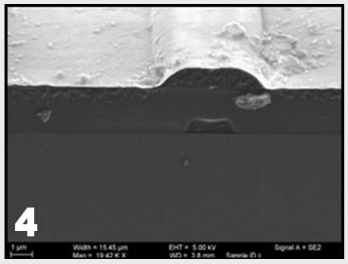

Figure 4: SU-8 waveguide after polishing.

Results:

The silicon mask, shown in Figure 2, has an acceptable sidewall profile and low surface roughness making it a promising hard mask. FOX-16 e-beam resist yielded the most favorable process for the two mask thickness based on field-emission scanning electron microscope (FESEM) images. The thicker resist layer protected the mask from being damaged by the RIE process.

The LN etch resulted in a smooth sidewall, which is important for the confinement of light in the waveguide, see Figure 3. The surface roughness of the structure (Figure 3) was a root mean square (rms) of 0.549 nm surface and 3.52 nm profile as measured with a Vecco NanoMan atomic force microscope. These values represent a relatively low surface roughness compared to results obtained using other fabrication methods. Based on these results, it may be concluded that the silicon mask thickness played an important role on surface roughness. The 800 nm silicon mask yielded a smoother sidewall profile and surface than the 600 nm mask due to better resistance to RIE damage.

Following the fabrication and optimization process, device integration using the SU-8 waveguides appeared to be greatly improved. The waveguides clearly extended to the edge of the sample, and are available to couple in light. The polished ends, as shown in Figure 4, will also be sufficient to not scatter the coupled laser light.

Conclusions:

Fabrication of LN devices with smooth sidewalls and a high aspect ratio has been demonstrated by using a silicon hard mask and RIE. This method has been used to show the potential to fabricate both ring resonators as well as a photonic crystal cavity structures using a silicon mask accompanied by RIE. The next step for the silicon mask process will be to optimize the mask thickness and the LN RIE process to create a steeper sidewall by tuning the RF power [1]. After the LN etch has been optimized, the quality factor, coupling coefficient between the resonator and the waveguide, and the laser coupling coefficient for the SU-8 will be tested. The design process can then be modified to deposit electrodes in order to electrically tune the resonator so as to create a fully functional and tunable modulator for potential use in telecommunications.

Acknowledgments:

I would like to thank my mentor Cheng Wang and Professor Marko Lončar, as well as the staff at the Center for Nanoscale Systems (CNS) for all their assistance. I would also like to acknowledge the NSF and the NNIN REU Program for funding and coordinating this research.

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PROC

A Piezoelectric Material P(VDF-TrFE) Thin-Film Process Flow for Ultrasonic Transducers

Mariella Arias
Biomedical Engineering, El Camino College

NNIN REU Site: Cornell NanoScale Science & Technology Facility, Cornell University, Ithaca, NY
NNIN REU Principal Investigator: Amit Lal, Electrical and Computer Engineering, Cornell University
NNIN REU Mentors: Jason Hoople and Po-Chen Cheng, Electrical and Computer Engineering, Cornell University
Contact: ariasmariella.brm@gmail.com, amit.lal@cornell.edu, jth5610@gmail.com, pc445@cornell.edu

Abstract:

Thin-film high-frequency ultrasonic transducers are a good candidate for generating high frequency ultrasound into various materials. The time-of-arrival, dispersion, amplitude, and phase of transmitted and reflected wave pulses can be used to characterize materials such as biological tissue. Piezoelectric polymer transducers are attractive in interrogating biological materials because of good acoustic impedance matching, leading to low voltage drive and higher bandwidth. For these reasons, we developed a microfabrication process for P(VDF-TrFE)-based ultrasonic transducers. The low acoustic impedance of the semi-crystalline copolymer (4.32 MRayls), allows for a better acoustic impedance matching to tissue/water (1.5 MRayls), resulting in increased coupling efficiency. All materials used in this process are CMOS-compatible, which allows for fabrication of transducers directly with CMOS, greatly improving system complexity and integration. Layers in this process were defined using standard contact lithography. The ultrasonic transducers fabricated by this process showed ultrasonic pulse transmission within the frequency range of 400-600 MHz. Signals with amplitudes of 2 Vpp resulted in receive signal amplitudes of 50 mVpp.

Introduction:

There are a plethora of biological applications that would benefit from large scale ultrasonic transducer phased array systems, such as ultrasonic imaging, neural stimulation, and cell trapping. It is of interest to develop a process which will allow the integration of ultrasonic transducers directly with the drive circuits fabricated in a complementary metal-oxide semiconductor (CMOS) process. This could greatly reduce the size and power of the phased array system. Such a system could be utilized to address sensory feedback issues in prosthesis.

Piezoelectric materials, such as bulk lead zirconate titanate and aluminum nitride, are frequently used due to their high coupling coefficient and commercial availability. However, a copolymer of poly[(vinylidenefluoride-co-trifluoroethylene], or P(VDF-TrFE), presents excellent physical characteristics that make it a great candidate for a range of biological applications. The low acoustic impedance (Z_o) (4.32 MRayls) of P(VDF-TrFE) makes this material a good acoustic match with water/tissue, resulting in more effective ultrasonic energy propagation. The copolymer also presents relatively small dielectric constant (4.0), easing transducer drive circuit design.

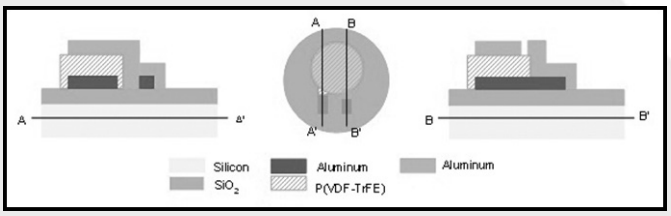

Figure 1: Schematic of fabrication process.

Device Fabrication:

All materials used in this process are CMOS-compatible, which allows for fabrication of transducers directly with CMOS, greatly improving system complexity and integration. Figure 1 illustrates left and right cross-sections of a transducer. Layers in this process were defined using standard contact lithography. The process began with an insulating layer of 500 nm PECVD of silicon dioxide (SiO_2) on a 500 μm thick 4-inch wafer. Aluminum bottom and top electrodes, of 210 nm and 250 nm respectively, were evaporated onto the substrate, and defined by wet etching. P(VDF-TrFE), dissolved in 2-butanone (7.00%w/v), was deposited by spin-coating to create a 1 μm thin layer, which was patterned using SPR 220-3.0 photoresist and etched by dry oxygen plasma etch.

After fabrication, an *in situ* electrical poling method was performed to induce piezoelectricity on the P(VDF-TrFE) film. An electrical field of 60 V/μm was applied on the transducer under 130ºC for one hour. The applied voltage was chosen in accordance with the work done by Li, et al. [1] on their fabrication of a piezoelectric tactile sensor using P(VDF-TrFE).

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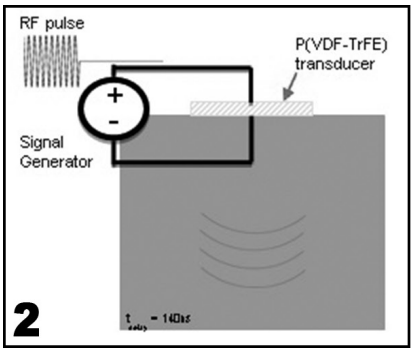

Figure 2: Experimental setup-wave propagation in silicon.

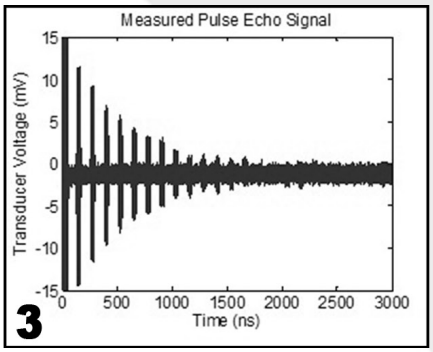

Figure 3: Pulse-echo signals.

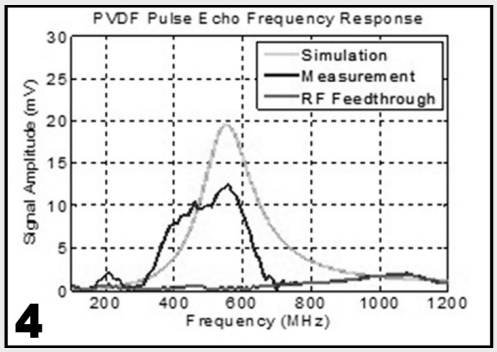

Figure 4: First echo as a function of RF.

Experimental Procedure:

A 40-nanosecond radio frequency (RF) pulse of fixed frequency was applied to the transducer through an RF switch. After approximately 130 ns, a signal was read on an oscilloscope. This signal corresponded to the time of flight of the ultrasound pulse in silicon traveling to the bottom surface, reflecting, and travelling back to the top surface (Figure 2). At the top, the ultrasonic pulse reflected again and made the journey back into the silicon. These repeated reflections were reflected in the captured signals with the same time delay corresponding to the time of flight in silicon (Figure 3).

It was of interest to investigate which signal frequencies allowed for efficient generation of ultrasound. By changing the frequency of the RF signal source, and looking at the amplitude of the first echo, the transducer's frequency response was characterized and plotted on Figure 4. Since the RF switches are not perfect isolators, there existed a small RF feed-through signal at the frequency of interest. The frequency response agreed with the simulation. Discrepancies between the two can be investigated further by considering the acoustic properties of the silicon dioxide layer, as well as considering the radiation pattern losses as opposed to the one dimensional model used for these experiments. The maximum amplitude level detected throughout the samples was 50 mVpp, though the sample here demonstrated a peak value of 24 mVpp. These differences could be accounted for due to RF losses in the printed circuit board traces, cable connections and different wire-bond lengths.

Conclusion and Future Work:

We have successfully characterized a P(VDF-TrFE) process for ultrasonic transducers, and used it to generate ultrasonic waves within the band of 400-600 MHz, using CMOS-compatible materials and processes. Future work will attempt to integrate this process flow with multimodal surgical silicon tweezers for tissue characterization, as well as CMOS for phased array circuit integration. Greater control of the ultrasonic beam is expected to result from the integration of P(VDF-TrFE) transducer arrays directly with CMOS. Alternate poling methods, such as magnetic field poling, will be addressed in the future to allow poling of multiple transducers at a time.

Acknowledgments:

This work was performed using the SonicMEMS laboratory, and the Cornell NanoScale Science and Technology Facility (CNF). I would like to thank Professor Amit Lal, and my mentors Jason Hoople and Po-Cheng Chen for their help and support, as well as the CNF staff. I also want to thank the National Science Foundation and the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program for the financial support and coordination of the program.

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PROC

Fabrication of Diamond Microwires for Quantum Information Processing Applications

Wu Joon Cha
Mechanical Engineering, Columbia University

NNIN REU Site: Howard Nanoscale Science & Engineering Facility, Howard University, Washington, DC
NNIN REU Principal Investigator: Dr. Gary L. Harris, Electrical Engineering, Howard University
NNIN REU Mentor: Michelle Chavis, Material Science and Engineering, Howard University
Contact: wc2444@columbia.edu, gharris1124@gmail.com, mac238@cornell.edu

Abstract:

The nitrogen-vacancy (NV) center in diamond has recently emerged as one of the potential candidates for quantum information processing applications due to its good coherence properties. However, interaction with the environment leads to decoherence — loss of quantum state. It has been reported that nanowire structures reduce interaction with the environment and increase coherence time. The purpose of this project was twofold: (1) grow and characterize diamond on silicon wafers, and (2) fabricate diamond microwires and nanowires using photolithography and electron-beam lithography. A hot filament chemical vapor deposition (HFCVD) system was used to grow nanocrystalline diamond on silicon wafers. Lift-off resists (LOR) 10B from MicroChem Corp. and Microposit S1818 from Shipley were used for a bilayer photoresist process followed by chrome (Cr) evaporation and liftoff process. An etch-back process was also studied to generate Cr patterns. Reactive-ion etching was used to etch diamond with an oxygen plasma with an etch rate of ~ 15 nm/min. We achieved ~ 3 μm sized diamond cylinders, which were characterized using scanning electron microscopy (SEM) and atomic force microscopy (AFM).

Introduction:

Quantum information processing (QIP) is promised to solve certain computational problems by drastically improving acquisition, transmission, and processing of information. Although quantum computers have their advantages, they have limitations: they must be isolated from their environment at low temperatures and the slightest interaction leads to decoherence — loss of quantum state [1].

The nitrogen-vacancy (NV) center in diamond has been proposed as potential candidate for qubit, a basic information unit for quantum computers, for its good coherence properties. The NV-center is formed by two-point defect in the diamond crystal lattice by replacing two carbon atoms with a nitrogen atom and a neighboring vacancy. Because of the particular orientation of electrons, their total spin can be manipulated and easily measured at room temperature [2]. However, when an NV-center interacts with the environment, it loses its coherence easily. Hence, it is important to enhance the coherence duration of the NV-center by reducing its interaction with the environment.

It has been reported that the interaction with the environment is reduced dramatically in diamond nanowires compared to bulk structure [3]. This was shown by comparing their collection efficiency of emitted photon. Having more efficient collection of emitted photon, nanowire structures reduce the interaction with the environment and increase the coherence time. Therefore, it is important to develop fabrication processes for diamond nanowires. In this work a method of diamond growth was studied and approaches to create micron-sized and nano-sized diamond wires were explored by using photolithography, electron-beam lithography process, and reactive-ion etching.

Methods:

We grew poly-crystalline diamond on silicon substrate via a HFCVD process, which flows current through filaments to increase their temperature in low pressure. The HFCVD system is from Blue Wave Semiconductors. At temperatures above ~ 1800°C, the hydrogen dissociates and interacts with hydrocarbon gas and forms free radicals which are essential for diamond growth. All silicon substrates were cleaned with trichloroethylene, acetone, and methanol, and sonicated in a 1:1 (nanodiamond seed:methanol) solution. We grew at 2300°C. with a ratio of hydrogen to methane of 60:1 or 80:1. The growth rate was approximately 0.25 μm per hour.

Photolithography was employed in this work. The fabrication processes are shown in Figure 1. A bilayer photoresist process was used for photolithography. Lift-off resists (LOR) 10B from MicroChem Corp and Microposit S1818 from Shipley were used to define etch patterns using a Karl Suss mask aligner. Next, a 150 nm Cr evaporation was performed followed by lift-off with acetone and Microposit Remover 1165 from Shipley that was heated at 90°C for 5 min.

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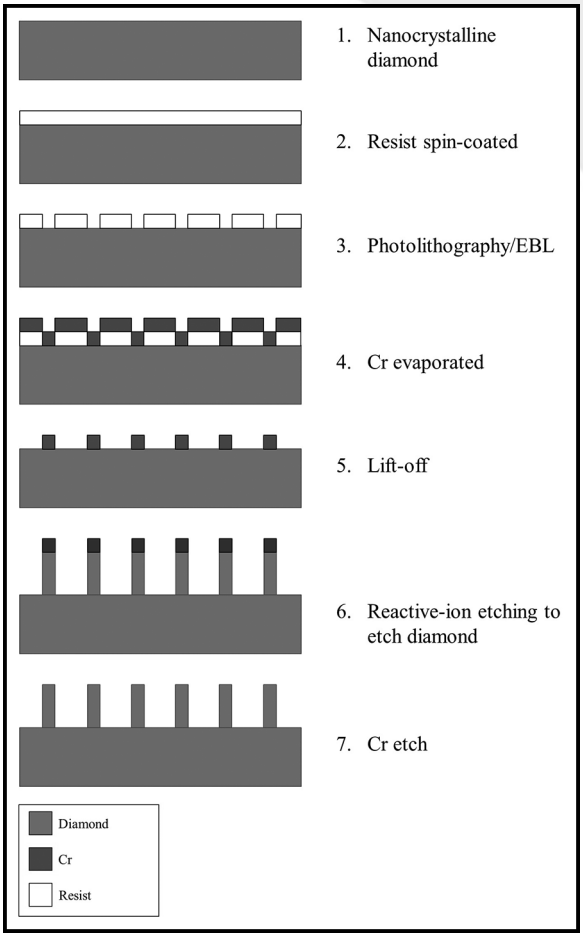

Figure 1: Fabrication process schematic.

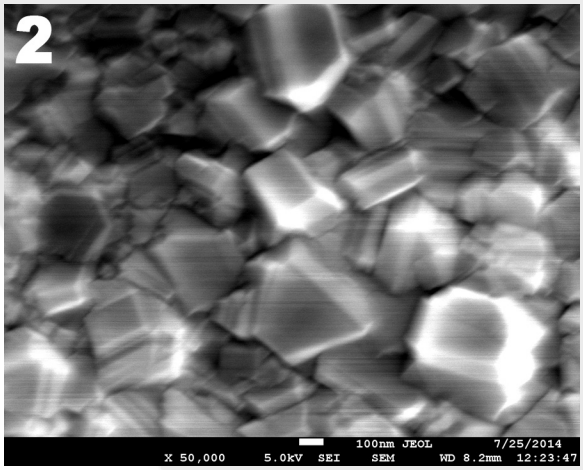

Figure 2, top: SEM image of grown nanocrystalline diamond.

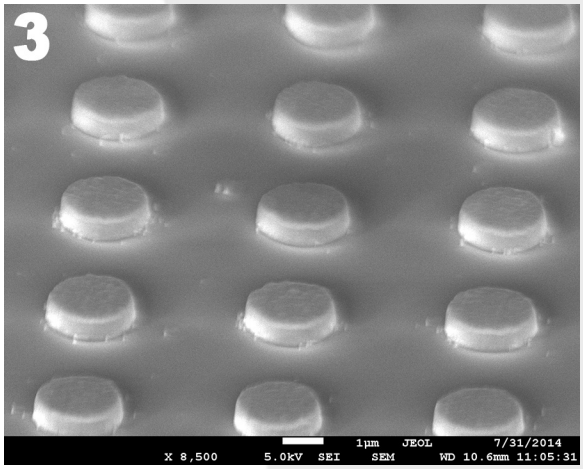

Figure 3, bottom: SEM image of fabricated ~ 3 µm sized diamond pillars.

Oxygen plasma cleaning was done to de-scum resist residue for effective lithography. Since oxygen plasma etches diamond, we also employed an etch-back process. In the etch-back process, the same lithography condition was used except Cr was deposited before resists.

A reactive-ion etching (RIE) system (Plasma-Therm 790) was used to etch the diamond and Cr. The etch recipe used for diamond etching consisted of an oxygen flow rate of 19.57 sccm, power of 100W and a chamber pressure of 10 mTorr. The etch recipe used for Cr etching consisted of an oxygen flow rate of 15 sccm and a flow rate of 35 sccm for chlorine, power of 50W, and a chamber pressure of 50 mTorr.

Results and Conclusions:

Nanocrystalline diamond was successfully grown as seen in the SEM image in Figure 2, which was characterized by SEM, AFM, and Raman spectroscopy. Micron-sized diamond pillars were successfully fabricated and were characterized by SEM and AFM. An SEM image of fabricated wires is shown in Figure 3. Reactive-ion etching was effective in etching diamond and Cr.

Future work includes fabricating nanowires with gold nanoparticles and electron-beam lithography using similar process. We hope to eventually dope nanocrystalline diamond with nitrogen to create NV-center embedded diamond pillars.

Acknowledgments:

I would like to thank my Principal Investigator, Dr. Gary Harris, my mentor, Michelle Chavis, site coordinator, Mr. James Griffin, collaborator, Ms. Anna-Kaye Barrett, and the staff of the Howard Nanoscale Science and Engineering Facility, the NNIN REU Program, and the NSF.

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PROC

Characterization of Ionic Liquid Gels used with Conformable Conducting Polymer and Textile Electrodes used for Electroencephalography

Dakota Crisp
Biomedical Engineering, University of Michigan

NNIN iREU Site: Centre Microélectronique de Provence, Ecole Nationale Supérieure des Mines de Saint Etienne, France
NNIN iREU Principal Investigator: George Malliaras, Department of Bioelectronics (BEL), Centre Microélectronique de Provence, Ecole Nationale Supérieure des Mines de Saint-Étienne, France
NNIN iREU Mentors: Thomas Lonjaret and Dr. Esma Ismailova, Department of Bioelectronics (BEL), Centre Microélectronique de Provence, Ecole Nationale Supérieure des Mines de Saint-Étienne, France
Contact: dncrisp@umich.edu, malliaras@emse.fr, thomas.lonjaret@emse.fr, ismailova@emse.fr

Abstract and Introduction:

Current electrodes for electroencephalography (EEG) and electrocardiography (ECG) recordings require the use of a liquid electrolyte to decrease the impedance at the electrode/skin interface. However, the liquid electrolyte can begin to dry within a few hours, limiting the time for usable data to be gathered. Recent efforts have been taken to combat this and other factors, leading to the creation of ionic liquid (IL) gels. IL is a substance that is conductive and liquid at room temperature, but can polymerize, creating a gel, upon UV curing. It has been shown that these IL gels have been mostly on par with its liquid electrolyte counterpart in terms of conductivity, and have also proven to maintain low impedance for much longer durations [1]. Additionally, a new gold (Au) electrode as well as the return of textile electrodes, are on their way to surpassing the performance of the standard medical electrode.

A more adhesive IL gel was produced to further improve the interface coupling. In this report, characterization of these new IL gels was performed, showing that improved adhesion does not compensate for conductivity lost due to deviation from the standard IL recipe. Information concerning trends in impedance with reference to IL gel volume, IL deposition, PEDOT:PSS deposition, and textile versus Au electrodes is also reported.

Device Fabrication:

A flexible Kapton® film sheet of 125 μm was used for the Au electrode substrate. CAD software was used to design the electrode schematics that were patterned on the Kapton sheet using a LPKF electronic laser cutter. Chromium (Cr) followed by Au were evaporated onto the substrate in thicknesses of ~ 30 mm and ~ 100 nm, respectively. Poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate), or PEDOT:PSS, was deposited on the heads of the electrodes.

Our first deposition method used two drop casts. The first was baked at 90°C for 2-3 minutes. The second was baked at 110°C for one hour. Our second deposition method involved four spin coatings, progressively getting thicker. The spin coater's RPM was as followed for each layer: 1500, 1300, 1000, 650. Finally, a single drop cast was performed.

Our third deposition method used a post-treatment of ethylene glycol. Replicas of these deposition methods were performed using a mixture of PEDOT:PSS and IPA in a 3:1 ratio. General cleaning and O_2 surface activation occurred between each majors steps. Textile electrodes were patterned with polydimethylsiloxane (PDMS), saturated in PEDOT:PSS, and then baked at 110°C for one hour.

Ionic liquid gels, supplied by an outside company, came in two components, IL + monomer and photoinitiator. Components were mixed together using specified ratios provided by the company and drop-casted on the heads of previously fabricated Au electrodes. Separate molds were also used as a control to test conductivity versus adhesion. Ultraviolet (UV) curing was performed with curing times that were dependent upon the IL formula being used. Distance between the IL composite and the UV lamp remained a constant 3 cm. For textile electrodes, 20 μl of IL was deposited, followed by another 20 μl of IL composite before curing.

Experimental Procedure:

UV curing times were discovered by drop-casting small samples on a glass slide and using a UVGL-58 handheld UV Lamp, set to long wave-365 nm. Curing intervals of five seconds were performed while physically testing the degree of polymerization between each interval.

Total UV curing time was recorded when samples displayed desired polymerization characteristics. These polymerization characteristics were such that each sample was determined to be solid yet release IL upon physical stimulation. This insured that our samples were reasonably resilient and exhibited conductive capabilities. Samples that were too dry were very adhesive and had low conductivity.

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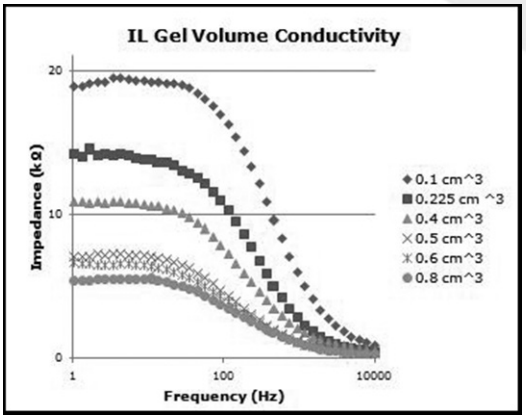

Figure 1: Impedance measurements of different IL gel volumes.

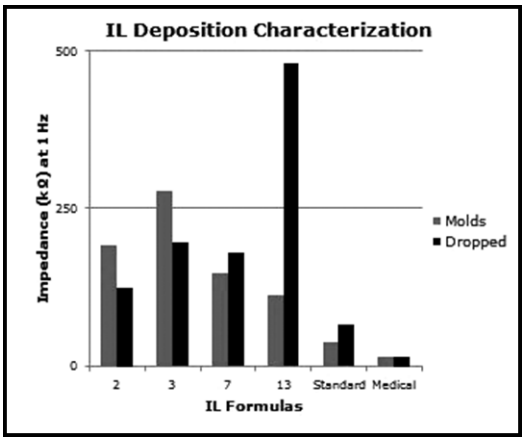

Figure 2: Impedance measurements of different IL formula differentiating drop casting versus external molds.

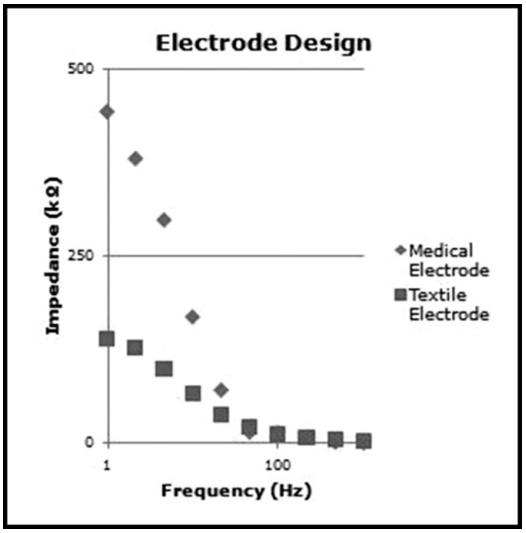

Figure 3: Impedance measurement of textile electrode versus standard medical electrode.

For impedance measurements, a cleaning solution of 75% H_20 and 25% ethanol was applied to the areas of the arm that would host the electrodes. The counter terminal was placed on the posterior side of the forearm, near the wrist. The working/source terminals were placed 3 cm superior to the counter electrode. The reference terminal was placed on the lateral side of the elbow, 20 cm superior of the working and source terminals. Standard medical electrodes were used as a control at the reference and counter terminals while the test electrodes were used at the working/source terminal. After each impedance test, the electrode in question was removed and the area on the skin was cleaned before the next test was performed.

Results and Conclusions:

It was shown that increasing IL gel volume decreased electrode impedance, instead of specifically thickness or surface area. However, this continuous decrease in electrode impedance was not linear and is assumed that a critical gel volume would then decrease conductivity. We also found that while some adhesive IL gels show a significant decrease in impedance when drop-casted directly on electrodes, as compared to an external IL gel mold, they exhibit overall less conductivity than the standard IL gel formula. Additionally, spin-coating four layers of PEDOT:PSS + ethylene glycol and then adding the extra drop-cast greatly improved the adhesion between the PEDOT:PSS and the Au, making it much more durable. However, conductive properties did not change. Finally, it was found that textile electrodes exhibited much less impedance than the Au or standard medical electrode.

Future Work:

Because there is still a potential for adhesive IL gels, more formulas will be synthesized and tested. Additionally, while the new PEDOT:PSS deposition method did exhibit more durable properties, the current process is very time consuming and wasteful of PEDOT:PSS. Thus, a more refined method, or possibly a better method, needs to be found.

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The Effect of Low Temperature Growth and Annealing on the $Al_2O_3/In_{0.53}Ga_{0.47}As$ Interface

Megan Hill
Materials Science and Engineering, Cornell University

NNIN REU Site: UCSB Nanofabrication Facility, University of California, Santa Barbara, CA
NNIN REU Principal Investigator: Susanne Stemmer, Materials Department, University of California Santa Barbara
NNIN REU Mentor: Varistha Chobpattana, Materials Department, University of California Santa Barbara
Contact: moh9@cornell.edu, stemmer@mrl.ucsb.edu, varistha@mrl.ucsb.edu

Abstract:

This work summarizes the characterization of the $Al_2O_3/In_{0.53}Ga_{0.47}As$ interface grown and annealed at low temperature. Samples were pretreated using atomic layer deposition (ALD) cycles of N*/TMA, then ~ 3-6 nm of Al_2O_3 were grown using ALD and furnace annealed to passivate the interface. Varying the annealing process found that a 250°C forming gas anneal, nearly independent of time, gave the best interface. Additionally nine cycles of N*/TMA was found as the optimum pretreatment giving a maximum midgap D_{it} of $6.85 \pm 0.37 \times 10^{12}$ $cm^{-2}eV^{-1}$. Though a better quality Al_2O_3 film and aluminum oxide/indium gallium arsenide (Al_2O_3/InGaAs) interface are achieved at higher temperature, these results show acceptable D_{it} and C-V behavior for use when low temperature processing is necessary.

Introduction:

$In_{0.53}Ga_{0.47}As$ is the leading candidate for post-Si n-channel technology partially due to its low effective electron mass. Additionally, high-κ dielectrics, like Al_2O_3, grown by atomic layer deposition (ALD) are being explored as gate oxides to prevent current leakage while maintaining high capacitances. However, high surface and interface defect concentrations lead to a high interface trap density (midgap D_{it}) at the Al_2O_3/InGaAs interface. Previous work has shown that *in situ* surface pretreatments using alternating cycles of nitrogen plasma and trimethylaluminum (N*/TMA) can successfully passivate the interface for a 300°C growth and 400°C furnace anneal [1]. However, material limits make it desirable to modify this passivation technique for low temperature processing, working with growth temperatures near 115°C and a maximum annealing temperature of 250°C.

Experiment:

InGaAs/InP samples were initially cleaned using a three minute buffered HF dip in order to remove any surface contaminants. An ALD reactor (Oxford Instrument FlexAl) was used for an *in situ* surface pretreatment and Al_2O_3 growth. The surface was pretreated using N*/TMA cycles, five to nine times, at 115°C. This pretreatment allows for the removal of native oxides and the initial passivation of the InGaAs surface. Immediately following the pretreatment, ~ 3-6 nm of Al_2O_3 was grown using cycles of TMA and water vapor. Al_2O_3/InGaAs samples were then post annealed in either a forming gas or N_2 environment for different times and temperatures below 250°C. Ni contacts (80 nm thick) were then deposited by thermal evaporation using a shadow mask. A Cr/Au contact (20/100 nm) was deposited on the back of the InP substrate in order to form the metal-oxide-semiconductor capacitors (MOSCAPs) used for electrical measurements. The MOSCAPs were tested using a two-point probe measurement to determine capacitance density and conductance as a function of gate voltage between 1 kHz and 1 MHz.

Results and Discussion:

Conductance and capacitance data was use to analyze the quality of the Al_2O_3/InGaAs interface. The optimum pretreatment and annealing conditions can be found by minimizing the frequency dispersion, but more importantly the midgap D_{it} response. The frequency dispersion is the difference in capacitance between 1 kHz and 1 MHz. This should be minimized both in the accumulation (high bias) and transition regions as seen in Figure 1. A high frequency dispersion can be a sign of a film with high trap densities, currently leakage, and channel resistance, which limit device speed and cause break down at high bias [2]. In addition to this, we want to minimize the midgap D_{it}, which is the quantitative estimate of the interface trap density in the InGaAs midgap. The "conductance" method described in Reference 3 uses the measured capacitance and conductance to calculate the D_{it} at 1 kHz.

Figure 2 shows the frequency dispersion as a function of annealing conditions. The lowest frequency dispersion of 2.5 $\times 10^{-8}$ F/cm^2 for the transition and 1×10^{-7} F/cm^2 for accumulation is found for a 15 minute, 200°C furnace anneal in a forming gas environment. However, the D_{it} response (Figure 3) is high for the 200°C case at about $1.1.10^{13}$ cm^{-2}/eV.

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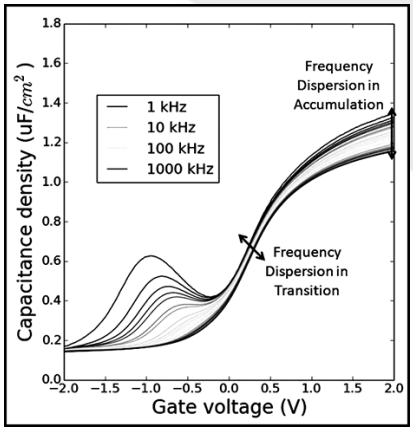

Figure 1: Example C-V curve for Al_2O_3/InGaAs MOSCAP. Frequency dispersion should be minimized in transition and accumulation regions. (See full color version on page xxxvi.)

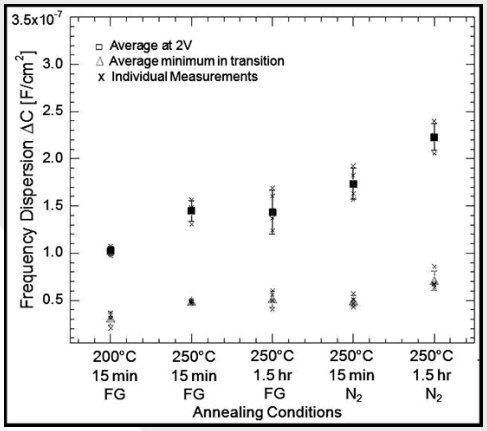

Figure 2: Frequency dispersion in accumulation and in transition versus annealing conditions. Samples were furnace annealed between 200°C and 250°C for 15 to 90 min in either a forming gas (5% H_2/95% O_2) or N_2 environment.

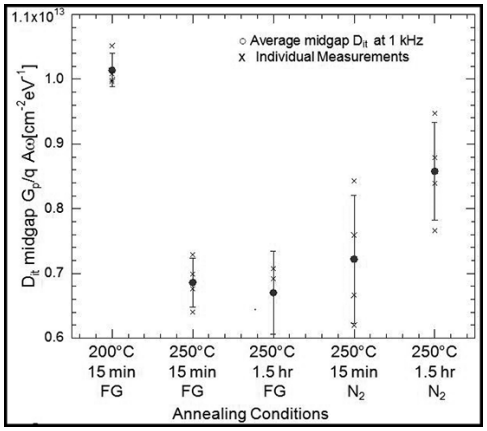

Figure 3: Midgap D_{it} response (estimate of interface trap density) versus annealing conditions.

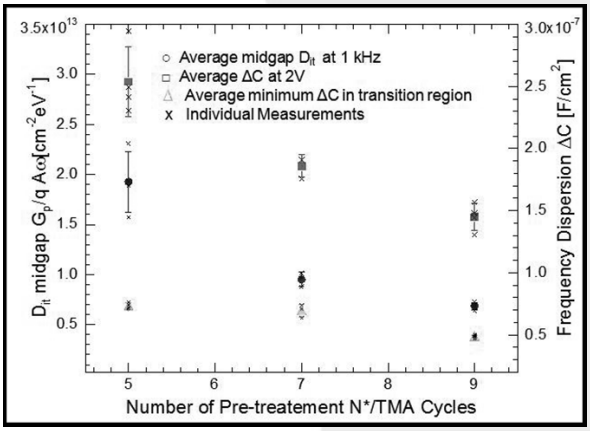

Figure 4: Midgap D_{it} response, frequency dispersion in accumulation, and frequency dispersion in transition versus number of N/TMA* in situ *pretreatment cycles.*

A 250°C forming gas anneal gives the lowest D_{it} response with little time dependence.

The frequency dispersion and midgap D_{it} response were also compared to find the optimum number of pretreatment cycles. Figure 4 shows that nine cycles N*/TMA is clearly the best condition for surface cleaning. It is possible that greater than nine cycles could give slightly better D_{it} results, but it is more likely that additional plasma exposure would damage the InGaAs surface.

Conclusions and Future Work:

It has been shown that it is possible to grow quality Al_2O_3 by ALD even at 115°C. C-V data show reasonable behavior with acceptable levels of current leakage. Additionally, a midgap D_{it} of 6.85 ± 0.37 × 10^{12} $cm^{-2}eV^{-1}$ has been achieved for a 250°C forming gas anneal with nine cycles of a N*/TMA *in situ* pretreatment. High temperature processing has reported midgap D_{it} values around 2 × 10^{12} $cm^{-2}eV^{-1}$ after optimization, but this result is still acceptable when low temperature processing is desired [1].

In the future, work may be done to further optimize this recipe by varying the plasma conditions during pretreatment. Additionally, further surface imaging has been started using AFM and SEM to better understand the film morphology and the affect of annealing time.

Acknowledgements:

I would like to thank my P.I. for her support on this project, and especially my mentor for her advice and guidance. Materials and project funding were provided by Northrop Grumman and the NSF. Student funding was provided by the SRC, NSF, and the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program.

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Surface Micromachining of Microfluidic Devices

Staci Hill
Chemistry, Middlebury College

NNIN REU Site: Lurie Nanofabrication Facility, University of Michigan, Ann Arbor, MI
NNIN REU Principal Investigator: Professor Jianping Fu, Mechanical Engineering, University of Michigan, Ann Arbor
NNIN REU Mentor: Weiqiang Chen, Mechanical Engineering, University of Michigan, Ann Arbor
Contact: stacih@middlebury.edu, jpfu@umich.edu, wqchen@umich.edu

Abstract:

Micro-through-holes were fabricated in thin-films of polydimethylsiloxane (PDMS). Standard photolithography was used to pattern photoresist coated on the PDMS substrate, while reactive ion etching (RIE) using both a capacitively coupled plasma (CCP) system and an inductively coupled plasma (ICP) system was used to transfer desired through-hole patterns from photoresist to underlying PDMS layers. By investigating the independent effects of RF power, total pressure, and gas composition (SF_6:O_2), an optimal etch recipe was identified for each RIE system. Optimal recipes were defined by the fastest PDMS etch rate with a respective etch selectivity over photoresist greater than one. Although the ICP system proved to be more time efficient, both systems were able to generate a desired 6 μm diameter through-hole pattern with relatively vertical sidewall profiles.

Introduction:

Reactive ion etching (RIE) of thin-films of PDMS has been used to fabricate micro-through-holes for microfluidic devices [1-3]. Previous research has investigated PDMS etch rate trends under varying plasma conditions using hard masks such as aluminum [2-4]. Recently, a new surface micromachining technique reported by Chen, et al. introduced a method to pattern PDMS directly using conventional photolithography [1]. This method serves as an inexpensive patterning technique; however, research regarding the selectivity of the etch is limited. Additionally, the disparities between etching PDMS on a capacitively coupled plasma (CCP) system and inductively coupled plasma (ICP) system have not been characterized.

In this report, we present optimal recipes for etching thin-films of PDMS on both a CCP and ICP system. The plasmas studied were composed of varying ratios of SF_6 and O_2. As proof of concept, optimal recipes were used to etch 6 μm diameter through-holes in a 10 μm thick PDMS layer. While both systems fabricated the desired feature, the PDMS etch rate was an entire order of magnitude greater on the ICP system. The etch was more selective using the CCP system; however, qualitative assessments found the ICP system generated less surface roughness and cracking of the PDMS in addition to more uniform features.

Experimental Procedures:

Etch rates of PDMS and photoresist were studied by varying total pressure, gas composition (SF_6:O_2), and RF power on both the CCP system (PlasmaTherm 790, Unaxis, Schwyz, Switzerland) and ICP system (LAM 9400, Lam Research, Fremont, CA). Thicknesses of thin-films of PDMS and photoresist were measured using a Dektak XT surface profilometer before and after each etch recipe, in which the difference divided by the total etch time was found to be the respective etch rate. Each recipe was done in triplicate.

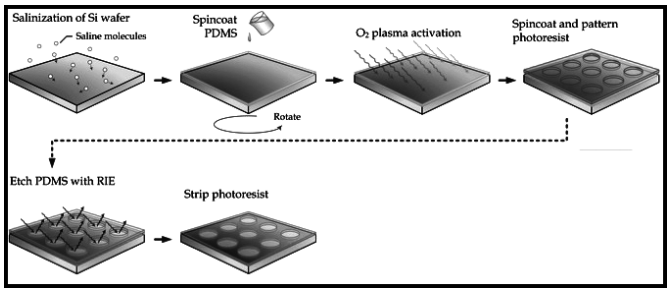

Figure 1: A schematic depicting the surface micromachining protocol used to fabricate micro-through-holes in thin-films of PDMS.

Optimal etch recipes were determined based on PDMS etch rate, etch selectivity, and quality of transferred pattern. Optimal etch recipes were used to fabricate 6 μm diameter holes in a 10 μm thick PDMS film (Sylgard 10:1 base:curing agent), which was achieved by spin-coating PDMS pre-polymer at 7,200 rpm for 35 sec. This fabrication method is illustrated in Figure 1 and adopted from [1].

Results and Discussion:

The determined optimal etch recipes as well as their respective rates and selectivities are reported in Table 1. Optimal etch recipes were determined by selecting the recipe with the fastest

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Plasma System	RF Power (Watts)	Total Pressure (mTorr)	Gas Composition	Etch Rate (nm/min)	Etch selectivity
CCP	100	30	100% SF_6	188	2.6
ICP	500	10	94% SF_6	1,180	1.8

Table 1: Optimal etch recipes for fabricating micro-through-holes using the surface micromachining method.

PDMS etch rate with a corresponding selectivity greater than 1.0 on both the CCP and ICP systems. A selectivity greater than 1.0 ensured that the 10 μm thick PDMS layer would be etched through prior to the patterned photoresist completely removed by RIE. Because the CCP system was not equipped with a cryogenic chuck, the photoresist would char as either RF power or total pressure increased. As a consequence, desired patterns would erode forming indistinguishable features. Therefore, the quality of the photoresist was also considered when defining an optimal recipe.

The etch rate of the optimal ICP recipe is an entire magnitude greater than the optimal CCP recipe. While the etch mechanism of PDMS is unknown [3] significant difference in etch rates can be attributed to the RF power and gas composition. A cryogenic chuck present on the ICP system allowed for a greater power supply while maintaining the quality of the photoresist. Additionally, the added oxygen was seen to increase the etch rate of PDMS, most likely by readily exposing the silicon in the PDMS to reactive fluorine species of the plasma [4]. Limitations on the CCP system prevented this idyllic ratio of SF_6 to O_2, and a plasma comprised of 100% SF_6 was seen to be optimal.

The features generated by the optimal etches can be seen in Figure 2 (a,b). Each system was able to fabricate features within 100 nm of expected diameter; however, the ICP system produced a clean, vertical sidewall. In contrast, the CCP system generated features with a rough perimeter.

Conclusions:

Both CCP and ICP systems can fabricate the desired micro-through holes. The ICP system proved more time efficient and generated less surface roughness. Due to the high cost of RIE, the possibility of a wet etch should be investigated.

Acknowledgements:

The National Science Foundation and the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program are acknowledged for funding this research. In addition, the support of Professor Jianping Fu and Weiqiang Chen is greatly appreciated.

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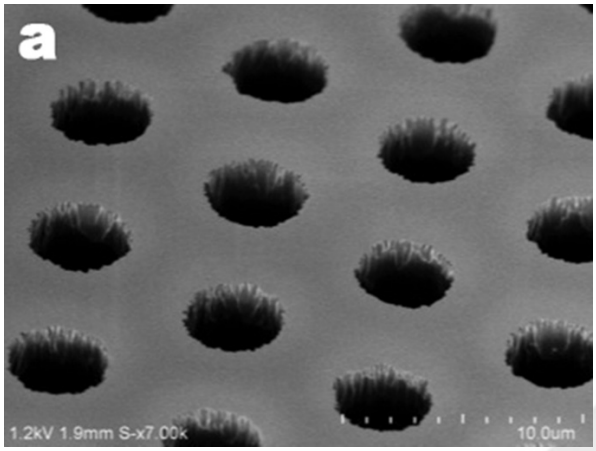

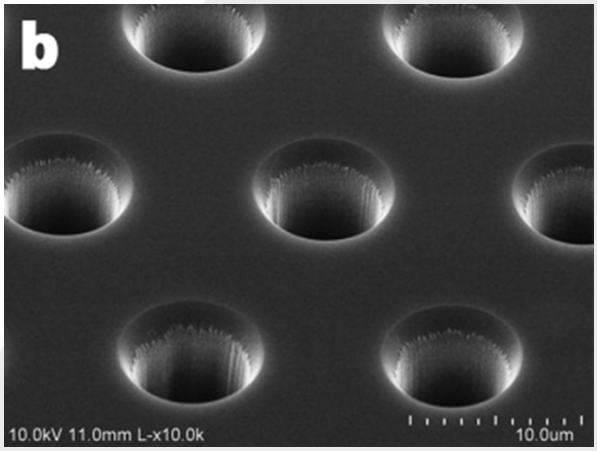

Figure 2: Fabricated 6 µm through-holes using the surface micromachining method etched by; a) CCP system, and b) ICP system.

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Fabrication and Characterization of Diamond Field-Effect Transistors

Tiffany Huang
Electrical and Computer Engineering, Baylor University

NNIN iREU Site: National Institute for Materials Science (NIMS), Tsukuba, Ibaraki, Japan
NNIN iREU Principal Investigator: Yasuo Koide[1], Division Director, Research Network and Facility Services Division, (NIMS), Tsukuba, Ibaraki, Japan
NNIN iREU Mentors: Masataka Imura[1], Liu Jiangwei[1], Hirotaka Oosato[2], Eiichiro Watanabe[2], and Daiju Tsuya[1,2]
NNIN iREU Affiliations: 1. Wide Band-gap Materials Group, Optical and Electronic Materials Unit, 2. Nano-Integration Facility, Nanotechnology Innovation Station; Tsukuba, Ibaraki, Japan
Contact: tiffanywhuang@yahoo.com, koide.yasuo@nims.go.jp

Abstract:

The next generation of communication technology requires materials that can handle higher frequency and higher power. Diamond's excellent physical properties, such as high band-gap, high breakdown field, and the highest thermal conductivity of all materials, make it ideal for communication applications. Improving diamond field-effect transistor (FET) performance will make diamond viable for such applications. We fabricated and characterized hydrogen-terminated diamond (H-diamond) FETs with an Al_2O_3 gate insulator using laser lithography, e-beam lithography, ozonolysis, e-gun sputtering, atomic layer deposition, microscopy, annealing, and FET device analysis. Challenges of this process included improving the process yield and the drain current. We found that the high stability of the H-diamond surface causing the metal electrodes to easily peel off the surface, causing a low process yield. Optimization of the fabrication process and annealing improved the process yield and the drain current, respectively.

Introduction:

As communication devices advance, they require materials that operate at higher frequency and higher power, and diamond's physical properties make it an ideal material for high frequency power applications. These properties include the highest breakdown field (10 MV cm^{-1}), a wide band-gap energy (5.47 eV), the highest thermal conductivity (22 W cm^{-1} K^{-1}), and the highest carrier mobility (2200 and 1800 cm_2 V^{-1} s^{-1} for electrons and holes, respectively) [1, 2]. Improving the performance of diamond FETs would allow the next generation of communication devices to use these properties.

Diamond FETs consist of a gate, source, drain, gate insulator, and hydrogen-terminated diamond (H-diamond) surface [3], as shown in Figure 1a. This H-terminated surface provides hole carriers, and these holes allow current to flow from the drain to the source. Varying the gate voltage and the drain voltage to measure the induced drain current results in an I_d-V_d graph, as depicted in Figure 1b, and these graphs are used to characterize FET performance. FET performance is considered superior when the maximum drain current is higher. In this work, we seek to improve existing fabrication procedures to increase the maximum drain currents.

Fabrication Procedures:

Figure 2 depicts the fabrication procedures performed on H-diamond samples. We first patterned the surface to define FET areas using laser lithography. Defining FET areas involved exposing the sample to ozone in UV light. Oxygen passivated the exposed H-terminated surface, and liftoff left a surface patterned with H-terminated FET areas (Figure 2a). Next, we used e-beam lithography to obtain high resolution patterns for the source-drain electrodes. We deposited palladium (Pd), titanium (Ti), and gold (Au) by e-gun deposition (Pd and Ti acted as adhesion layers), before performing liftoff (Figure 2b). The third step consisted of depositing the gate insulator aluminum oxide (Al_2O_3) by atomic layer deposition (ALD) and defining the gate electrodes. We used laser lithography to pattern the surface, and we evaporated onto the surface Ti (as an adhesion layer) and Au (Figure 2c). Liftoff revealed fully fabricated diamond FETs (Figure 2d).

The previous and improved procedures were alike, except for the third and fourth steps. In the previous procedure, we deposited the photoresist before the Al_2O_3 and gate metal, and liftoff. However, many of the source-drain electrodes peeled off the surface, as shown in Figure 3a, nullifying 10/36 FETs.

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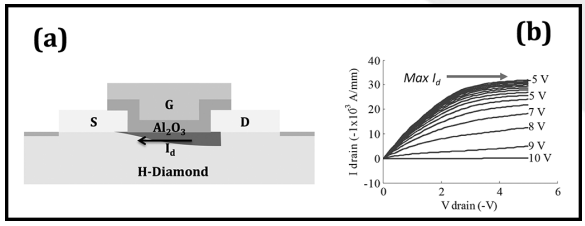

Figure 1: (a) Diamond FET. (b) I_dV_d characteristic of FETs.

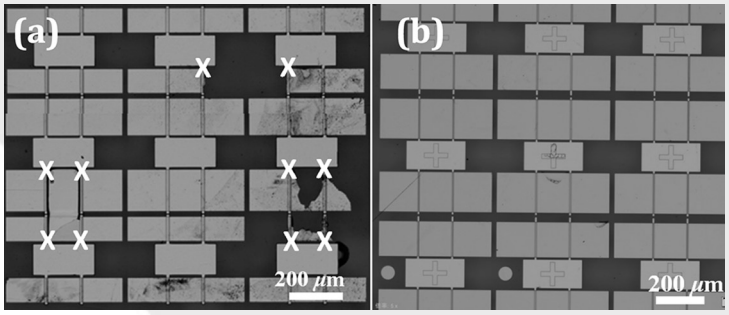

Figure 3: Sample following lift-off in (a) the previous, and (b) the improved processes.

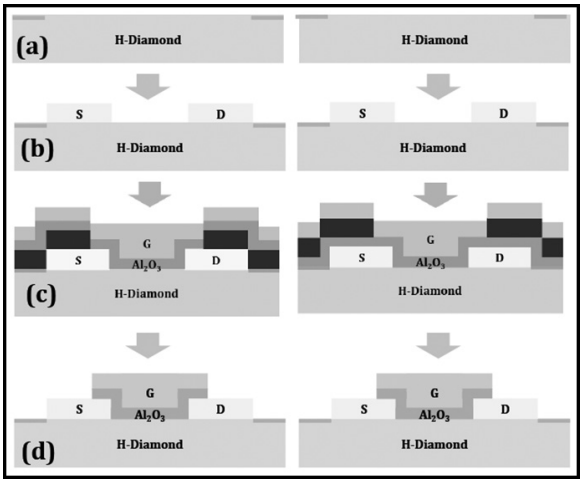

Figure 2: Previous (on left) and improved (on right) procedures for diamond FETs. (a) Defining FET areas.
(b) Defining the source-drain electrodes. (c) Depositing gate insulator and defining the gate electrodes. (d) Lift-off to form diamond FET.

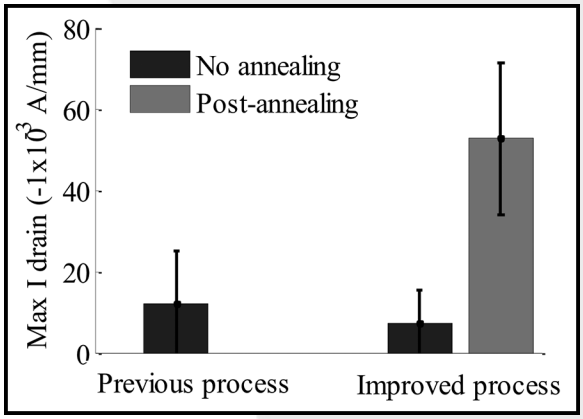

Figure 4: Maximum drain currents for the previous (n = 7) and improved (n = 8) fabrication processes.

In the improved procedure, we deposited the Al_2O_3 before the photoresist and gate metal, and liftoff. This eliminated the peel-off behavior, as shown in Figure 3b. We then annealed the improved sample at 200°C for one hour in vacuum to improve device performance.

Characterization and Results:

Varying the last steps of the procedure eliminated the peel-off behavior due to the stability of H-diamond. The source-drain electrodes were weakly attached to the H-terminated surface. The photoresist to source-drain attachment may be stronger than the source-drain to H-diamond attachment. Thus, lifting off the photoresist may also peel off source-drain electrodes. Passivating the surface with Al_2O_3 removed this effect due to the unique properties of ALD Al_2O_3. ALD Al_2O_3 is commonly used as a diamond gate insulator, because it both protects and strongly adheres to the H-terminated surface. Thus, passivating the entire surface with Al_2O_3 after defining the source-drain electrodes ensured the source-drain electrodes would not easily peel off.

Figure 4 shows the maximum drain current of the previous and improved process, and it shows the maximum drain current of the improved process post-annealing. Post-annealing significantly increased the average maximum drain currents of the procedures from 7.22 mA/mm to 52.6 mA/mm, and following annealing, one sample obtained a maximum drain current of 88.5 mA/mm. Annealing likely reduced the hole trap density in the Al_2O_3 and the interface between the Al_2O_3 and the H-diamond, although further work is needed to verify this hypothesis.

Conclusions and Future Work:

Improvements to the fabrication procedure of diamond FETs eliminated peel-off behavior, and post-annealing significantly increased the drain current of the FETs. Future research involves further investigation of the post-annealing phenomenon.

Acknowledgments:

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Graphene Growth by Chemical Vapor Deposition

Laura Huddleston
Electrical Engineering, Georgia Institute of Technology

NNIN REU Site: Howard Nanoscale Science & Engineering Facility, Howard University, Washington, DC
NNIN REU Principal Investigator: Dr. Gary Harris, Electrical and Computer Engineering, Howard University
NNIN REU Mentor: Mr. Crawford Taylor, Electrical and Computer Engineering, Howard University
Contact: llhudd@gatech.edu, gharris1124@gmail.com, crawford@msrce.howard.edu

Abstract:

Graphene is a single layer of carbon atoms that is extremely strong, electrically conductive, transparent, and flexible. These properties lead it to have a variety of applications depending on how it is produced. Chemical vapor deposition (CVD) is the preferred method of production to implement in touch screens, smart windows and solar cells. The focus of this project was to determine the ideal conditions in which to grow graphene via CVD. Based on success in previous graphene experiments, the two materials chosen to use in this project were copper (Cu) and nickel (Ni). The samples were heated to 1000°C and both methane and hydrogen gasses were pumped through the system. Raman spectroscopy was used to characterize the samples, and it showed single-layer graphene on both Ni and Cu. Through this, a range of conditions has been deduced where it is most probable that graphene will grow.

Introduction:

CVD uses high process temperature to produce the high quality graphene needed in solar cells, however, CVD has a high production cost and only moderate sustainability. The goal of this project was to create a controlled environment where graphene could be efficiently reproduced. In order to achieve this goal, growth conditions had to be narrowed down to a specific range of conditions and ratio of gases. Once this was achieved, future work could shift to exploring graphene growth on other substances such as silicon and silicon dioxide.

Experimental Procedure:

The two main materials used were Cu foil and Ni evaporated onto silicon dioxide (SiO_2) wafers. These materials were pretreated by allowing them to soak in trichloroethylene, acetone, and methanol for three minutes each. The Cu was further treated by allowing it to sit in a warm acetic acid bath for five minutes. Ni was evaporated onto the SiO_2 wafers at varying thicknesses ranging from 150 to 3000 Å. The evaporated Ni was later switched out for annealed Ni foil.

Once the materials were placed inside the CVD system, they were annealed with hydrogen at 1000°C for 60 minutes. The methane gas was added to the hydrogen for the next 40 minutes during the growth phase. The furnace was then allowed to slowly cool to room temperature while still flowing the methane and hydrogen gases. Finally, the system was purged with argon for 15 minutes, so that the materials could be removed from the system.

Results and Conclusions:

The substrates were characterized by Raman spectroscopy, and this confirmed successful graphene growth on both Cu and Ni. The results ranged from no growth to multi-layer graphene to graphite. This allowed the conditions to be narrowed down until a range was found where graphene would consistently grow. Graphene was determined to have optimal growth when hydrogen gas flow was 1-2% of the methane gas flow. A range for Ni was unable to be narrowed to a specific ratio.

The lack of consistent growth on Ni most likely was caused by the amount of Ni evaporated on the SiO_2 substrate. When there was a larger amount of evaporated Ni, it was found to form into beads during the growth process, which inhibited graphene formation. Future research would find the optimum thickness of evaporated Ni and would move on to attempt growth on other materials such as silicon.

Acknowledgements:

I would like to thank the following for their support: PI Dr. Gary Harris, Research Mentor Mr. Crawford Taylor, Site Coordinator Mr. James Griffin, the staff at the Howard Nanoscale Science and Engineering Facility, the National Nanotechnology Infrastructure Network Research Experience for Undergraduates (NNIN REU) Program, and the National Science Foundation.

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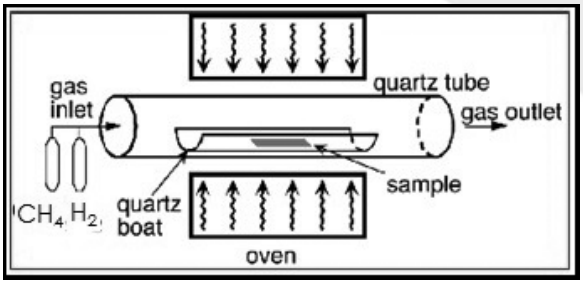

Figure 1: Diagram of simple CVD system.

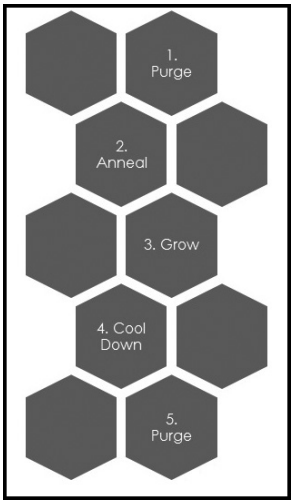

Figure 2: Diagram of CVD growth process.

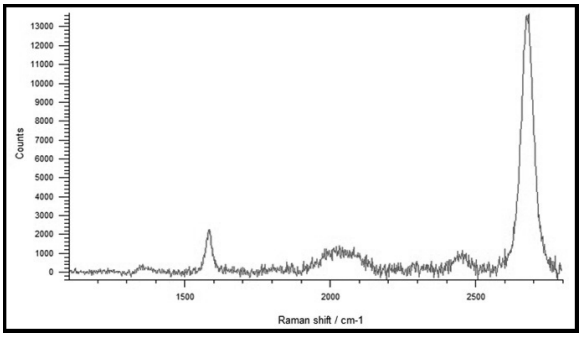

Figure 3: Raman spectroscopy results showing single-layer graphene growth on copper foil.

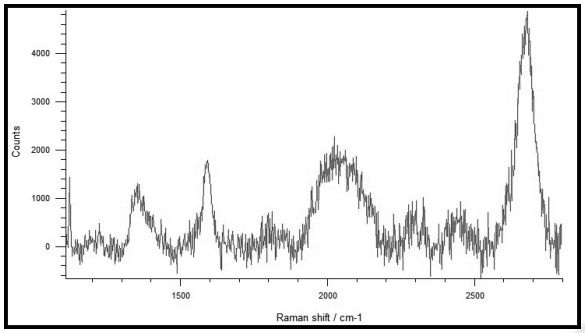

Figure 4: Raman spectroscopy results showing single-layer graphene growth on evaporated nickel.

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Microtensiometers with Patterned Porous Silicon

Adriana Mulero
Chemical Engineering, University of Puerto Rico-Mayaguez

NNIN REU Site: Cornell NanoScale Science & Technology Facility, Cornell University, Ithaca, NY
NNIN REU Principal Investigator: Abraham Stroock, Chemical and Biomolecular Engineering, Cornell University
NNIN REU Mentor: Michael Santiago, Mechanical and Aerospace Engineering, Cornell University
Contact: adriana.mulero1@upr.edu, abe.stroock@cornell.edu, ms2343@cornell.edu

Abstract:

The mission of this project was to decrease significantly the porous membrane in our MEMS-fabricated tensiometer [1] to be used as a probe with high spatial-resolution. Following the protocol of Ohmukai [2], we used photolithography with image reversal to pattern the membrane. We modified the membrane's etching recipe since the area coverage was less than original devices. We reported on the characterization of the patterned membranes by optical and electron microscopy and the formation of test devices based on anodic bonding with glass. We concluded with our measurements of permeability of the patterned membranes and perspectives for future experiments and applications.

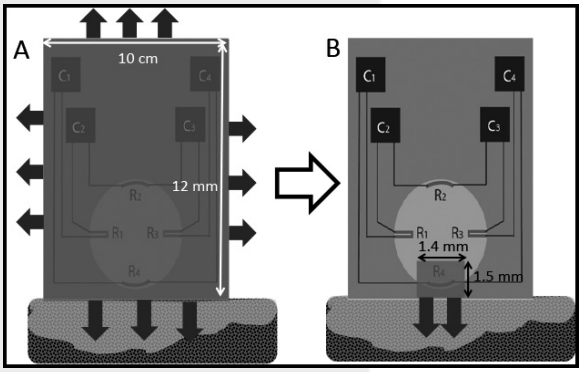

Figure 1: Mission. Two tensiometers measuring a soil sample with varying water potentials. Figure A represents a device with a full membrane receiving information from all its surroundings, while (B), with a smaller membrane, receives information from a specific area (higher resolution).

Introduction:

Our tensiometer quantifies the water potential in plants and soils directly as pressure. It measures the pressure in an internal water-filled cavity that equilibrates with the measured media through a porous silicon (PoSi) membrane, a layer of nanopores electrochemically etched on a silicon wafer. Previously the PoSi connected the cavity with the perimeter of the whole sensor, thus the sensor equilibrated with all its surroundings. Our goal (Figure 1) was to decrease the PoSi so the sensor will have a higher spatial resolution. We faced two main challenges. First, we had to use a technique to decrease the patterned area that did not compromise the bonding process or the ability to sustain large tensions. Second, there was a need to increase the permeability of the PoSi to compensate for the decrease in cross-sectional area relative to the original design.

In a broader view, by characterizing these devices we could improve water management in agriculture by providing *in situ* values of water availability in soils and plants.

Experimental Procedure:

Porous Membrane Patterning. We designed a mask using L-edit with the new porous membrane dimensions, 1.4 mm wide and 1.5 mm tall. The patterning process consisted of basic photolithography steps using S1827 photoresist. We did an image reversal and a hard bake. After the wafer was successfully patterned, we proceeded with creating the pores in the areas not covered by the photoresist.

PoSi Etching. Using the previously-used electrochemical etching setup [1], and a 1:1:2 HF:water:ethanol solution (mixed in a separate container) we were able to create the PoSi. We used the same current density as in the previous versions of the tensiometer's porous membrane of 20 mA/cm^2, so given the change in the total area coverage from the whole wafer to 1.3%, the current had to change from 900 mA to 12 mA. However, the time the wafer was exposed to the current remained at five minutes. In order to increase permeability, we created bigger holes in some devices by lowering the HF concentration to 21%. After the wafer was successfully etched, it was anodically bonded to glass, diced using the dicing saw, and studied under an optical and electronic microscope.

Permeability Testing. We compared previous devices (full membrane) with new patterned devices with membrane containing small and big pores. The purpose of the tests was to determine how effective these new devices were. Test devices had a 16 μm-deep cavity ranging from 1.4 to 2 mm in diameter, and either a full or patterned membrane. First, each device was filled with water at high pressure (~ 950 psi) using a pressure

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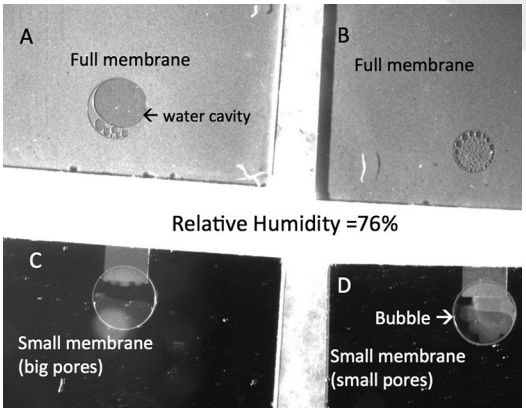

Figure 2: Permeability test. Devices (A) and (B) contain porous membrane covering them completely, while (C) and (D) have the new patterned porous membrane. All four of them (A, B, C and D) have bubbles in the water cavity, which means they have started to empty.

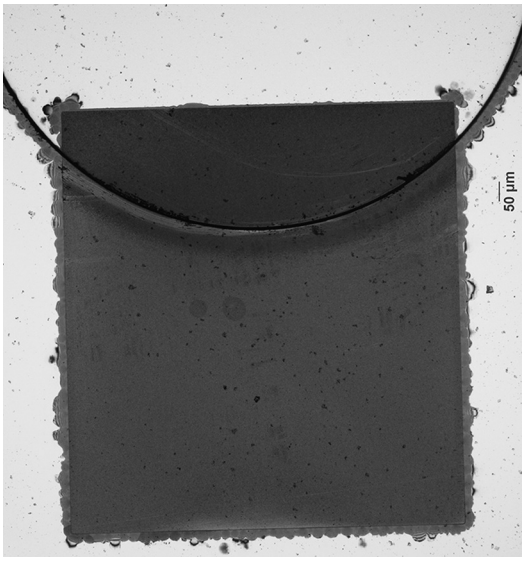

Figure 3: Top view of tensiometer with the new patterned membrane.

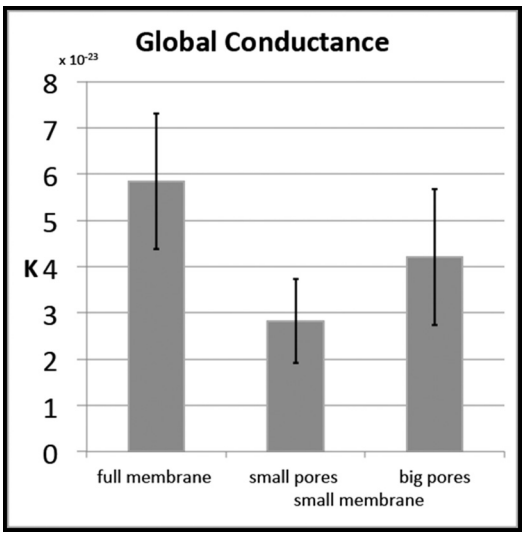

Figure 4: Global water conductance graph.

bomb [1]. Second, three to four water-filled tensiometers were placed in a sealed Petri® dish that contained a saturated NaCl salt solution setting a relative humidity of 76%. Finally, the devices where placed under a stereoscope to record the time each of them took to empty. The experimental setup can be found in Figure 2.

Results and Conclusions:

We successfully decreased the patterned area with photolithography patterning (Figure 3). Regarding its thickness, the membrane was expected to be ~ 5 μm thick, however it measured ~ 2 μm. We tried to correct this issue—altering the etching by increasing the current density and the exposure time—but the wafer deformed quickly. One reason for the decrease in thickness was that the larger ratio of edge to bulk etch areas led to a larger portion of the current passing through the edges, decreasing etching of the central area. Also, the devices were bondable.

With the emptying times, the membrane total area coverage, and the Darcy's law, we were able to compare each type's global conductance and permeability. Darcy's law states that the global conductance is directly proportionate to the area of PoSi, so it was expected that the full membrane devices had a higher conductance (Figure 4). The small membrane/small pores devices were two times less conductive than full membrane devices. Bigger pores were created in the patterned devices to compensate for the membrane area loss, however these were not as conductive as wanted. The permeability stayed approximately the same; values ranged from 1.25 to 2.25. We concluded that there is a need to increase conductivity for faster response time.

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References:

[1] Pagay, V., et al. Lab Chip 14, 2806-17 (2014).

[2] Ohmukai, M., et al. J. Mater. Sci. 16, 119-121 (2005).

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