Patterning Silicon Nanowire Arrays using EBL

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Abstract:

Silicon nanowires have applications as advanced solar energy collectors, lithium ion anodes, catalysts and biological and chemical sensors. Silicon nanowires have demonstrated superior light absorbance in photovoltaic cells. The peak wavelength of light absorbed is tunable, depending on length, doping, spacing and diameter. Length and doping control in silicon nanowires are fairly well understood. The focus of this project was to develop a method for finely controlling diameter and spacing of silicon nanowires in an array and to transfer technology from ultra-high vacuum (UHV) to more scalable systems. Electron-beam lithography (EBL) was chosen because it can pattern samples with the nanometer resolution required. Using poly (methyl methacrylate) (PMMA) as the electron-beam resist, and electron-beam evaporation to deposit gold, an array of gold catalyst nanodots was developed on the silicon substrate surface. Then silicon nanowires were grown from each gold catalyst dot through vapor-liquid-solid deposition — in which silane decomposes on the catalyst surface, creating a liquid gold silicon eutectic, and a silicon crystal grows epitaxially on the bottom of the eutectic droplet. The goal was to create arrays of nanowires with diameters as small as 20 nm.

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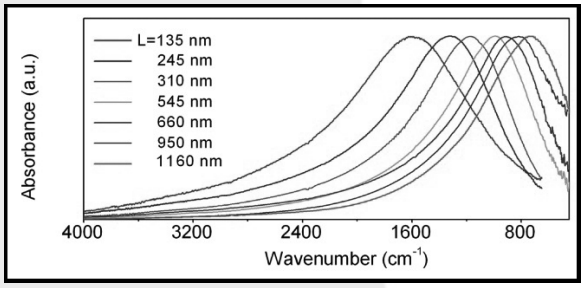


Figure 1: Surface plasmon resonance frequency varies with nanowire dimensions and spacing. (See full color version on page xxxvi.)

Introduction:

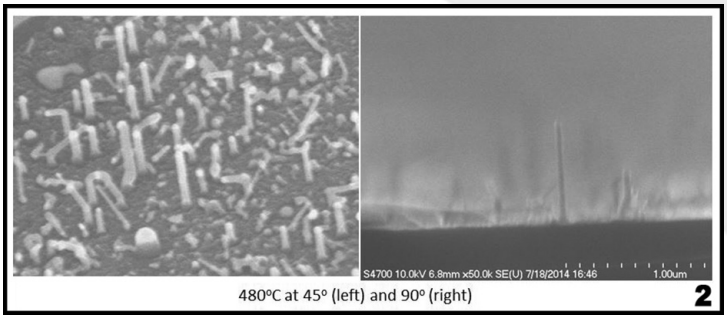
Semiconductor nanowires, also called nanopillars, are of increasing interest in scientific research. Their synthesis methods and chemical, mechanical, electronic and photonic properties have been studied. They may have use as solar cell enhancers [1]. Our research team designed silicon (Si) nanowire synthesis methods with the electronic properties in mind. Surface plasmon resonance frequency varies with nanowire dimensions and spacing (Figure 1) [2], so dimension and spacing control is critical to nanowire function.

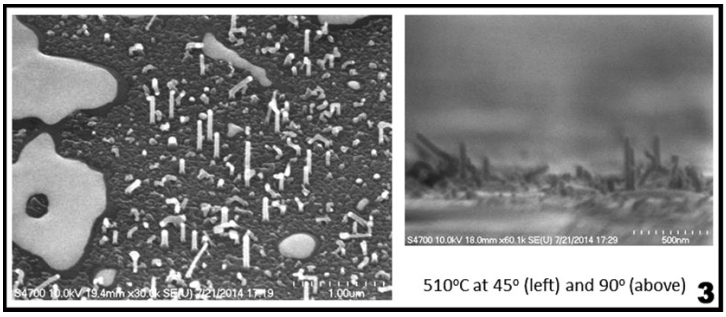
Experimental Procedure:

A set of samples were made by cutting approximately 1 cm^2 from <111> Si wafers, which are necessary — as opposed to <100> Si — to produce vertical nanowires by the vapor liquid solid growth method [3]. The cut samples were then immersed in 10% hydrofluoric acid (49% HF diluted 1:4 in distilled water) for three minutes to remove silicon oxide (SiO_2), rinsed in distilled water and dried with nitrogen. They were immediately placed in an electron-beam evaporator, pumped down to 8×10^{-7} Torr and coated with 3.0 nm of gold (Au). Au-coated samples may have been stored, in clamshell sample holders in a cool dark space in the cleanroom, for as long as a week.

To grow nanowires, the reactor chamber was first vented. The reactor employed was a "CVD FirstNano Graphene Furnace" with quartz chamber, graphite susceptor, RF heating up to 2200°C, turbo pump for base pressure of 6.0×10^{-7} Torr, and fed by argon, hydrogen (H), silane and methane gas lines. An Au-coated sample was immersed in 10% HF for 15s to remove any SiO_2 that may have formed on unprotected surfaces, rinsed in distilled water and dried with nitrogen.

Immediately, the sample was placed onto the reactor susceptor and the reactor was pumped down to a base pressure below 10^{-5} Torr. The pressure was set to 7.0 Torr with only H flowing





Figures 2, above, and 3, below: An inverse relationship was found between temperature and both nanowire kinking fraction and diameter and spacing.

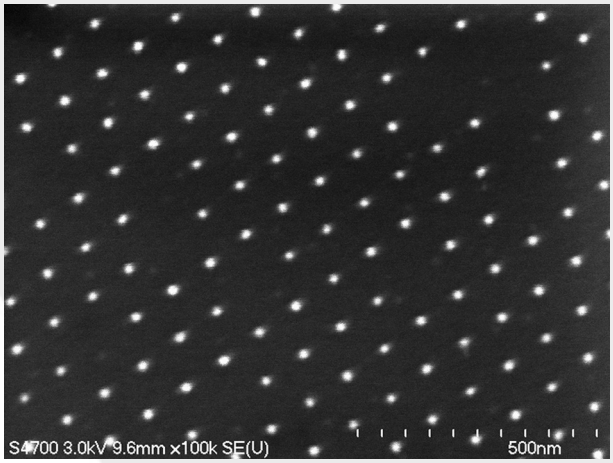


Figure 4: EBL patterning.

at 500 standard cubic centimeters per minute (sccm). The temperature was then ramped up to 400°C over five minutes and finally, to the temperature setpoint over three minutes. After the temperature setpoint was reached, silane was flowed at 25 sccm for ten minutes and the H flow was reduced to 475 sccm to maintain a constant total flow rate. This was regarded as 350 mTorr of silane pressure for comparison to experimental results from other systems. The system was then vented and the sample removed.

The sample was then fractured for imaging by pressing with a scribe at the edge. The larger fragment of the two was placed on the 45° sample mount and the smaller fragment was placed on the 90° mount so that the fractured edge could be viewed by scanning electron microscopy (SEM).

Results, Conclusions, and Future Work:

At the tested silane pressure, an inverse relationship was found between temperature and both nanowire kinking fraction and diameter and spacing (Figures 2 and 3). There was a direct relationship between temperature and wire size uniformity at this silane pressure. Variability in the reactor controls made it difficult to draw strong correlations between temperature and nanowire morphology. More data needs to be collected, after the reactor is fixed, at higher temperatures and different silane pressures to thoroughly understand how process conditions affect nanowire morphology. Once growth conditions are optimized, EBL patterning methods can be applied to achieve an ordered array, or more complex pattern, of nanowires by seeding the gold, or other metal, catalyst exactly where it should go (Figure 4).

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References:

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