Optimizing Insulator Layer Deposition for Diamond MOSFETs

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Abstract:

Field effect transistors (FETs) are important components in electronic devices due to their ability to act as electrical switches. They are comprised of a source, drain and gate, and there must be enough energy potential difference in order for the carriers, electrons or holes, to flow from the source to the drain. One of the ways the effectiveness of these devices can be improved is by applying an insulator or oxide layer on top of the channel layer in order to reduce the number of carriers that escape through the gate contact. In the case of this research, aluminum oxide was analyzed for its application as an oxide layer in these devices.

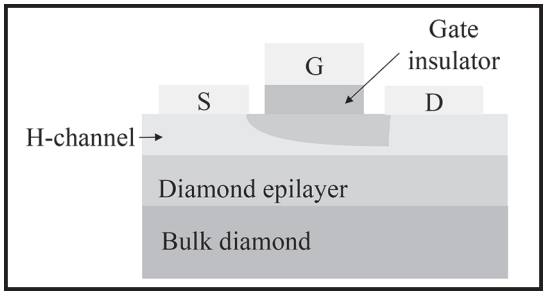

Figure 1: A graphic depicting the cross-sectional structure of the fabricated MOS devices.

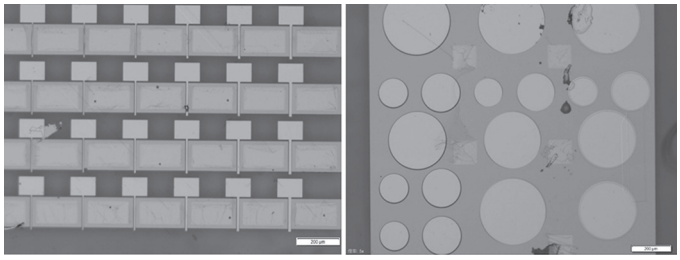

Figure 2: A microscope image of a fabricated FET (left) and diode (right). It should be clear to see the individual source, gate, and drain pairs for the individual FET devices.

Introduction:

It has been found that diamond can be used as a viable substrate for fabricating both field effect transistor devices and diode devices. This is because it is a wide band gap material with a high degree of hardness, thus making it ideal in high-power applications. Additionally, diamond has the ability to have a hydrogen-terminated surface providing it with a high concentration of holes that then act as the carriers in the device. So in a metal oxide semiconductor field effect transistor, or MOSFET, the diamond behaves as the base semiconductor.

Figure 1 shows the current device set up, including demarcations for the source (S), the drain (D), the gate (G), and the gate oxide, aluminum oxide (Al_2O_3). In the image, it also shows two diamond layers, the bulk layer and an epilayer. This epilayer is a high-quality layer that improves the quality of the contacts that are made.

Procedure:

The fabrication process was a multi-step process beginning with the development of the H-terminated surface, which was done through microwave plasma chemical vapour deposition. This also created the diamond epilayer on the bulk diamond to improve the surface quality. Afterwards, photolithography, followed by dry etching and electron gun evaporation, was used to deposit the metals for the key pattern, the mesa structure for the fabricated FETs, and the source and drain. The metals used were titanium, platinum, and then gold.

After the source and drain were completed, the oxide layer of Al_2O_3 was deposited by means of atomic layer deposition (ALD). Three different deposition temperatures were used in order to understand the influence of temperature on the deposition quality and furthermore, on the total current output. After the ALD, photolithography and e-gun

evaporation were used again in order to create the metal component of the gate. Finally, the samples were annealed in order to improve the drain current values.

A set of successfully fabricated MOSFETs and MOS diodes can be seen in Figure 2.

Results and Conclusion:

The electrical properties of the Al_2O_3/H-diamond based metal-oxide-semiconductor (MOS) diodes and MOSFETs were studied. This was done by using a semiconductor probe measuring system where contacts were made to the source, drain and gate, and then the total current observed in the drain was measured. Based on the results, it was found that there exists an ideal deposition temperature range for the Al_2O_3.

The best results were found when the oxide was deposited at 300°C, because it produced ideal capacitance-voltage behavior without flat-band shift in the MOS-diode devices. Figure 3 shows the shift in the hysteresis curve as the deposition temperature was varied.

Additionally, the MOSFET showed good operation with normally-on, ohmic characteristics. The standard drain current versus voltage (IV) was expected to have a linear piece beginning at the origin, before it plateaued into the saturated region. Figure 4 shows an IV-curve for an FET device fabricated at 300°C and then annealed for an hour at 180°C. The maximum drain current it produced was -7.0 mA/mm, which is relatively low.

Future Work:

After establishing a reliable deposition technique and discovering the existence of the ALD temperature window, the next steps are to continue to manipulate the ALD parameters and observe the maximum drain current that is produced. Once devices with a reasonable drain current can be produced and reproduced, it will be able to prove diamond to be a practical and beneficial MOSFET semiconductor substrate.

Acknowledgments:

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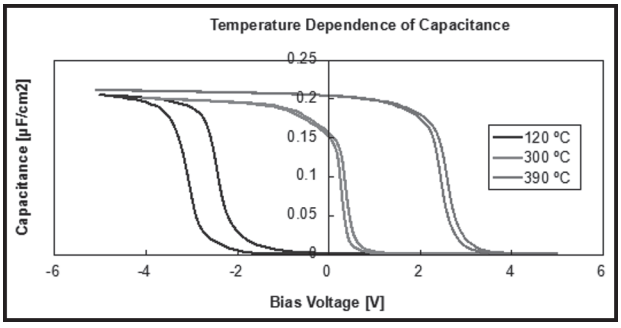

Figure 3: An overlay of the capacitance dependence found for devices fabricated at 120°C, 300°C, and 390°C. The shift in the curve represents an existence of positive charges (shifted left) and negative charges (shifted right), which are not desired.

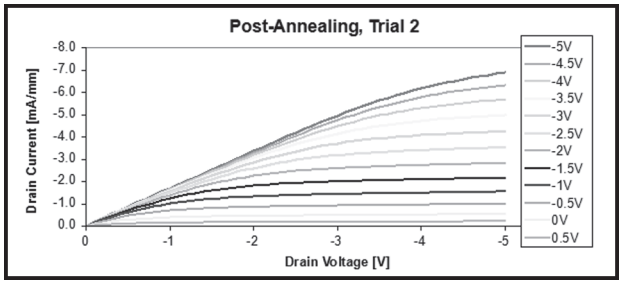

Figure 4: A drain current versus voltage curve for the 300°C trial.