Fabricating Nano-Gap Metal Electrodes using Photolithography

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Abstract:

The ability to measure the electrical properties of individual molecules is a crucial step en route to the possible use of molecules in transistors. Measuring the electronic properties is limited by difficulties encountered when trying to capture a single molecule and place it between two electrodes.

In this work, we are developing a new process to make such measurements possible. Using conventional photolithography, we are designing a procedure to fabricate nano-gap metal electrodes on a wafer scale. During fabrication, the source and drain are connected, and this connection is designed to have a weak spot, which can easily be broken with an applied voltage. By cooling the device to 4K using a liquid helium dewar and applying a voltage, we were able to break the shorted electrodes and create nm-scale gaps.

Introduction:

Having the ability to trap an individual molecule between two electrodes is very desirable for several reasons, two of which are; being able to measure the electrical properties of a single molecule and being able to fabricate devices significantly smaller than previously thought possible. The first step in being able to achieve both of these goals is to have a device in which the gap between the two electrodes is small enough such that a single molecule will fit snugly between them. These devices can be made using electron-beam (e-beam) lithography [1, 2, 3] and photolithography. Both approaches are similar in that in each process, shorted devices are patterned then broken by applying a voltage yielding the desired gap.

The advantage of using e-beam lithography is that very small feature sizes can be patterned which, in turn, can be broken to give gaps on the range of 2-3 nm. Dai et al. and others [3] have already made these devices and the results are shown in Figure 1, showing that breakdown occurs at ~1.68 volts. The inset graph shows the tunneling current across the newly formed gap, indicating a gap size of nm scale. The disadvantages to using e-beam are that it is very time consuming, expensive, and it cannot be mass-reproduced. In this work, our goal is to develop an inexpensive process using conventional photolithography that can make devices similar to those made using e-beam lithography but on a wafer scale.

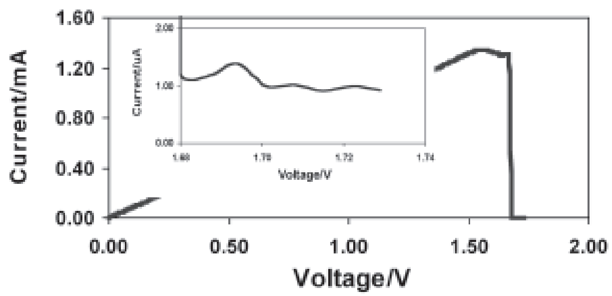

Figure 1: Electrical breakdown data for a device made by e-beam lithography.

Procedure:

In order to obtain the desired gap size between the two electrodes, two separate masks were designed, one for the source electrode (half circle) and one for the drain electrode (small finger). The masks were designed to have various spacings between the electrodes with the hopes that any misalignment would still yield some functional devices. Starting with a p-type silicon substrate, a thin 10 nm gate oxide was grown. The source electrode was patterned using photolithography, and 0.5 nm Ti and 10 nm Au was deposited using e-beam evaporation. The drain electrode was patterned in the same manner, followed by evaporation of another 0.5 nm Ti and 10 nm Au. The unwanted metal and photoresist were removed by soaking the wafer in acetone for three hours. Upon closer inspection, it was determined that most of the devices had gaps between the two electrodes ranging from 100-250 nm (due to misalignment).

The approach we intended to use required a very small overlap of the two electrodes so we patterned the source electrode again. This time only 0.5 nm of

Ti and 7 nm Au were deposited, followed by soaking the wafer in acetone for three hours to remove the remaining photoresist and metal. The devices were then cooled to 4K using a liquid helium dewar followed by electrical breakdown.

Results:

A completed device is shown in Figure 3 with the electrical breakdown data in Figure 2. The break occurred around 6.2 volts, which is a lot higher than we wanted. The e-beam devices broke at ~ 1.6 volts and there was a tunneling current left after the break; the devices we fabricated did not have any tunneling current after the break occurred. Figure 4 is a Scanning Electron Microscopy (SEM) image of a representative device made by photolithography after the break. From this image it can be seen that the breaks were not very clean, but in some regions, the gap is within the desired range. We feel the inconsistent gap ranges across the break are caused by excessive overlap, which requires higher voltage to break the devices resulting in a more violent break.

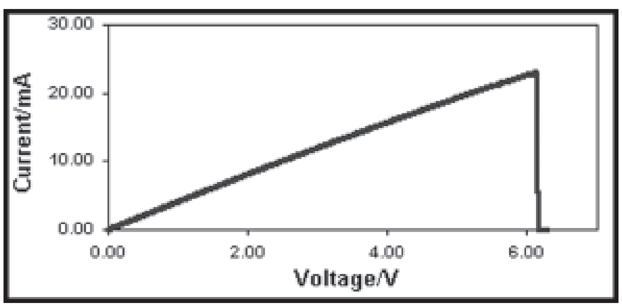

Figure 2: Electrical breakdown data for a device made by photolithography.

Summary and Future Work:

In this work, we have developed a process to fabricate devices with nm scale gaps. The process still needs to be optimized but we feel that we are on the right track and can easily achieve our goal of making 2-3 nm gaps using photolithography.

Our plans include varying the thickness of both electrodes such that one is very thick and the other is very thin. Our hope is that this will allow us to form an even weaker spot, which can be broken at a very low voltage (< 1V). Once the process is optimized, we plan to deposit various molecules in the gaps and begin measuring their electrical properties and determine their possible use in transistors.

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References:

[1] Park, J. et al., "Coulomb blockade and the Kondo effect in single-atom transistors," Nature 417, 722-25 (2002).

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[3] Park, H. et al., "Fabrication of metallic electrodes with nanometer separation by electromigration," Applied Physics Letters 59, 301-303 (1999).

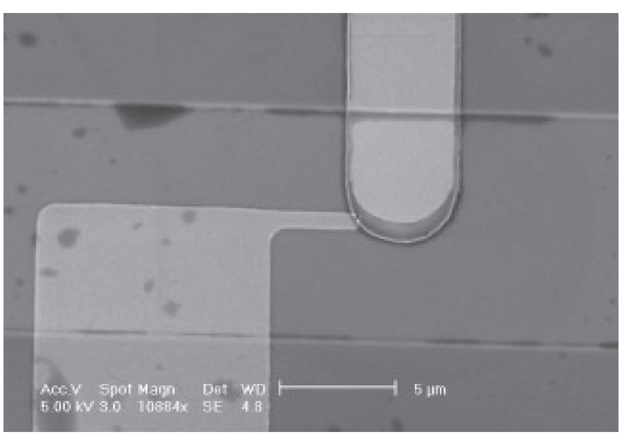

Figure 3: SEM image of completed device made by photolithography.

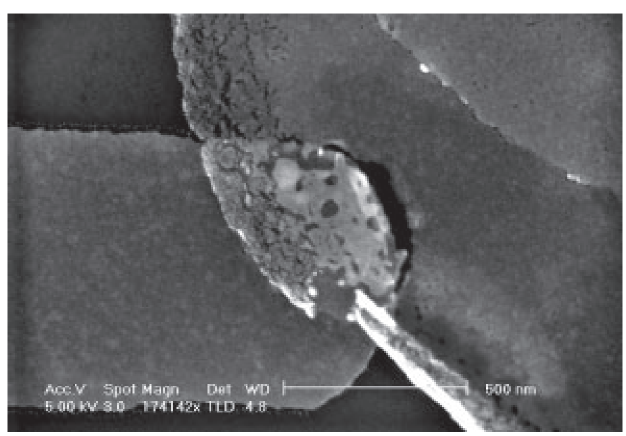

Figure 4: SEM image of a device made by photolithography after electrical breakdown.