

# Making Connections to Molecules for Molecular Electronics

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## Abstract:

Cross-bar molecular electronic devices can be used for both memory and logic purposes. Our project's ultimate goal was to fabricate a cross-bar array to characterize molecule-based electronic junctions using a self-assembling monolayer (SAM) to form the molecular layer. The immediate objectives were to optimize SAM growth on blanket films and to develop a process for patterning the bottom electrodes into a substrate. To study SAM growth, blanket platinum films were evaporated on silicon substrates. The usefulness of chemical-mechanical polishing (CMP) the platinum substrates was also investigated. Using atomic force microscopy (AFM), the CMP and non-CMP samples were characterized for roughness. Octadecanethiol was used to form the SAMs. The SAMs formed were then characterized using AFM, contact angle measurements, and ellipsometry. It was seen that the SAMs were more uniform on the polished substrates. The electrode patterning was done using standard fabrication techniques.

## Introduction:

The motivation for developing molecular electronic devices is the ability to fabricate denser circuits. Traditional devices can take up large amounts of space, but in working with molecular layers, the basic unit of measurement can be brought down from the  $\mu\text{m}$  scale to the molecular scale.

The design of our molecular electronic device is a cross-bar array where a single molecular layer is

sandwiched between two sets of parallel electrodes perpendicular to each other. Before actual fabrication of the device, research had to be done to learn how to produce a uniform layer of single molecules standing up vertically from the surface of the substrate; the process flow for patterning the electrodes also had to be developed. An octadecanethiol self-assembling monolayer (SAM) was used to form the molecular layer. A uniform molecular layer is critical to the device performance because any deformities in the layer, such as separation of molecules due to too much tilt or holes in the layer, could cause undesirable short circuits to form between the electrodes in later fabrication processes.

Using nano-imprint lithography, H-P Labs were able to fabricate a similar device where each cross point was able to be used as an active memory cell. By simultaneously applying different voltages to the electrodes, the resistance at each cross point could be reversibly switched. In doing so, an electric current could be switched on and off creating rewritable, nonvolatile memory, and in other settings could be used for demultiplexing and multiplexing [1].

## Procedure:

Research began by using e-gun evaporation to evaporate 1400 Å blanket platinum films with 100 Å titanium adhesion layers onto silicon wafers with a native oxide layer. Some of these samples were then chemical-mechanical polished (CMP). In performing the CMP, a platinum slurry wasn't commercially available so the slurry normally used for  $\text{SiO}_2$ , which

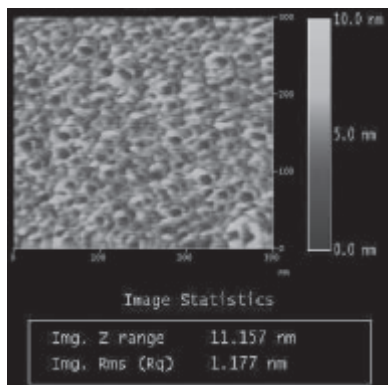


Figure 1: SAM growth on non-CMP sample.

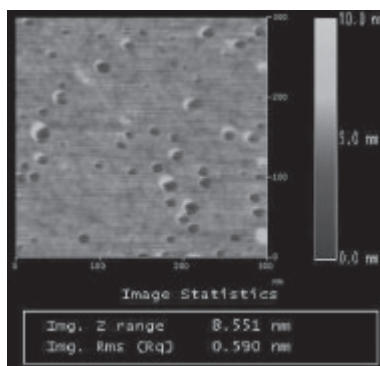


Figure 2: SAM growth on CMP sample.

is the least chemically aggressive, was used. Using the atomic force microscope (AFM), the surface roughness of all the samples was analyzed. The surface roughness is important because a more uniform SAM forms on a flatter surface. It was seen with the AFM that the non-CMP samples had a RMS roughness of about 6-8 Å, while the CMP samples had a RMS roughness of 3-4 Å.

Next a 24-hour liquid phase deposition process was used to grow the octadecanethiol SAM on the substrate surfaces. The AFM was used again to examine the growth of the monolayer. Figure 1 and Figure 2 show the SAM growth on the non-CMP and CMP samples, respectively.

The design of the electrodes called for a set of eight parallel platinum strips, 15 μm wide and 1000 μm in pitch, which fanned out to 200 μm by 200 μm macroscopically accessible contact pads. To perform the patterning of the bottom electrodes, a silicon wafer with 6000 Å of thermal oxide was started with. Soft contact photolithography was used to transfer the design from the mask to the resist. A reactive ion etch was used to etch down 1500 Å into the unprotected thermal oxide. Again, e-gun evaporation was used to evaporate a 1400 Å platinum film with a 100 Å titanium adhesion layer onto the substrate. Lift-off was then carried out. The electrodes were made ideally flush with the surface to prevent complications in the CMP and SAM growth. Again, some of the patterned samples were then CMP. The next steps were to grow SAMs on the samples and form the top electrodes. The top electrodes were to be formed by evaporating through a silicon nitride shadow mask of the same dimensions. This work was performed by an REU intern from the Cornell Center for Materials Research who was also on this project.

### Results and Conclusions:

As shown in Figure 1, there's a denser amount of holes in the monolayer on the non-CMP sample. Whereas in Figure 2, it shows that greater defect-free areas are covered on the CMP sample. In the lower left, there's an ~100 nm by 100 nm area of a perfectly

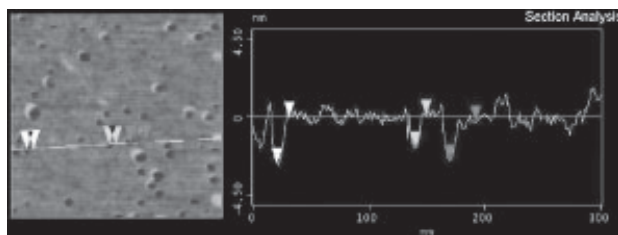


Figure 3: Line scan of SAM on CMP sample.

uniform monolayer. Looking at the profile of the non-CMP sample with a line scan showed that there were many islands of about 23 Å in height, the theoretical length of the octadecanethiol molecule. Figure 3 shows a line scan of the monolayer on the CMP sample in Figure 2. The left part of the graph shows a relatively flat section which corresponds to a uniform layer of densely packed molecules standing vertically. The pits in this scan are again about 23 Å deep, showing where there are holes in the monolayer. From this analysis, it's clearly concluded that the SAMs grow more uniformly on CMP platinum films than on non-CMP ones.

To begin the fabrication of the device, a process to pattern the bottom electrodes into the substrate was developed. The result of this process can be seen in Figure 4, a scanning electron microscope (SEM) image of the patterned wafer.

### Future Work:

The next steps in the project are to finish the fabrication of the device for the testing and characterization of molecular electronics. The next area of challenging research is how to integrate molecular electronic devices with existing electronics, such as CMOS [1].

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### References:

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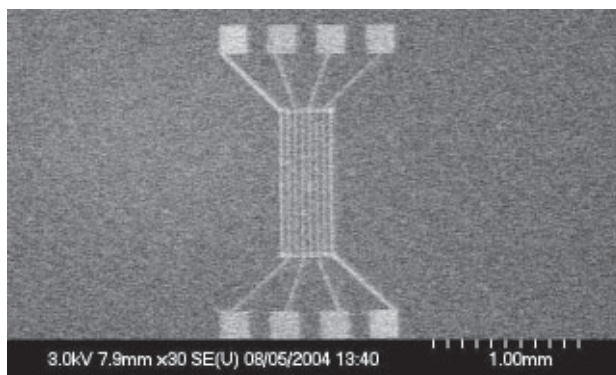


Figure 4: SEM image of bottom electrodes.