Silicide Contacts to Ultra-Thin Silicon Films for Nano-Scale Devices

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Abstract:

The goal of this project was to develop and understand techniques to produce ohmic contacts using cobalt silicide, and to use this method to achieve a silicide thickness of 10 to 15 nm. Test structures were fabricated with varying thicknesses of N^+ polysilicon, and factors contributing to polysilicon loss and poor silicidation were determined, as well as optimal annealing temperatures. Electrical and film thickness measurements taken on the finished wafers showed the presence of cobalt silicide on a 17 nm film of polysilicon.

Introduction:

Techniques have been developed to build nano-scale devices on single-crystal silicon films as thin as tens of nanometers, such as transistors and memories with 30 nm gates built on 15 nm silicon films. However, at this size it is difficult to make low-resistance, device-quality ohmic contacts to the silicon, since interface reactions are often on the same order of thickness as the silicon film itself.

A solution to this problem is silicidation, an annealing process that results in the formation of a silicon-metal alloy. The advantages of using silicide include: less parasitic resistance, lower thin-film resistivity than polysilicon, higher thermal stability, and protection of the contact interface from surface effects. Since its resistivity is approximately 1/5 that of doped polysilicon, cobalt silicide serves well as an ohmic contact and significantly improves the performance of devices that use it [1].

Cobalt was chosen specifically for this project because it consumes less polysilicon in the process and produces more silicide than the other available metals. Also, its thin-film resistivity of 14-20 μΩ-cm is one of the lowest among common silicides [2].

Procedure:

Three fundamental test devices, as shown in Fig.1, were designed. The first, a transmission line structure,

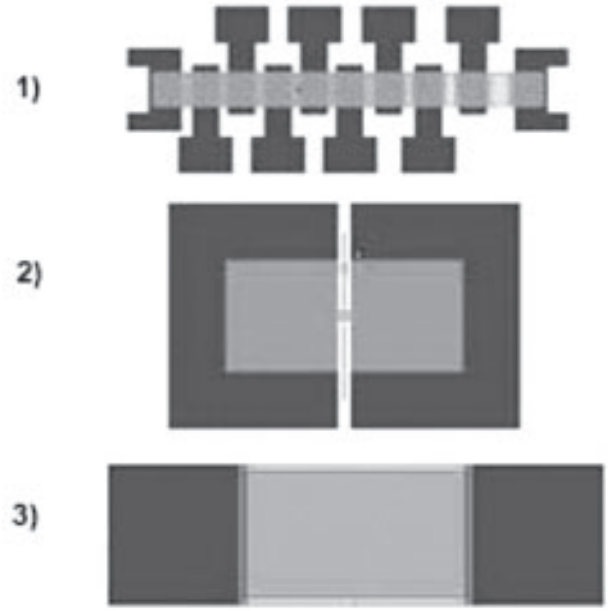

Figure 1: Test structure layouts.

tests contact resistance. The second, consisting of two contacts, monitors the formation of silicide around a thin strip of silicon dioxide that imitates the gate of a transistor. The third, a single via with varying separation between the metal interconnect pads, tests the resistance of the metal to the silicide. These designs were also modified to make devices to monitor effects on silicidation from via size, active region width, and slanted sidewalls.

Masks were made for the final layout, and pseudo-SOI wafers were prepared for device fabrication. The wafers were divided into groups, each having 18, 41, 47, or 71 nm of N^+ polysilicon on top of 500 nm of SiO_2. After a thin sacrificial oxide growth and deposition of 50 nm of low stress nitride, the polysilicon active regions were lithographically defined and plasma etched. A local oxidation step grew additional oxide around the active regions, and then a hot phosphoric acid bath removed the remaining nitride.

Next, 100 nm of low temperature oxide was deposited, and the contacts were patterned and etched through the LTO onto the active regions. Cobalt was

then sputtered onto the wafers, followed by titanium to protect the cobalt from oxidation. The first rapid thermal anneal, just to start the silicidation reaction, was performed at 550°C on one group of wafers and at 450°C on the next. A Nanostrip dip selectively etched the non-silicided metal. Finally, the second anneal was performed at 700°C to ensure that the cobalt silicide was in the correct phase, $CoSi_2$ rather than CoSi or Co_2Si.

Results:

After the etch that opened the contact regions, film measurements showed that negligible amounts of polysilicon remained within active regions on all of the wafers except for the group with the greatest polysilicon thickness. This loss was due to the lateral etching of polysilicon during the oxide etching process, and also to oxide's property of consuming polysilicon during growth.

Several bare N-type wafers and wafers with 100 nm of LTO that were used during the metal sputtering were also annealed in order to experiment with annealing temperatures. Originally, the first rapid thermal anneal was planned to be at 550°C, but the test wafers exhibited a flaky, non-conducting surface. Other wafers that underwent the fabrication process up to the first anneal exhibited a brittle, non-conducting layer that had to be scratched through in order to get contact between the probe tips and the vias. Annealing at 450°C gave consistently better results; Figure 2 shows the difference in appearance before and after the anneal.

Ultimately, wafers from the 71 nm polysilicon group exhibited silicide formation between 17 nm of polysilicon and a metal layer consisting of 20 nm of cobalt and 7 nm of titanium. The silicide thickness was not determined, but preliminary electrical measurements after the first anneal showed resistances between 465 Ω and 535 Ω on contacts in the silicided areas of the wafer, resistance on the order of $10^3\Omega$ over contacts in non-silicided areas, and resistance on the order of 10^{11} Ω (essentially zero current) over field oxide. The phenomenon of silicidation at relatively low temperatures, below 600°C, was also observed. Figure 3 shows a sample that had 20 nm of cobalt and 7 nm of titanium over a bare wafer grew approximately 20 Å of cobalt silicide after undergoing transmission electron microscopy (TEM).

Future work includes determining the thickness of the silicide grown on the samples that underwent the full fabrication process, and applying this process toward fabricating transistors.

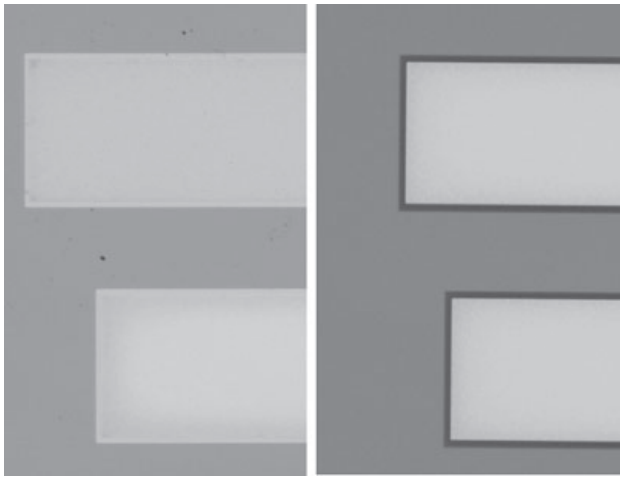

Figure 2: Left: before anneal. Right: after anneal.

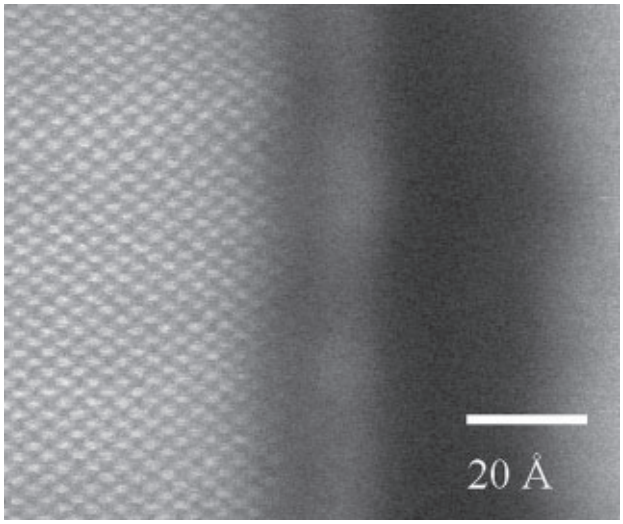

Figure 3: TEM of silicide (center) at Si-Co interface.

Acknowledgements:

My sincerest thanks to Dr. Tiwari and the Tiwari group for all their help, Michael Guillorn for the TEM work, Melanie-Claire Mallison, and the CNF staff. I also thank the NNIN and National Science Foundation for making this experience possible.

References:

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