Micro-Scale Two Phase Flow Device Fabrication

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Abstract:

As computer chips get smaller and faster, there rises a need for new innovative ways to keep them cool without making the computer chip bulky. This study investigated the possible heat transfer abilities of micro-scale two-phase flows, primarily in water. The devices used varied in surface roughness, temperature, flow regime, length, and methods of two-phase heat exchange. They were fabricated with three main components: micro-channels, a heater, and a thermistor. The micro-channels were etched into silicon substrates and then bonded to glass. An external pump created the flow through the channels. On the bottom sides of the substrates, in order to model an application such as a hot computer chip, Aluminum heaters were installed. Also, for temperature measurement accuracy, polysilicon thermistors were introduced underneath the heaters (in close proximity to the channels). Preliminary testing has begun, but no results have been measured currently.

Introduction:

The present methods of heat dissipation could pose a problem in the near future for the miniaturization of the electronic world. The heat transfer capabilities of two-phase flow on the micro-level demonstrate an effective response to this problem. Unlike the common heat transfer of single-phase flow available today on the macro-scale, in radiators for example, two-phase micro flow offers two exceptional advantages. Though both single- and two-phase flows can occur at the micro-scale, the convective heat transfer coefficients of two-phase flows are predicted to be higher than those of single-phase flows, which will allow energy to be removed at a higher rate. Also, the energy exchange involved with phase change from liquid to vapor will facilitate more heat dissipation than that of single-phase flow. Our study works primarily with water but the idea of two-phase flow heat transfer is applicable to any substance.

Procedure:

The devices were devised of three major components: A thermistor, a heater, and the micro-channels. The thermistor and heater were both located on the bottom side and the micro-channels on the top side.

Thermistor: Using a standard silicon wafer, a 0.5 μm layer of thermal oxide was grown on both sides with a MOS furnace. Then, on the top side, another 1 μm layer of oxide was deposited using PECVD which served as the hard mask for the micro-channel deep etch in a later step. This step designated the 'top side' of the wafer. A 2 μm layer of polysilicon was deposited next using a LPCVD MOS furnace. Then, on the bottom side of wafer, a thermistor was etched into the polysilicon using CF_4 reactive ion etch in a PT 72 after the necessary photolithography. This was followed by the metallization of the thermistor vias with 150Å of Ti for adhesion and 0.3 μm of Al+1%Si+4%Cu in the CVC sputtering machine. Following photolithography of the vias, the Al+1%Si+4%Cu was etched into the thermistor vias using Type A Aluminum Etchant. The Ti was etched using 10:1 HF. In order to isolate the thermistor and vias, a protective layer of 1 μm oxide was deposited using PECVD.

Heater: On the bottom side, over the isolated thermistor component, the metallization of the heater and its vias was achieved with the CVC sputtering machine. A 150 Å Ti adhesion layer, a 0.5 μm Al+1%Si+4%Cu layer for the heater, and a 1 μm Cu layer for the vias of the heater were respectively deposited. Basic photolithography was used to pattern the heater's vias into the Cu layer and then the Cu was etched using Copper Etchant. Next, the pattern for the heater was imposed over the existing vias with contact photolithography and the heater itself was etched with Aluminum Etchant Type A. The remaining adhesion layer of Ti was etched using a 10:1 HF dip. Another isolating protective layer of 1 μm oxide was deposited over the heater and its vias using PECVD.

Micro-Channels: On the top side, after the photolithography of the micro-channels was completed, the hard mask for the subsequent deep etch, or Bosch etch, of the micro-channels was made by etching the polysilicon and oxide layers in a PT 72 with a CHF_3 plasma etch. The Unaxis 770 was used to etch the actual channels 100 μm initially, with a pause when the photoresist was removed, and then was continued 150 μm more. A protective 1 μm oxide layer was then deposited with PECVD. The micro-channels are shown in Figures 1 and 2. Figure 1 illustrates micro-channels with re-entrant cavities and Figure 2 shows a close-up of the actual micro-channels.

Access to Channels: On the bottom side, the photolithography for the access to channels was performed and then followed by the etching of the 2.5 μm of oxide layers in the PT 72 with a CHF_3 plasma etch. The first 100 μm of the through-etch was realized with the Unaxis 770, only stopping briefly to remove the photoresist. Then the through-etch for access to the channels was completed in the Unaxis 770.

Sealing of Channels: First, the bottom side was coated with photoresist. Then, the oxide layer on the top side was removed with BOE 6:1. The wafer was then anodically bonded to a Pyrex® glass wafer using an EV501 wafer bonder.

Access to Heater/Thermistor: A window photolithography was done on the bottom side and succeeded by an oxide etch in the PT 72 with a CHF_3 plasma etch allowing contacts to be made with the heater and thermistor. Finally, the wafer was cut into singular devices with a wafer saw making them ready for the fixture used in experimentation. Experiments are currently being carried out with results pending.

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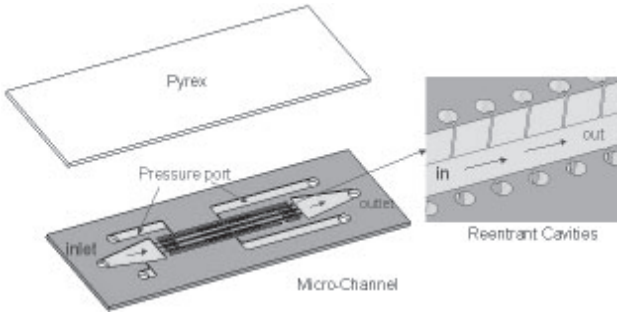

Figure 1, above: Sample micro-channel features.

Figure 2, below: Micro-channels with re-entrant cavities to facilitate phase change.