Thermal Stability of Ge-on-Si Thin Films

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Abstract:

The purpose of this project was to examine the effects of thermal annealing on film quality germanium (Ge) grown directly on silicon (Si), as measured by atomic force microscopy (AFM). The temperature stability of the Ge-on-Si films was observed for different annealing temperatures and times.

AFM scans the sample surface to image the surface topography. These images can then be used to determine the surface roughness of the films, which indirectly provides an indication of film quality. For this experiment, thermal annealing conditions were applied to a set of eight wafers, each with a different Ge-on-Si growth condition. Each wafer was labeled and subdivided into 10 pieces.

The first set of four wafers consisted of blanket Ge films grown over the entire Si wafer, with no additional layers. The second set had blanket Ge films, but with a thin high-κ dielectric deposited on top. The 10 pieces of each wafer consisted of a control piece (with no thermal annealing), a piece used for film thickness measurement by AFM step height, 4 pieces that underwent rapid thermal annealing, and 4 pieces that were furnace annealed.

All eighty pieces (8 wafers times 10 pieces each) were measured using the AFM system.

Introduction:

Metal-oxide-semiconductor (MOS) capacitors are two-terminal semiconductor devices where a dielectric insulator separates the metal from the semiconductor. The insulator is silicon dioxide (SiO_2) because of its compatibility with conventional Si processes. The MOS capacitor is the foundation the metal-oxide-semiconductor field-effect transistor (MOSFET) device. The MOSFET structure comprises a gate layered on an insulator, layered on a semiconductor channel that separates the source and drain. When a voltage is applied to the gate, the MOSFET operates as a semiconductor switch that connects the source and drain terminals by creating a conducting channel region filled with charge carriers (electrons or holes). The gate of the MOSFET controls the number of charge carriers in the channel.

The charge carriers in the channel have a property called mobility (μ). The mobility of the charge carriers determines the current capacity of the MOSFET, which in turn determines the switching speed of a logic circuit that incorporates MOSFETs. The advantage of Ge is it produces higher μ (for both electrons and holes) than Si. It's difficult to grow Ge on Si because of the 4% larger lattice constant of Ge compared to Si. However, very thin Ge films can still be grown on Si at low growth temperatures. The thermal stability of these thin Ge-on-Si films should be examined to determine their resilience to high-temperature processing.

Ge MOSFETs have drawn more attention in the research literature in recent years due to the advent of high-κ dielectrics. High-κ dielectrics have been shown to be compatible with Ge. In addition, high-κ dielectrics are effectively thinner (but physically thicker) than SiO_2 layers because of their higher dielectric constant, therefore reducing gate leakage.

Figure 1 shows leakage characteristics for a Ge-on-Si film with hafnium oxide (HfO_2) dielectric and TaN metal, which are greatly affected by film quality. The purpose of this work is to improve leakage characteristics of Ge-on-Si MOS capacitors. Since the Ge film quality determines the electrical quality

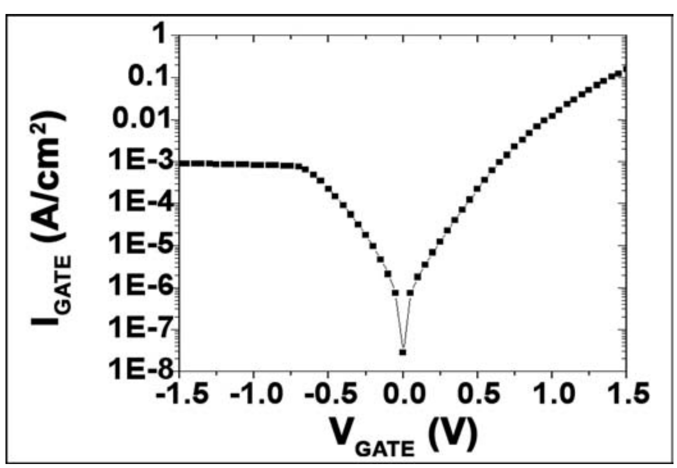

Figure 1: Gate leakage characteristics of Ge-on-Si MOS capacitor.

of the MOS capacitors, it is important to study how film quality maintains throughout the MOS fabrication process, so thermal stability studies have been performed for thin Ge-on-Si films.

Experimental Procedures:

The Ge-on-Si films were already fabricated for use, using ultra-high-vacuum chemical vapor deposition (UHVCVD). The high-κ deposition, HfO_2, was sputtered over the germanium at 60-70Å thickness, deposited by reactive DC magnetron sputtering.

After the growth process was completed, the eight wafers were labeled with an alphabet and then split into 10 pieces where a number (ranging from 0-9) was applied. By doing so, we are able to then apply thermal annealing conditions properly in accordance to the number. The 10 pieces of each wafer consisted of a control piece (piece 8, with no thermal annealing), a piece (piece 9) used for film thickness measurement by AFM step height, 4 pieces (pieces 4-7) that underwent rapid thermal annealing (RTA), and 4 pieces (pieces 0-3) that were furnace annealed. Then time (in minutes), temperature (in C^{o}), roughness (in nanometers, nm), and the film's thickness were recorded for each sample.

Conclusion:

Figure 2 shows a comparison on blanket Ge films both furnace (left set of plots) and RTA (right set of plots) anneals. There was no significant difference in roughness between furnace and RTA annealed samples.

In Figure 3, we see that the Ge films with no high-κ have higher roughness than those films with high-κ whether furnace or RTA annealed under the assumption that the high-κ improves the stability of Ge. At 600°C, 30 min, the plot dropped because all of the Ge desorbed off, leaving only bare silicon to be measured.

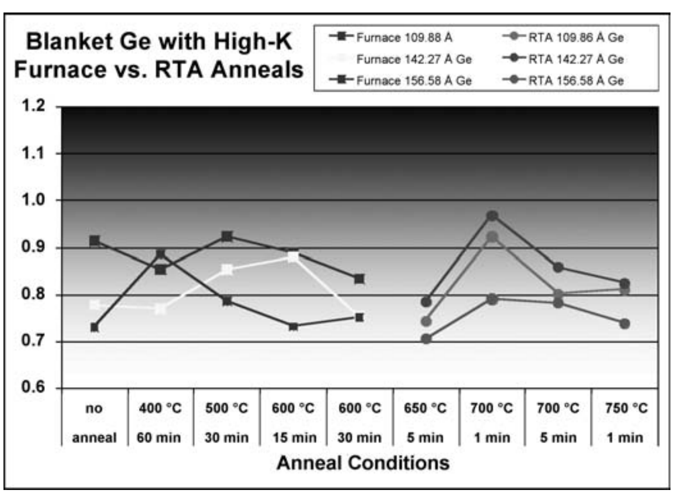

Figure 2. Comparison of surface roughness for furnace and RTA annealing.

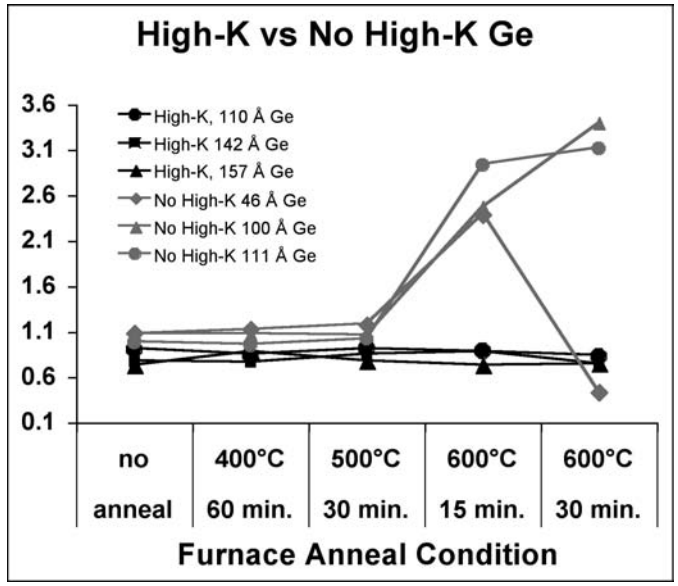

Figure 3. Comparison of surface roughness for high-κ and non-high-κ samples.

Future Work:

Future revisions will focus on the study of area dependency, which would require developing patterned wafers. The patterned wafers will consist of a field oxide layer thermally grown on a Si wafer with windows, with different areas etched into the oxide and Ge selectively grown inside the patterned windows. The objective is to compare the blanket wafers to the patterned wafers to see which film has a higher quality when used for Ge MOSFETs. The completion of RTA anneals for blanket Ge films without a high-κ are needed to be compared to RTA anneal with the additional layers.

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References:

[1] R. F. Pierret, "Field Effect Devices," Second Edition, Addison-Wesley, 1990.

[2] B. G. Streetman and S. Banerjee, "Solid State Electronic Devices," Fifth Edition, Prentice Hall, 2000.